

MOSFET - Power, Single N-Channel, TOLL

40 V, 0.57 mΩ, 300 A



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NVBL50D5N04C

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- Small Footprint (TOLL) for Compact Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DS}	40	V	
Gate-to-Source Voltage	V_{GS}	+20/-16	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D 300	A
		$T_C = 100^\circ\text{C}$	300	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D 198.4	W
		$T_C = 100^\circ\text{C}$	97.4	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D 65	A
		$T_A = 100^\circ\text{C}$	46	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D 4.3	W
		$T_A = 100^\circ\text{C}$	2.1	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM} 4700	A	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	170	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 55 \text{ A}, L = 1 \text{ mH}$)	E_{AS}	1512	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

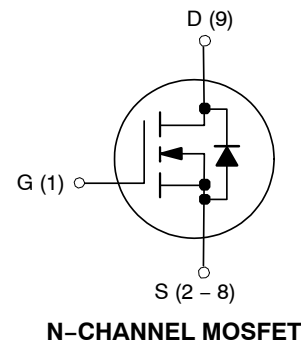
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	0.77	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	35	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Current is limited by bondwire configuration.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
40 V	0.57 mΩ @ 10 V	300 A



**H-PSOF8L
CASE 100CU**

ORDERING INFORMATION

Device	Package	Shipping†
NVBL50D5N04CTXG	H-PSOF8L (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Table 1. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			21.3		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 175^\circ\text{C}$		1	mA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +20/-16 \text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 475 \mu\text{A}$	2	2.8	4	V
Threshold Temperature Coefficient	$V_{GS(th)}/T_J$			-7.4		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$		0.5	0.57	$\text{m}\Omega$

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		12600		μF
Output Capacitance	C_{oss}			6705		μF
Reverse Transfer Capacitance	C_{rss}			227		μF
Gate Resistance	R_g	$V_{GS} = 0.5 \text{ V}, f = 1 \text{ MHz}$		1.8		Ω
Total Gate Charge	$Q_{G(tot)}$	$V_{GS} = 10 \text{ V}, V_{DS} = 20 \text{ V}, I_D = 50 \text{ A}$		185		nC
Threshold Gate Charge	$Q_{G(th)}$	$V_{GS} = 0 \text{ to } 2 \text{ V}$		22		nC
Gate-to-Source Gate Charge	Q_{gs}	$V_{DD} = 32 \text{ V}, I_D = 50 \text{ A}$		48		nC
Gate-to-Drain "Miller" Charge	Q_{gd}			38		nC
Plateau Voltage	V_{GP}			4.2		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10 \text{ V}, V_{DD} = 20 \text{ V}, I_D = 50 \text{ A}, R_{GEN} = 6 \Omega$		40		ns
Turn-On Rise Time	t_r			84		ns
Turn-Off Delay Time	$t_{d(off)}$			164		ns
Turn-Off Fall Time	t_f			81		ns

DRAIN-SOURCE DIODE CHARACTERISTICS

Source-to-Drain Diode Voltage	V_{SD}	$I_{SD} = 50 \text{ A}, V_{GS} = 0 \text{ V}$		0.76	1.2	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0 \text{ V}, dI_S/dt = 100 \text{ A}/\mu\text{s}, I_S = 50 \text{ A}$		108		ns
Charge Time	t_a			62		ns
Discharge Time	t_b			46		ns
Reverse Recovery Charge	Q_{rr}			288		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures

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TYPICAL CHARACTERISTICS

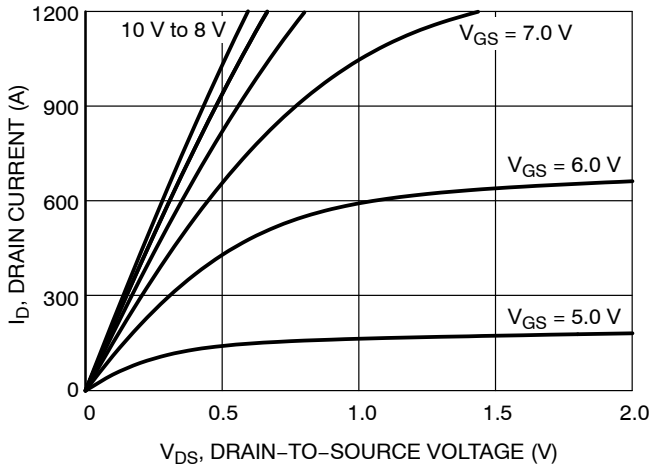


Figure 1. On-Region Characteristics

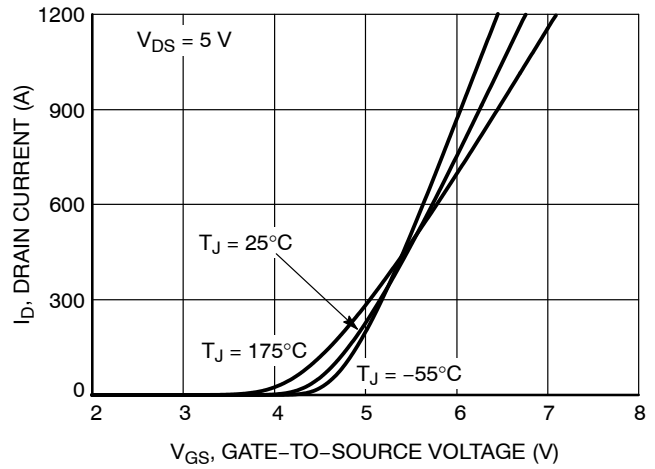


Figure 2. Transfer Characteristics

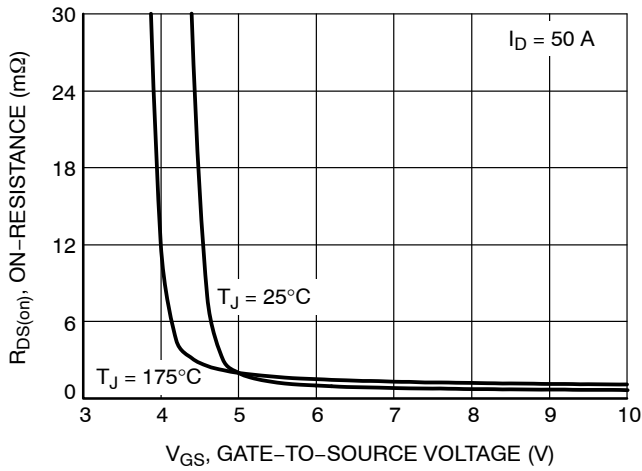


Figure 3. On-Resistance vs. Gate-to-Source Voltage

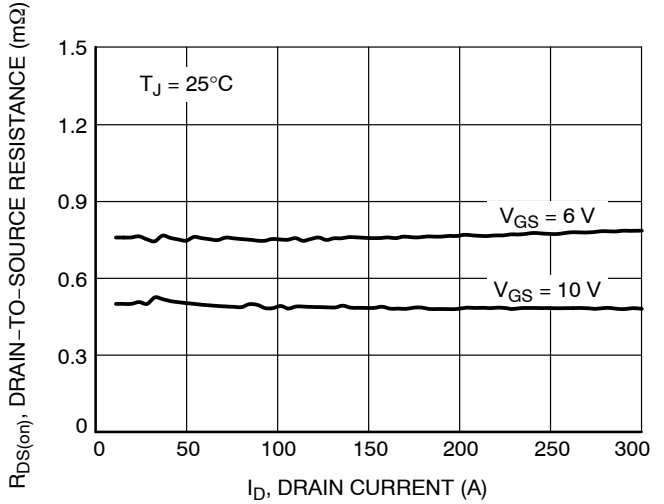


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

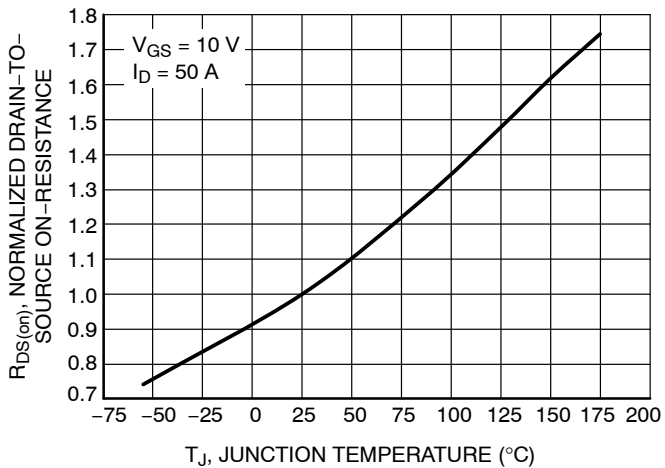


Figure 5. On-Resistance Variation with Temperature

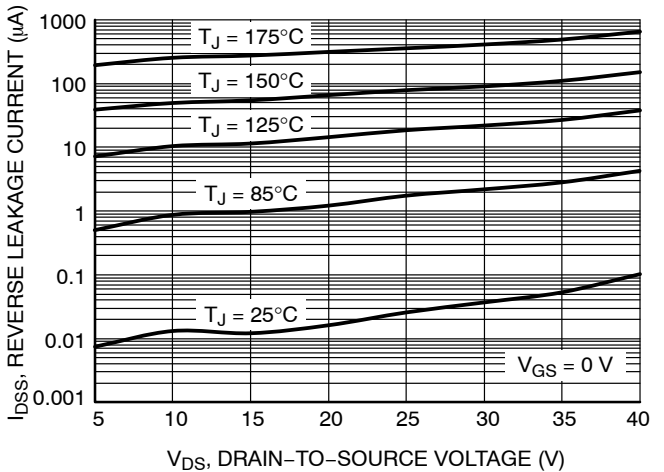


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

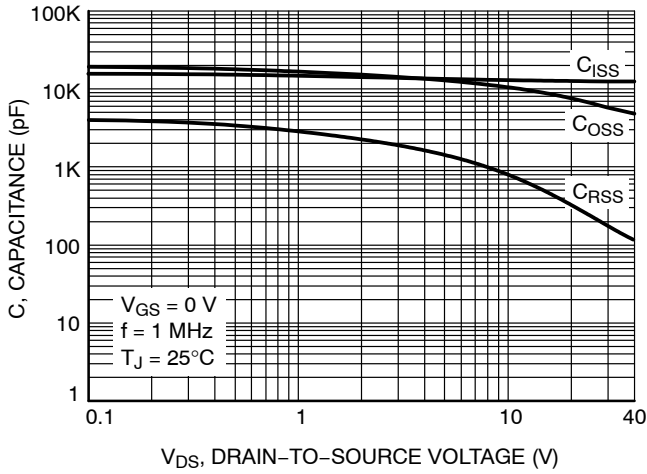


Figure 7. Capacitance Variation

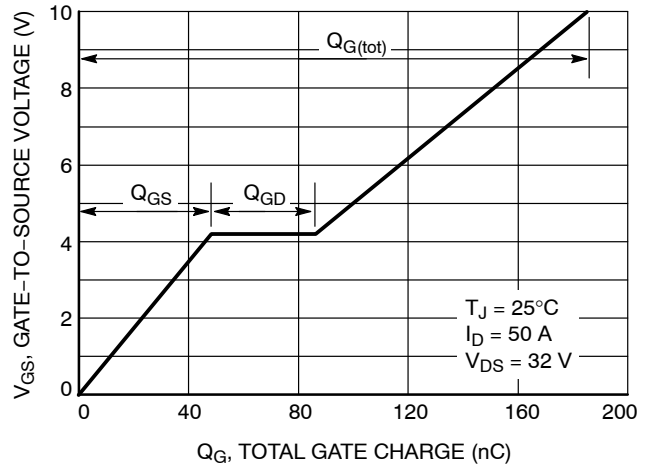


Figure 8. Gate-to-Source Voltage vs. Total Charge

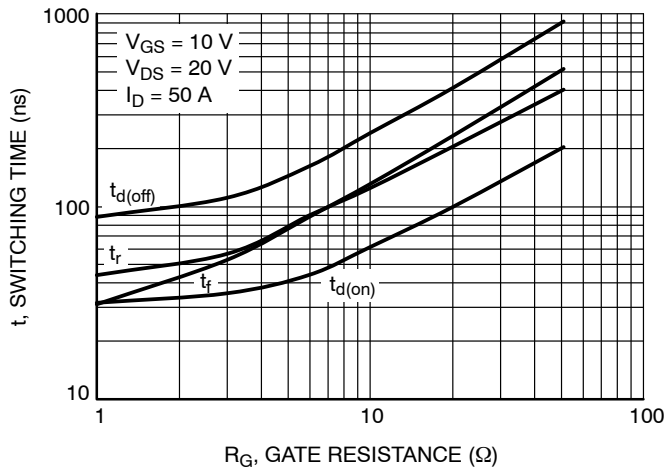


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

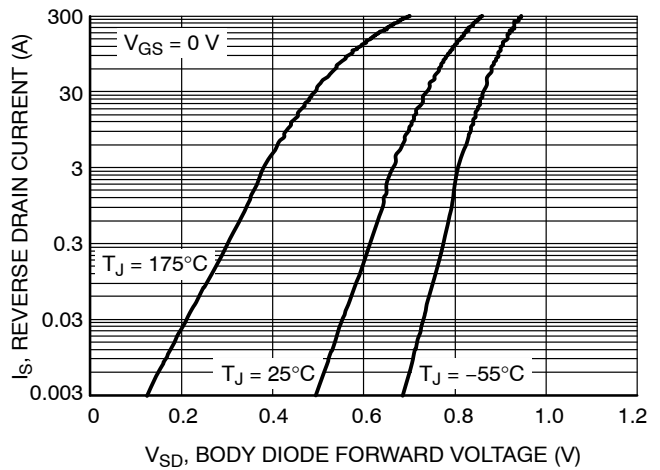


Figure 10. Diode Forward Voltage vs. Current

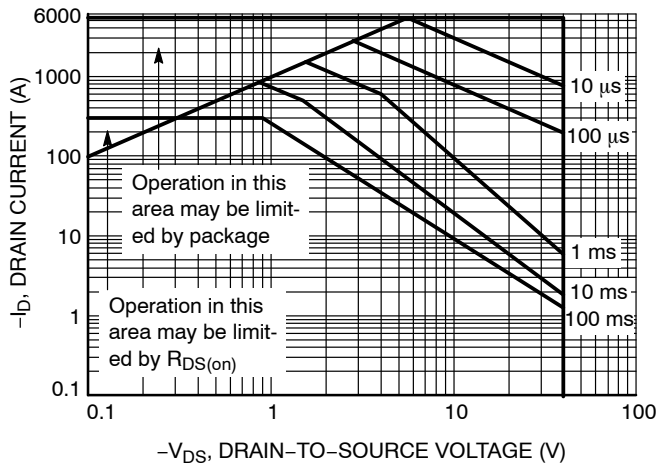


Figure 11. Forward Biased Safe Operating Area

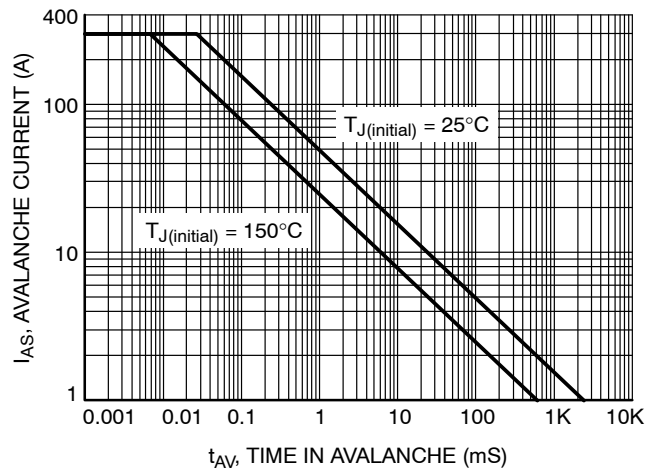


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

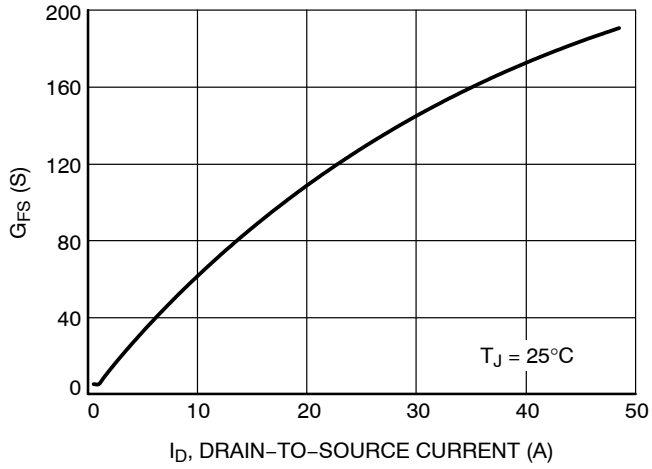


Figure 13. G_{FS} vs. I_D

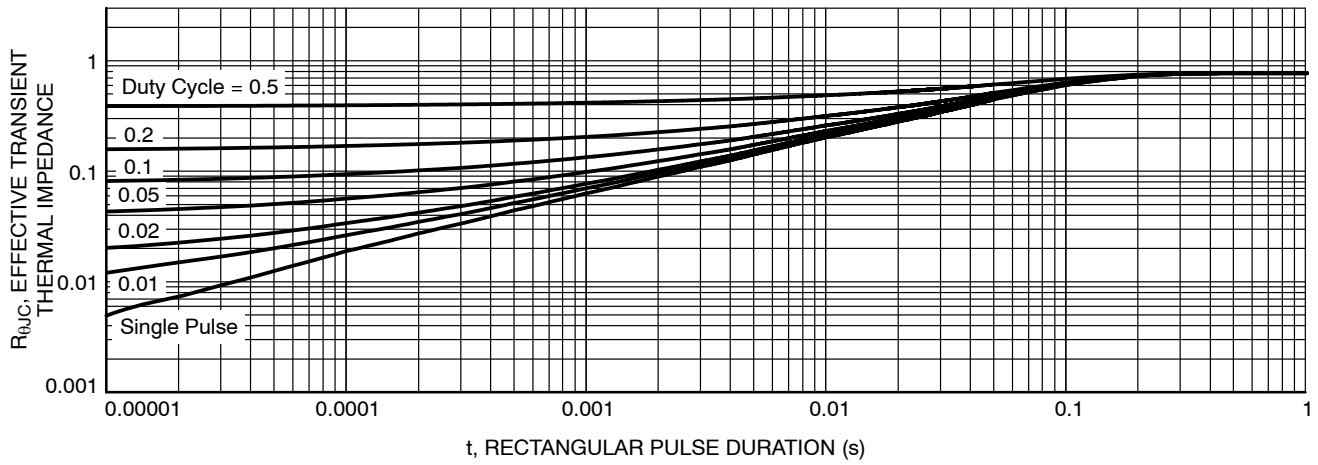


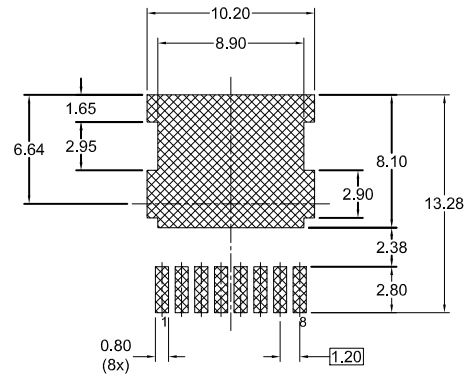
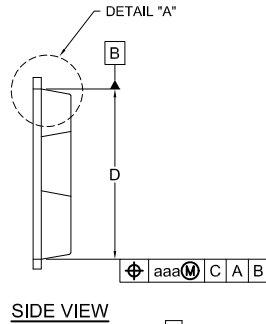
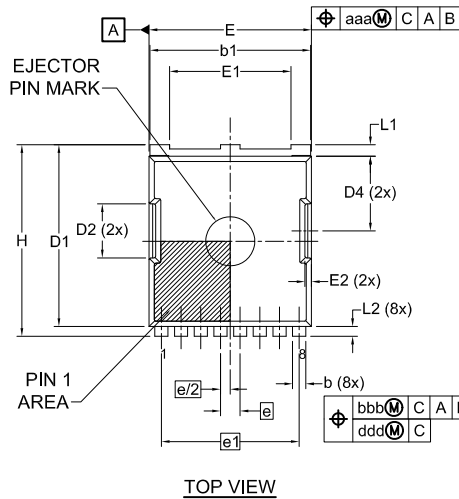
Figure 14. Transient Thermal Impedance

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



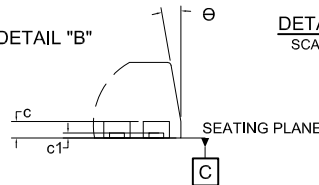
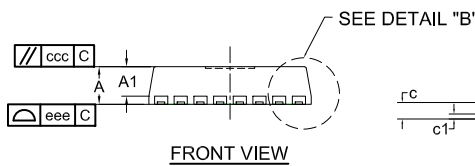
H-PSOF8L 11.68x9.80
CASE 100CU
ISSUE C

DATE 22 MAY 2023



LAND PATTERN RECOMMENDATION

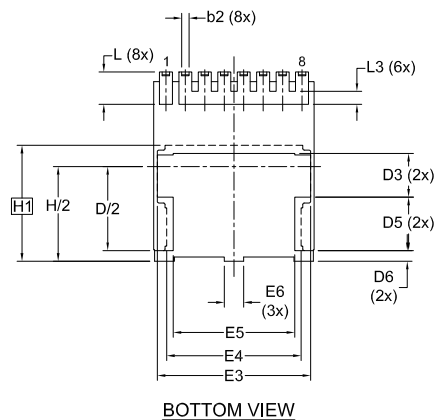
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DETAIL "A"
SCALE: 2X

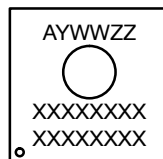
NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DETAIL "B"
SCALE: 2X

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	—	—
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
θ	0°	—	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

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