Application Report
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Using the CDCE421 as a Frequency Synthesizer

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ABSTRACT

This application report is a general guide for using the CDCE421 from Texas Instruments as a frequency synthesizer for data communications. This report explains the basic functionality and methods for using the device efficiently. The document concludes with several recommendations for line termination and power-supply decoupling.

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1 Introduction

A phase-locked loop (PLL) is a closed-loop system that generates a signal related to the frequency and phase of an input reference signal. It typically involves locking its output (derived from a high-Q device) to its input, which is usually from a low-Q device. The PLL responds to input frequency and phase variations by automatically raising or lowering the frequency of the controlled oscillator through feedback, until the output is aligned with the system phase and frequency. A practical phase PLL usually assures lock in phase, but a lock in frequency with 0 ppm error has not yet been demonstrated. Typical commercial PLLs demonstrate ensured frequency lock with a margin of error.

PLLs are widely used for synchronization purposes in several communication and consumer domains, including radio transmission, clock recovery and deskewing, spread spectrum, clock jitter reduction, clock generation, and clock distribution. PLLs typically used in high-performance, high-speed systems are required to have low noise/jitter clock outputs, and low clock skew, among other requirements.

1.1 Past High-Performance PLL Trends

High-performance, high-speed systems demand components that exhibit close-to-ideal characteristics, such that precision is not compromised while ensuring that the systems themselves do not become overly complicated. In electronic systems, this approach has led to shifting all processing from the analog domain to the digital domain while the signal transmitting and receiving are performed in the analog domain. This shift means that high-performance systems generally have both analog and digital blocks as well as additional blocks to perform the analog-to-digital (A/D) and digital-to-analog (D/A) signal conversions. All the digital, A/D, and D/A blocks also require high-precision clocking that involves high-performance clock generation and distribution circuitry; typically, this circuitry is a high-performance PLL. In the past, as a result of silicon process and chip design limitations, high-performance PLLs have generally relied on off-chip, high-Q mechanical devices such as crystal oscillators to complete the feedback system in order to ensure high-quality outputs. Technology has not advanced enough to ensure a high-Q oscillator on silicon that integrates successfully with the rest of the PLL components.

Crystal oscillators are not without drawbacks, however. Traditional, fundamental-mode crystals are very difficult to cut, and are therefore very expensive at frequencies beyond 200 MHz. Moreover, long frequency lines produce undesirable effects (such as electromagnetic interference, or EMI); to reduce these effects, multiple crystal oscillators are required at the point of clocking, greatly increasing system costs. For applications that require a variety of high frequencies, the use of multiple programmable-frequency synthesizers or fixed-frequency crystal oscillators also drives up the system cost.

1.2 Recent High-Performance PLL Trends

Recent advances in silicon process technology have made possible the design of an on-chip, high-Q, inductor-based oscillator that costs just a fraction of a similar crystal-based oscillator. The performance difference between these two types of devices is negligible and insignificant for most applications. This new trend on silicon also allows for all PLL operations to be done on-chip without the need for external components. Moreover, the use of a programming on-chip oscillator and dividers enables the PLL to track a wide range of frequencies that are useful for many test applications.

TI's CDCE421 is an example of this type of advanced device. The CDCE421 PLL components are all on-chip, requiring no additional off-chip components for device operation. The CDCE421 also includes a programming interface, enabling the PLL to both cover wide frequency ranges at its output and operate at a wide range of PLL bandwidths, while ensuring very low noise and jitter over the entire device operating range.

2 Functional Description

The CDCE421 is a high-performance, low-jitter clock synchronizer and jitter cleaner that synchronizes the reference clock to its on-chip, voltage-controlled oscillator (VCO) frequency. The input reference clock can be provided from either a crystal or a rail-to-rail LVCMOS buffer. The programmable prescaler, output divider, and choice of either of the two on-chip VCOs combine give a high flexibility to the frequency ratio of the reference clock to the output clock that operates from 10 MHz to 1.2 GHz. Through the selection of the programmable loop filter components and the charge pump current, the PLL bandwidth can be

adjusted to meet different application requirements. Device programming is done through TI's one-pin programming, a proprietary interface protocol that can be configured and programmed via a single input pin to the device, using an onboard microcontroller. The device also comes with an on-chip EEPROM that allows for saving default start-up settings. The CDCE421 is characterized for operation from 3.0 V to 3.6 V and is specified from –40°C to +85°C.

2.1 Clock Synthesizer

As shown in Figure 1, the CDCE421 PLL consists of an internal phase frequency detector, a charge pump, an active loop filter, two LC-oscillator-based VCOs, prescalers, and feedback dividers. Through the PLL operation, the VCO output synchronizes with the input reference clock. The VCO output is then sent through the programmable output dividers and is made available in either a differential LVPECL or LVDS output that is also synchronized in phase and frequency with the input reference clock.

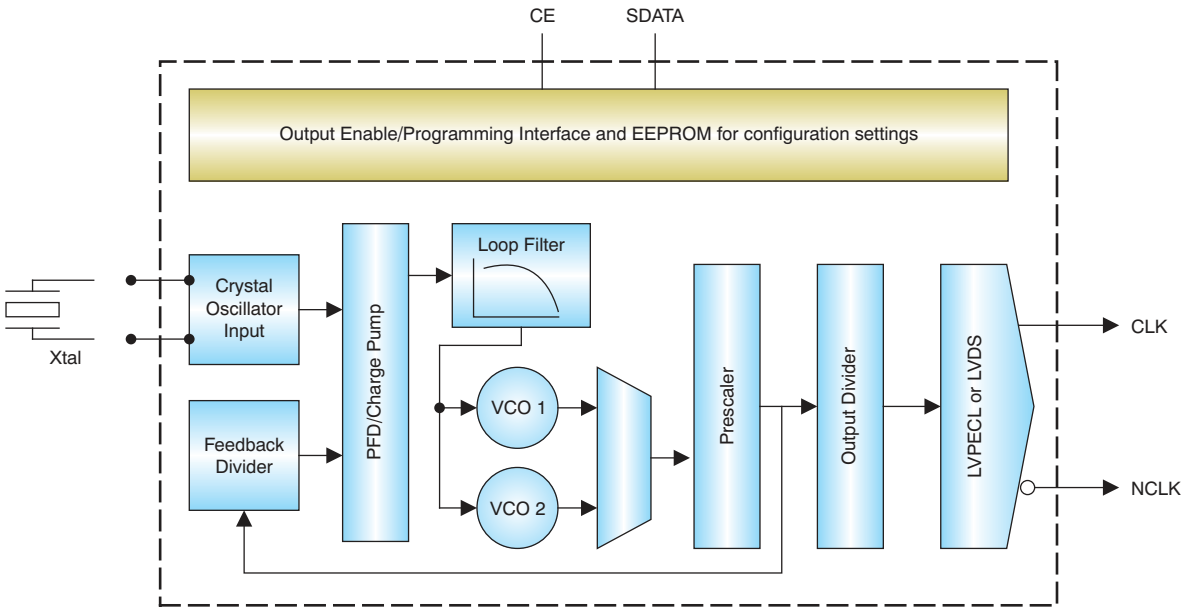

Figure 1. CDCE421 Block Diagram

2.2 Frequency Multiplication and Division

Through the proprietary one-pin programming interface, the prescalers can be set from 2 to 5; either VCO can be chosen (***note:*** for inputs between 27 MHz and 34 MHz, VCO 1 is recommended; use VCO 2 for inputs between 31 MHz and 39 MHz); and the output dividers can be set from 1, 2, 4 ,8, 16, or 32. Depending on whether the prescaler is odd or even, the selected VCO center frequency is either 60 times or 64 times the input reference frequency, respectively. The feedback dividers are then automatically chosen in such a way that the phase frequency detector sees the same frequencies at both the input and the output of the feedback divider. The output type is chosen to be either LVPECL or LVDS; the frequency is fixed by the chosen output divider setting.

3 CDCE421 Frequency Synthesis

This section provides some insight on choosing the input frequency, divider, and VCO settings needed to obtain a particular output frequency. It also guides on locating a common input frequency needed to generate multiple output frequencies using multiple CDCE421 devices.

3.1 Single Frequency Synthesis Example

Assume a typical application, where a 448-MHz output clock is desired and must be phase-locked to a back-plane input reference clock. The goal of this example is to identify the input reference frequency to lock to and the related PLL settings necessary to derive the output frequency from the input frequency. The following steps achieve these results.

Step 1. From Figure 1, it can be inferred that the relationship between the output frequency and the input frequency is represented by Equation 1:

$$F_{IN} = \left(\frac{\text{Output Divider}}{\text{Feedback Divider}}\right) \times F_{OUT} \quad (1)$$

Step 2. These parameters must be considered:

- the output divider can be set from 1, 2, 4, 8, 16 or 32
- the output signal type can be chosen as LVPECL or LVDS
- the on-chip VCO_1 tuning range is from 1.75 GHz to 2.1 GHz
- the on-chip VCO_2 tuning range is from 2 GHz to 2.3 GHz
- the prescaler divider can be chosen from 2, 3, 4 or 5.

The feedback divider is automatically chosen by the device depending on the user-selected prescale divider such that the VCO frequency is 60 times the input frequency for odd prescaler dividers, and the VCO frequency is 64 times the input frequency for even prescaler dividers. So, for a prescale divider of 2, the feedback divider is 32; for a prescale factor of 3, the feedback divider is 20; for a prescale divider of 4, the feedback divider is 16; and for a prescale factor of 5, the feedback divider is 12.

Step 3. For any desired output, we must establish a VCO frequency according to the following relationship:
F_{VCO} = Prescale Divider $\times$ Output Divider $\times F_{OUT}$
Such that the VCO frequency always lies between 1.75 GHz and 2.3 GHz for the chosen output and prescale dividers.

For the example of a 448-MHz output frequency, it can easily be shown that for all possible combinations of prescale and output dividers, the combinations of:

- *[prescale divider = 2, output divider = 2]*
- *[prescale divider = 4, output divider = 1]* and
- *[prescale divider = 5, output divider = 1]*

generate VCO frequencies within the allowable range. Respectively, the VCO frequencies for these combinations are 1.792 GHz, 1.792 GHz, and 2.24 GHz. Therefore, the correct VCO for each of these three combinations are VCO_1, VCO_1, and VCO_2 (see earlier note).

Step 4. Recall from Step 2 that the ratio of VCO frequency to input frequency is 60 (if the prescale divider is odd) or 64 (if the prescale divider is even). For this current example, the three possible combinations result in a ratio of VCO frequency to input frequency of 64, 64, and 60, respectively. Therefore, from this calculated ratio, the required input frequency to generate a 448-MHz output frequency is calculated for the three combinations as 28 MHz, 28 MHz, and 37.333 MHz, respectively.

Figure 2 is a block diagram showing the values of the programmable components of the CDCE421 required for each of the three combinations in order to generate a 448-MHz output frequency.

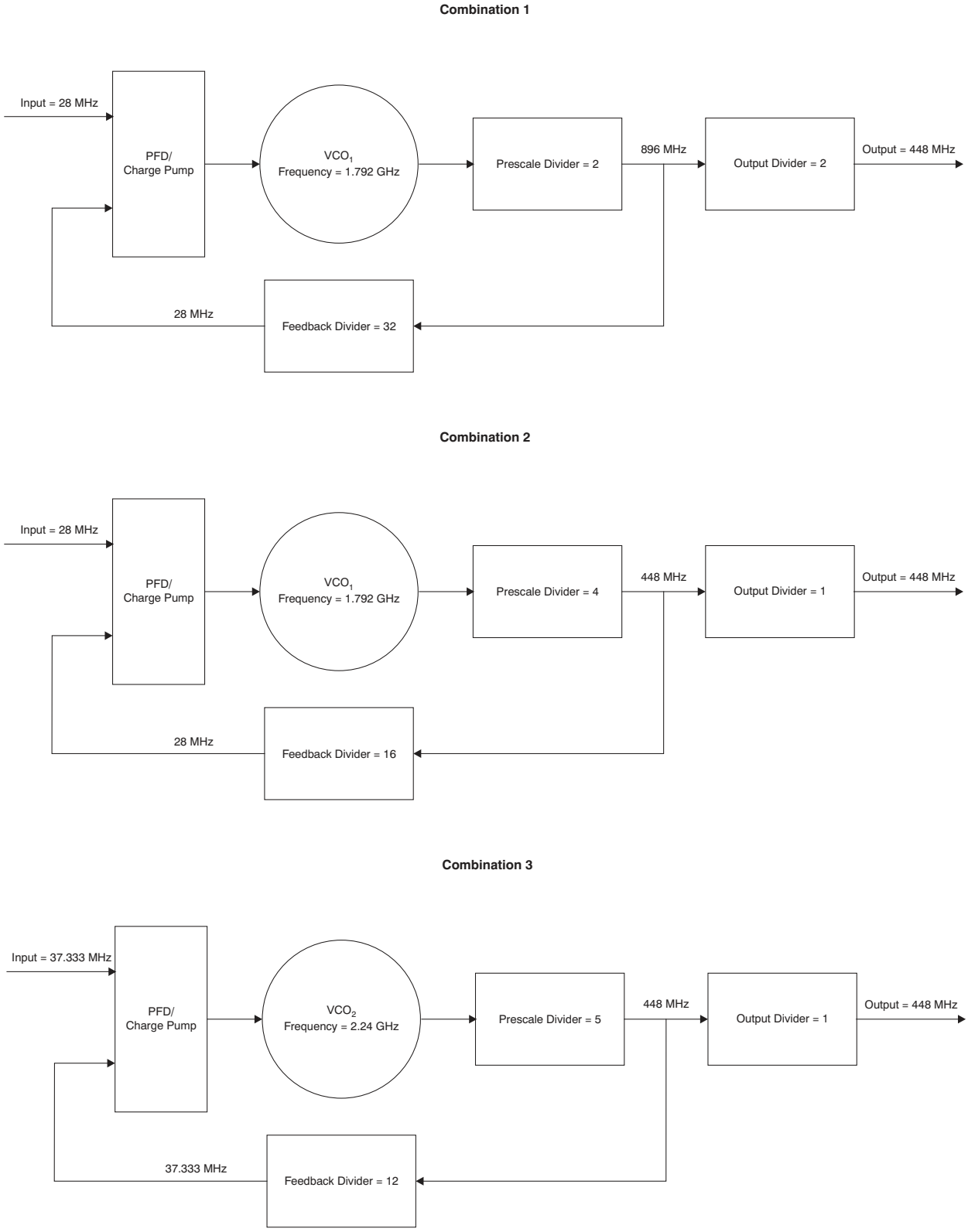

Figure 2. CDCE421 Programming Settings and Required Input Frequencies to Generate a 448-MHz Output Frequency

3.2 Multiple Frequency Synthesis Example

Assume a typical application, where 1066.56-MHz and 83.33-MHz output clocks are desired and must be phase-locked to a single back-plane input reference clock. The goal of this example is to identify the input reference frequency to lock to and the related PLL settings needed to derive the two output frequencies from the common input frequency. Follow these steps to solve this example.

Step 1. From Figure 1, it can be inferred that the relationship between the output frequency and the input frequency is given by Equation 2:

$$F_{IN} = \left(\frac{\text{Output Divider}}{\text{Feedback Divider}}\right) \times F_{OUT} \quad (2)$$

Step 2. These parameters must be considered:

- the output divider can be set from 1, 2, 4, 8, 16 or 32
- the output signal type can be chosen as LVPECL or LVDS
- the on-chip VCO_1 tuning range is from 1.75 GHz to 2.1 GHz
- the on-chip VCO_2 tuning range is from 2 GHz to 2.3 GHz
- the prescaler divider can be chosen from 2, 3, 4 or 5.

The feedback divider is automatically chosen by the device depending on the user-selected prescale divider such that the VCO frequency is 60 times the input frequency for odd prescaler dividers, and the VCO frequency is 64 times the input frequency for even prescaler dividers. So, for a prescale divider of 2, the feedback divider is 32; for a prescale factor of 3, the feedback divider is 20; for a prescale divider of 4, the feedback divider is 16; and for a prescale factor of 5, the feedback divider is 12.

Step 3. Given two desired output frequencies and using as many CDCE421 devices as the number of required output frequencies, the next step is to establish a common input frequency for different feedback and output divider settings, as shown in Equation 3, such that the common input frequency always lies between 27 MHz and 38.5 MHz for the two sets of chosen output and feedback dividers.

$$F_{IN} = \left(\frac{\text{Output Divider}_1}{\text{Feedback Divider}_1}\right) \times F_{OUT1}$$

$$F_{IN} = \left(\frac{\text{Output Divider}_2}{\text{Feedback Divider}_2}\right) \times F_{OUT2} \quad (3)$$

For this example of 100-MHz and 83.33-MHz outputs, it can easily be shown that for all sets of possible combinations of feedback and output dividers, the set of combinations of:

- *[output divider = 1, feedback divider = 32]* and
- *[output divider = 8, feedback divider = 20]*

result in a common input frequency of 33.33 GHz for the two CDCE421 devices that is within the allowable range.

Step 4. Recall from Step 2 that the feedback divider is 32 for a prescale divider of 2, 20 for a prescale factor of 3, 16 for a prescale divider of 4, and 12 for a prescale factor of 5. For the current example, the combinations set the prescalers to (2, 3). Additionally, the ratio of VCO frequency to input frequency is set as (64, 60) and the VCO frequency is set as (2 GHz, 2.133 GHz). It can be inferred that the VCO to be used is VCO_1 (see earlier note).

Figure 3 illustrates a block diagram outlining the values of the programmable components of the two CDCE421 devices required for the set of combinations necessary to generate the 1066.56-MHz and 83.33-MHz outputs.

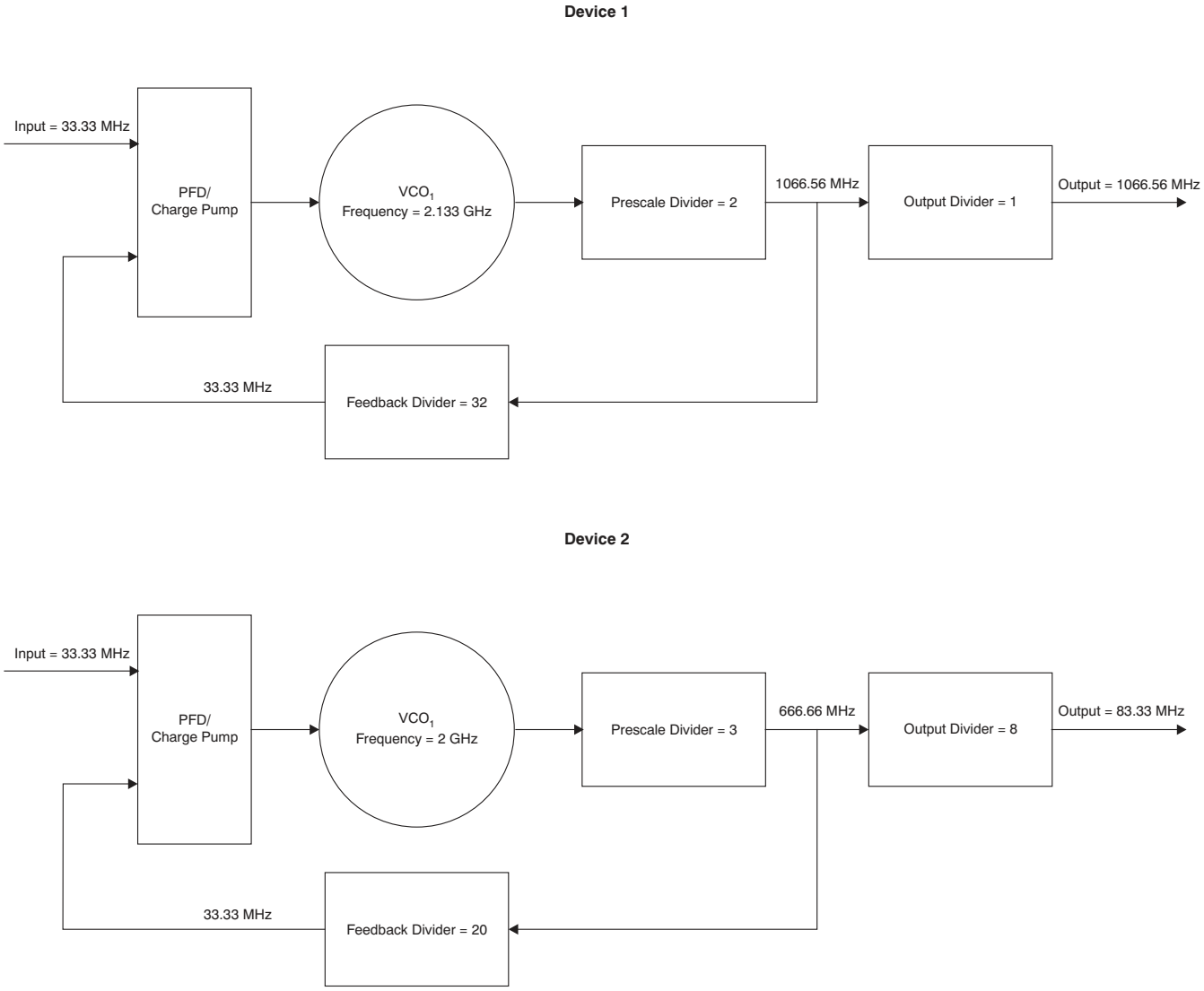

Figure 3. Dual CDCE421 Device Programming Settings and Required Input Frequencies to Generate 1066.56-MHz and 83.33-MHz Outputs

4 CDCE421 Default Configuration

The on-chip EEPROM of the CDCE421 has been factory-programmed to the default settings of VCO_2, prescaler divider of 4, output divider of 8 and output signaling type of LVPECL. The default register settings are:

REG0[3:10] = 00111010, REG1[3:10] = 11111010, REG2[3:10] = 11000000, REG3[3:10] = 00011110, REG4[3:10] = 00000001, REG5[3:10] = 00000000.

Additionally, if there are any *on the fly* programming changes to the CDCE421 PLL settings, the ENCAL bit (Word 4, Bit 10 as explained in Page 10 of the CDCE421 datasheet) or the CE pin (Pin 1) should be toggled.

5 CDCE421 Startup Modes

If the EEPROM has been pre-configured, the CDCE421 can start up with its register values loaded from the EEPROM, and therefore proper operation of the PLL ensures output at the correct frequency. Startup time depends on the power supply ramp time. Once the supply voltage crosses a pre-determined threshold voltage (2.0 V to 2.7V), PLL auto-calibration initiates and sets the dividers and the VCO to the appropriate frequency. Auto-calibration can also be restarted by toggling the Chip Enable pin of the CDCE421 from high to low and back to high. As a result, if the reference input to the CDCE421 is unstable even after the power-supply voltage crosses the threshold voltage (and therefore, after auto-calibration is completed), the Chip Enable pin can be tied to the supply voltage through a low-pass filter—for example, a simple first-order RC circuit—with a fairly high time constant that would depend on the average time before which the reference input stabilizes. For example, for a 10-ms delay before input clock stabilizes, the RC circuit values are calculated as R = 10 kΩ and C = 1μF.

6 Input Crystal Selection Guidelines

The CDCE421 has an internal 8-pF load on the XIN1 pin. Therefore, if a crystal within the acceptable input range of the CDCE421 is chosen with a particular load capacitance rating, extra loading must be added on each of the crystal terminals connected to the XIN1 and XIN2 pins of the CDCE421 such that the crystal oscillates at the exact frequency at which it is rated. For example, given a 10-pF load rating for a chosen crystal, an additional 12-pF load can be added on the XIN1 pin, and an extra 20-pF load can be added on the XIN2 pin, such that (12 + 8) pF ‖ 20 pF = 10 pF.

Table 1 lists several recommended crystal vendors for working with the CDCE421.

Table 1. Recommended Crystal Manufacturers

Manufacturer	Part Number
KDS	SMD-49
Pletronics	SM13T
Quartzcom	UM-1 MJ

7 CDCE421 PLL Bandwidth Selection

Unlike other PLLs, the CDCE421 loop filter components and charge pump current are not fixed. It is possible to choose a loop bandwidth from 50 kHz to 400 kHz through the programming interface.

7.1 Loop Bandwidth

The PLL bandwidth depends on the loop filter, charge pump current, VCO gain, and PFD update frequency. In the CDCE421, the VCO gain, and the PFD update frequency are fixed quantities, as Figure 4 shows.

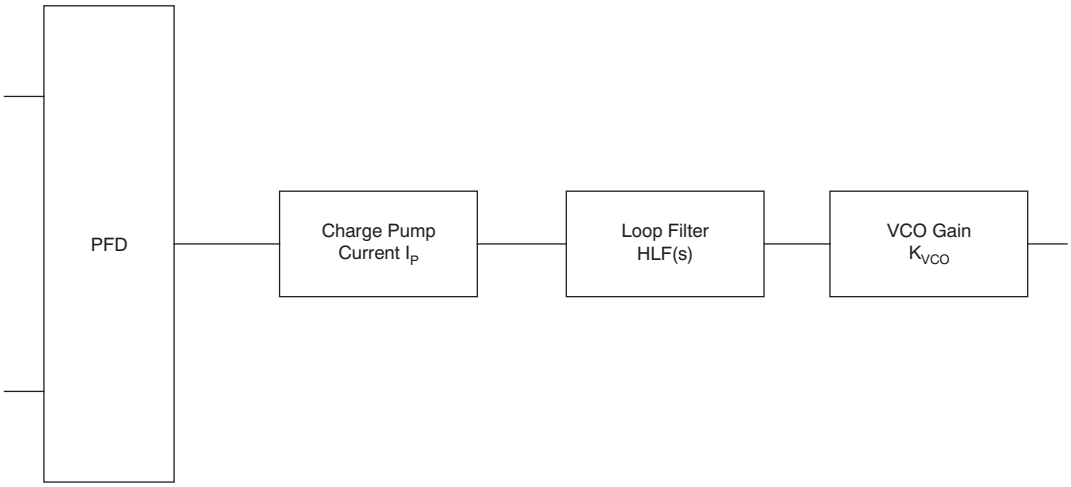

Figure 4. PLL Bandwidth Dependencies

7.2 Jitter Peaking

Around the loop bandwidth, the incoming jitter from the reference clock may be amplified. This phenomenon is called *jitter peaking*. For some applications, jitter peaking has an adverse effect on jitter performance, if the jitter peaking occurs within the band of interest. If the jitter peaking occurs outside the band of interest, applications generally do not see any unusual effects. In any case, limit the jitter peaking to within 10 dB to prevent the loop from becoming unstable. Figure 5 shows an example of a PLL phase response with jitter peaking of 2 dB.

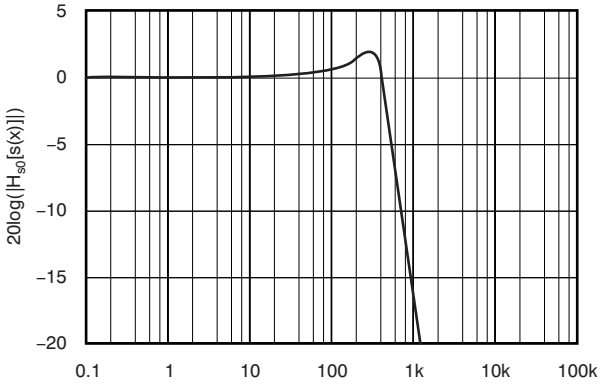

Figure 5. Jitter Peaking Around PLL Bandwidth

7.3 Phase Margin

Phase margin is important for PLL stability, and influences the PLL lock time. The rate at which the PLL output settles to its final value depends on the PLL phase margin. As a rule of thumb, no less than a 30-degree phase margin is recommended for a stable clock operation.

8 Changing the CDCE421 On-Chip Loop Filter

The CDCE421 has an on-chip active loop filter that has a structure similar to that illustrated in Figure 6. In Figure 6, R_2 and C_2 generate a zero. R_1 (not shown) and C_1 generate the first pole while R_3 and C_3 generate the second pole.

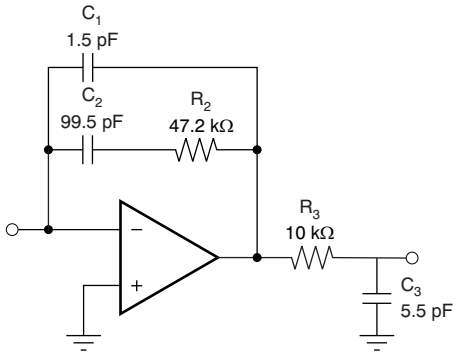

Figure 6. CDCE421 On-Chip Active Loop Filter

Depending on the target application for the CDCE421, the PLL bandwidth can be reduced by adjusting the loop filter components and charge pump current settings separately so that the resulting jitter peaking appears outside a band of interest.

9 Output Termination

The CDCE421 is a 3.3-V clock driver that has an option of these differential output types: LVDS or LVPECL.

9.1 LVPECL Termination

The CDCE421 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure proper device operation and to minimize signal integrity. The proper termination for LVPECL is 50 Ω to (V_{CC} – 2 V), but this dc voltage is not readily available on a printed circuit board (PCB). Either a direct termination or terminations for ac coupling can be used to terminate the LVPECL outputs. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage of the driver and the receiver differs, ac coupling is required.

9.1.1 Direct-Coupled LVPECL Termination

In order to eliminate the necessity of having a (V_{CC} – 2 V) supply on the board, a Thevenin-equivalent network composed of two resistors with a 3.3-V supply replaces the 50 Ω to (V_{CC} – 2 V), ensuring proper biasing and termination. Figure 7 shows a direct termination circuit.

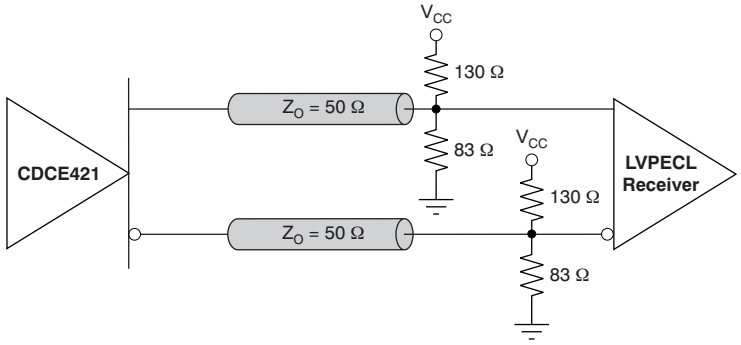

Figure 7. DC Termination Circuit

9.1.2 AC-Coupled LVPECL Termination

If ac-coupled termination is used, the input and output stages must be biased properly. The 150-Ω resistor near the CDCE421 ensures proper output biasing. Figure 8 shows an ac-coupled termination circuit.

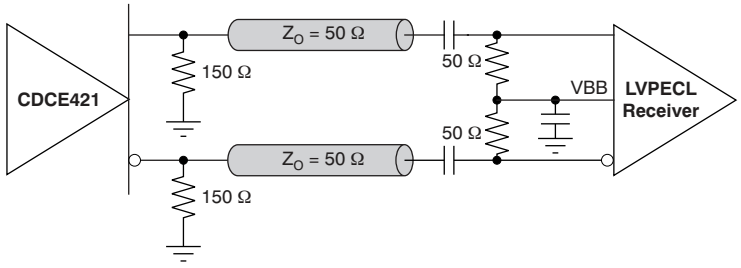

Figure 8. AC-Coupled Termination Circuit

9.2 LVDS Termination

The CDCE421 has onboard 100-Ω termination resistors between the two LVDS outputs. Therefore, no additional biasing is needed, but termination is required to minimize signal integrity. The proper termination for signal integrity over two 50-Ω lines is a 100-Ω resistor between the outputs on the receiver end. Either a direct termination or terminations for ac-coupling can be used to terminate the LVDS outputs. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage of driver and receiver is different, ac-coupling is required.

9.2.1 Direct-Coupled LVDS Termination

Figure 9 shows a termination circuit for the direct termination of LVDS outputs for an LVDS receiver with onboard 100-Ω termination resistors between the outputs.

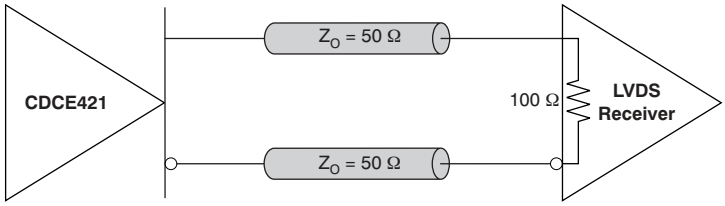

Figure 9. DC Termination Circuit

9.2.2 AC-Coupled LVDS Termination

Figure 10 shows a termination circuit for the ac-coupled termination of LVDS outputs for an LVDS receiver with onboard 100-Ω termination resistors between the outputs.

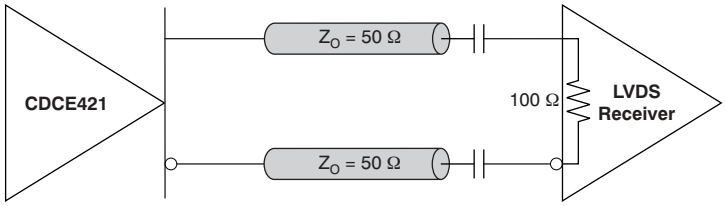

Figure 10. AC-Coupled Termination Circuit

10 Input Termination

The CDCE421 is a 3.3-V clock driver two input type options: a crystal or 3.3-V LVCMOS. The device has internal biasing circuitry for both input types.

10.1 Crystal Input

For a crystal input, the crystal should be direct-coupled between the XIN 1 and XIN 2 pins of the CDCE421, as shown in Figure 11.

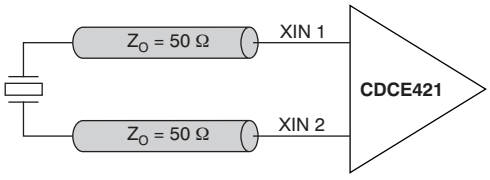

Figure 11. Direct-Coupled Crystal Input Circuit

10.2 LVCMOS Input

For driving the CDCE421 with a 3.3-V LVCMOS input, it should be ac-coupled to the XIN 1 pin of the CDCE421, as shown in Figure 12.

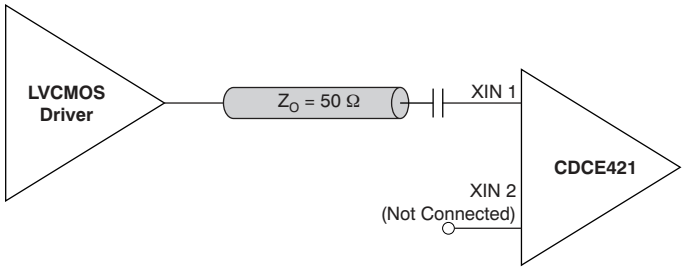

Figure 12. AC-Coupled LVCMOS Input Circuit

11 Power-Supply Decoupling

PLL-based frequency synthesizers are very sensitive to power-supply noise that can dramatically increase PLL jitter. This effect is especially true for analog-based PLLs. Consequently, it is essential to reduce noise from the system power supply, especially when jitter and phase noise are very critical to applications. A PLL will have attenuated jitter as a result of power-supply noise at frequencies beyond the PLL bandwidth because of attenuation by the loop response.

Filter capacitors are used to eliminate low-frequency noise from the power supply, whereas the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against any induced fluctuations. Inserting a ferrite bead between the board power supply and the chip power supply isolates the high-frequency switching noise generated by the clock driver, preventing the noise from leaking into the board supply. Choosing an appropriate ferrite bead with low dc resistance is important because it is imperative to maintain a voltage at the power-supply pin of the CDCE421 that is over the required minimum operating voltage. At dc, the ferrite bead has a voltage drop across itself and the maximum drop depends on its maximum dc resistance and the maximum dc current that the CDCE421 draws from the 3.3-V power supply.

For proper operation, the CDCE421 requires a minimum power-supply voltage of 3 V and draws a maximum supply current of 100 mA. Assuming a 3.3-V board power supply, the ferrite bead maximum dc resistance can be 3 Ω. Figure 13 shows a recommended option for decoupling the power supply.

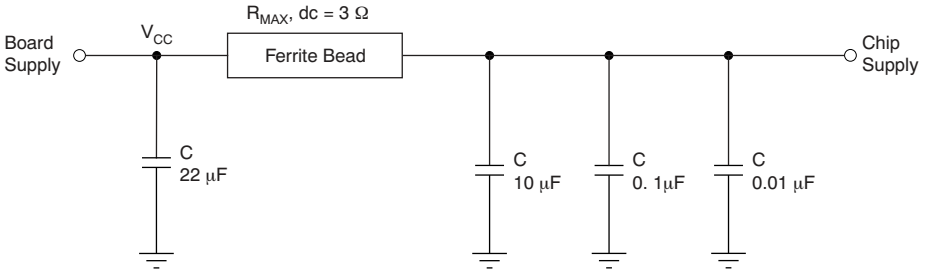

Figure 13. Power-Supply Decoupling

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