

**14-Lead Dual-In-Line  
Plastic Package  
"E"-Suffix Type**

## 1-GHz Prescaler

For Industrial Applications

**Features:**

- Typical broadband operation - dc to 1 GHz
- High sensitivity
- Standard T<sup>L</sup>L or ECL power supply
- Dual-mode operation - VHF/UHF (÷ 64/ ÷ 256)
- Complementary ECL outputs
- Independent VHF and UHF input terminals

The RCA-CA3179E is an integrated-circuit prescaler intended for use in communications and instrumentation systems. It performs division by 256 in the uhf mode and division by 64 in the vhf mode.

The mode of operation is selected by means of the bandswitch and the separate uhf and vhf input terminals provided. Either single- or double-ended inputs can be applied. These inputs are normally ac coupled, but dc coupling can be used if the specified bias levels are maintained. The output is a complementary emitter-coupled stage capable of driving a 33-pF or equivalent load. The harmonic output is reduced above 40 MHz by limiting output-signal rise and fall times and by maintaining a balanced load.

In the uhf mode, which is activated by applying a high level (logical 1) to the bandswitch input terminal, all eight divider stages are operative, resulting in division by 256. In the vhf mode, activated by a low level (logical 0) at the vhf input terminal, two divider stages are bypassed, resulting in division by 64. An internal amplifier/multiplexer provides this control while isolating both inputs, amplifying the input signal, and improving sensitivity.

The CA3179E is supplied in the 14-lead dual-in-line plastic package.

**Applications:**

- Digital frequency synthesizers for:  
VHF/UHF receivers  
Satellite communications  
Instrumentation
- High-frequency divider for:  
UHF frequency counters  
UHF timers  
High-speed computers  
Frequency standards  
SHF second IF local-oscillator injection  
PCM communications  
Satellite communications  
Radar ranging systems
- High-frequency up-converters

**Table of Absolute-Maximum Ratings**

Term. No.	Min. Volts	Max. Volts	Max. I <sub>IN</sub> (mA)	Max. I <sub>OUT</sub> (mA)
1 & 2*	0	5.5	110	0
3	-0.3	20	1	1
4 & 5	—	—	0.1	10
9, 10, 13, 14 <sup>▲</sup>	—	4	0.1	1

\*Terms. 1 & 2 tied together.

▲ Maximum if drive = 500 mVRMS.

Terms. 7 & 8 are system ground and tied together.

Terms. 6, 11, 12 = no connection.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY VOLTAGE .....	5.5 V
DC BANDSWITCH VOLTAGE .....	20 V
RMS INPUT VOLTAGE .....	0.5 V
<b>DEVICE DISSIPATION:</b>	
UP TO $T_A = 70^\circ\text{C}$ .....	700 mW
ABOVE $T_A = 70^\circ\text{C}$ .....	derate linearly at 11.1 mW/ $^\circ\text{C}$
<b>AMBIENT TEMPERATURE RANGE:</b>	
OPERATING .....	0 to 85 $^\circ\text{C}$
STORAGE .....	-65 to +150 $^\circ\text{C}$
<b>LEAD TEMPERATURE (DURING SOLDERING):</b>	
AT DISTANCE 1/16 $\pm$ 1/32 INCH (1.59 $\pm$ 0.79 MM)	
FROM CASE FOR 10 SECONDS MAX. ....	+285 $^\circ\text{C}$

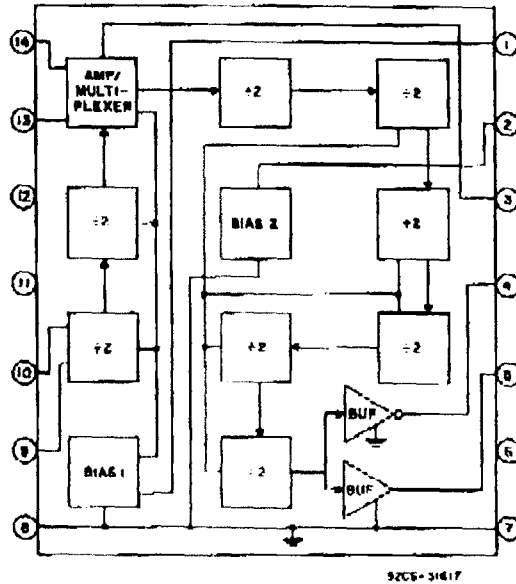


Fig. 1 - CA3179 block diagram.

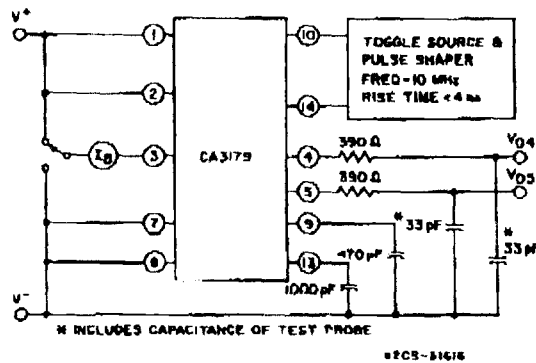


Fig. 2 - DC characteristics test circuit.

**ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$**

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		Min.	Typ.	Max.		
<i>Static (See Fig. 2)</i>						
Supply Current, $I^+$	Terms. 1 & 2	30	65	100	mA	
Bandswitch Voltage:	Term. 3	Low, $V_{BL}$	2.4	—	V	
		High, $V_{BH}$	—	0.8		
Bandswitch Current:	$V_3 = 0\text{ V}$	Low, $I_{BL}$	-1	—	mA	
		High, $I_{BH}$	—	0.5		
<i>Dynamic (See Fig. 3)</i>						
Sine Wave Sensitivity (Single-ended)	$f_{IN} = 450\text{ to }950\text{ MHz}$ $V_3 = 5\text{ V}$	0	30	80	mVRMS	
	$f_{IN} = 80\text{ to }450\text{ MHz}$ $V_3 = 5\text{ V}$	—	50	160		
	$f_{IN} = 90\text{ to }275\text{ MHz}$ $V_3 = 0\text{ V}$	—	5	40		
Output Voltage:	Term. 4 or 5	High, $V_{OH}$	—	4.2	V	
		Low, $V_{OL}$	—	3		
		Peak-to-Peak, $V_{OP-P}$	0.65	1.1	1.6	
Output Rise or Fall Time, $t_r, t_f$			40	70	110	ns
Internal Bias	Term. 13 or 14	$(V_{DD} - 1)$			V	
	Term. 9 or 10	$(V_{DD} - 2.7)$				
DC Input Resistance, $R_i$	Term. 13 to 14	2000			$\Omega$	
	Term. 9 to 10	1000				
Complex Input Impedance	Term. 9 to 10, $V_{IN} = 100\text{ mV}$ , $f_{IN} = 950\text{ MHz}$	20			$\Omega$	
	Term. 9 to 10, $V_{IN} = 100\text{ mV}$ , $f_{IN} = 450\text{ MHz}$	30 - j80				
	Term. 13 to 14, $V_{IN} = 100\text{ mV}$ , $f_{IN} = 275\text{ MHz}$	35 - j100				

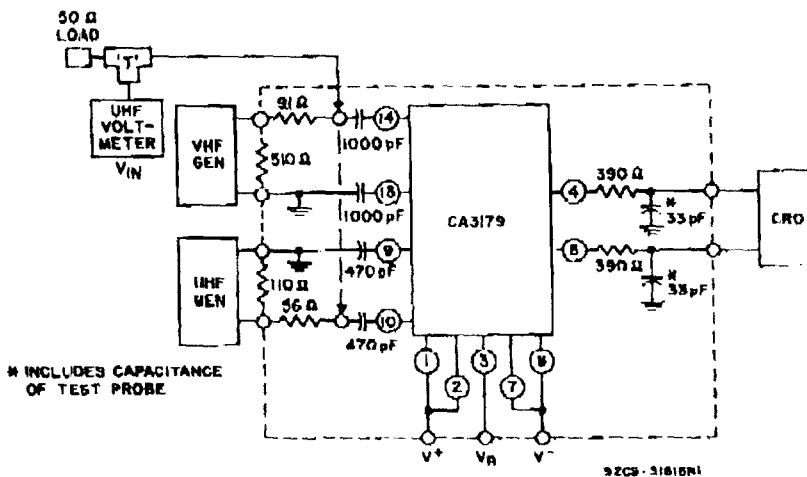


Fig. 3 - AC characteristics test circuit.

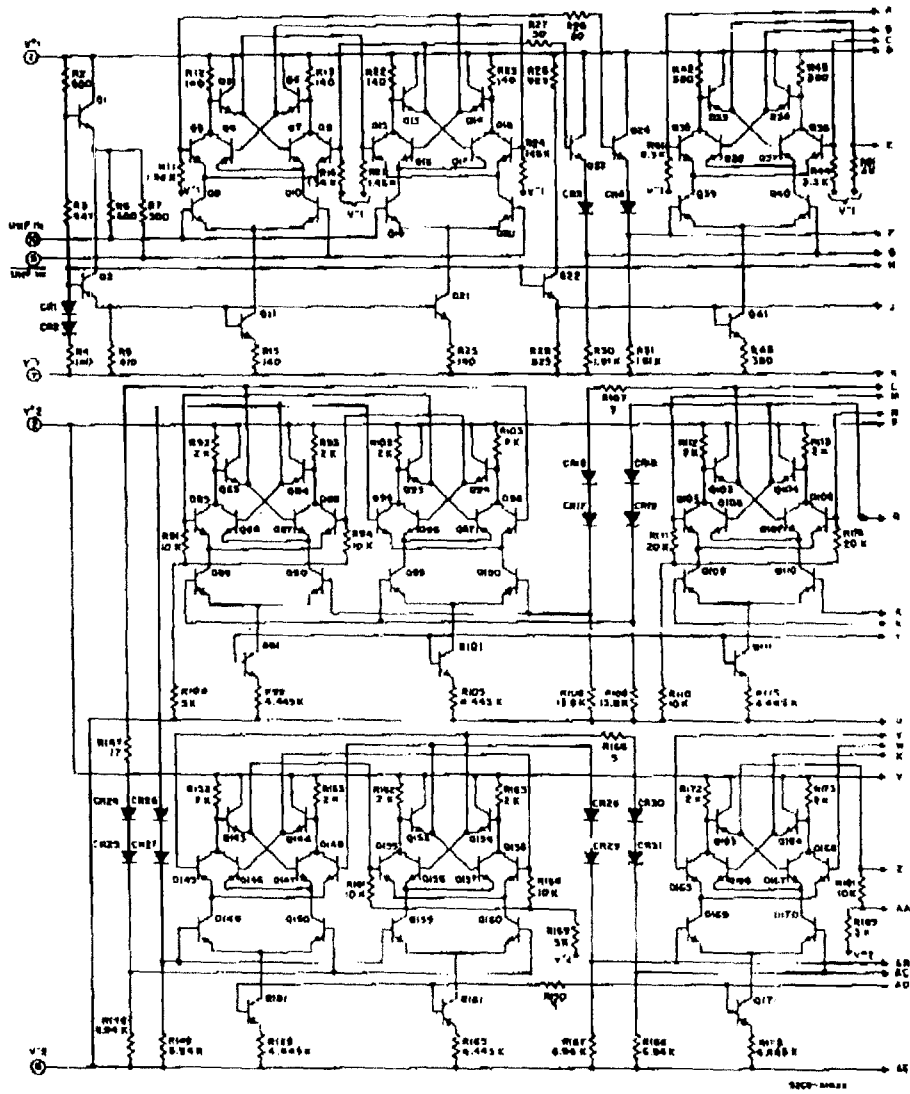


Fig. 4 - Schematic diagram (cont'd on next page).

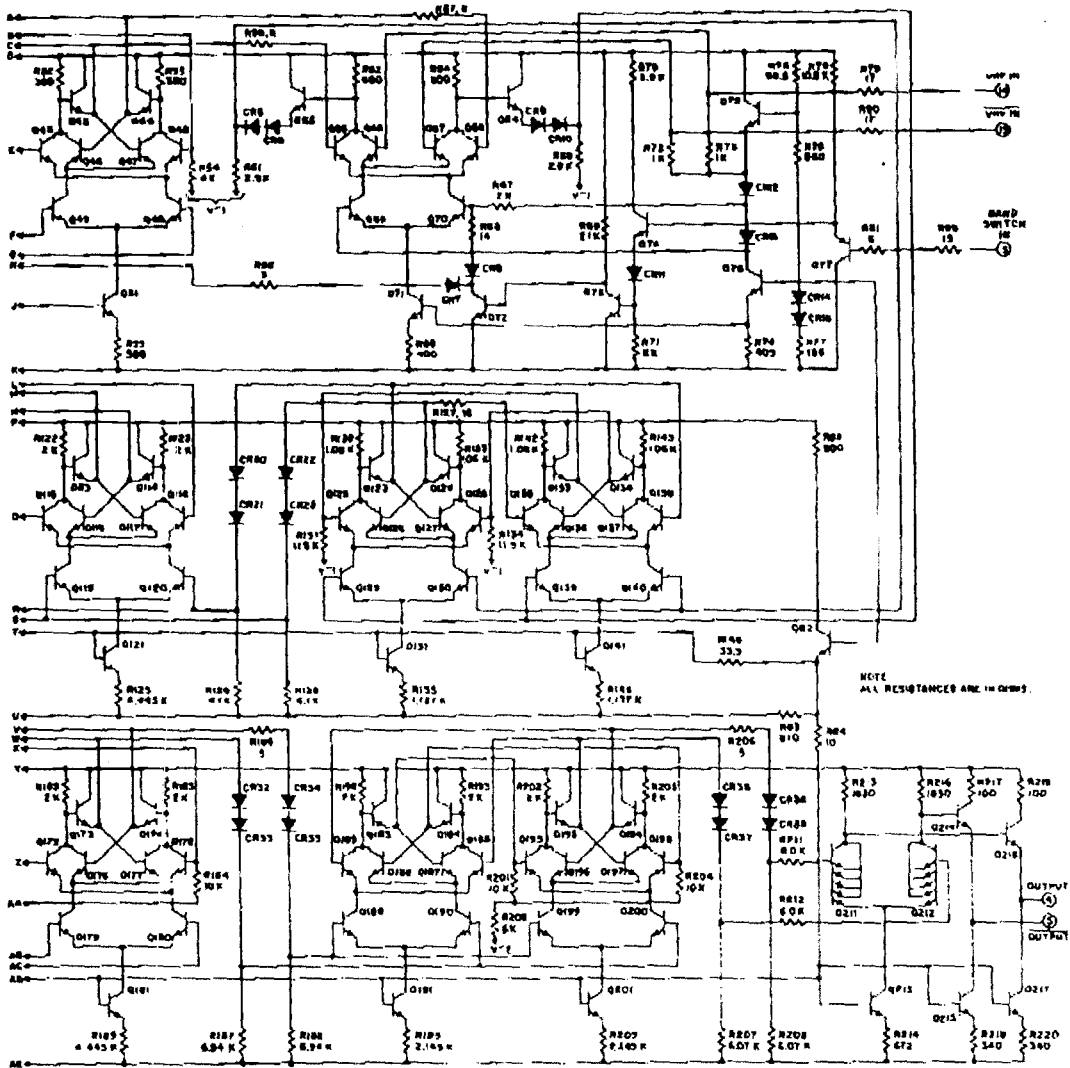


Fig. 4 - Schematic diagram (cont'd from previous page).

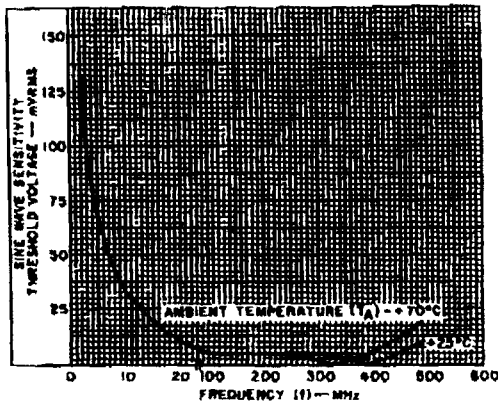


Fig. 5 - Typical threshold sensitivity in the +64 VHF mode.

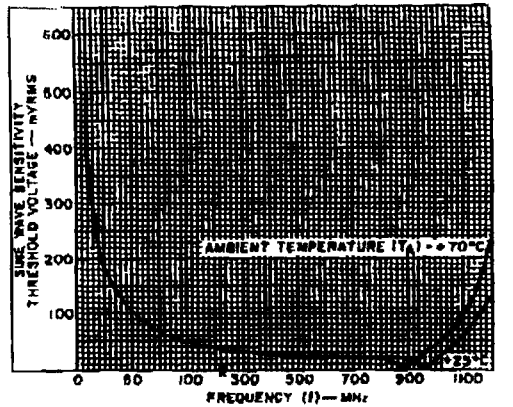


Fig. 6 - Typical threshold sensitivity in the +268 UHF mode.

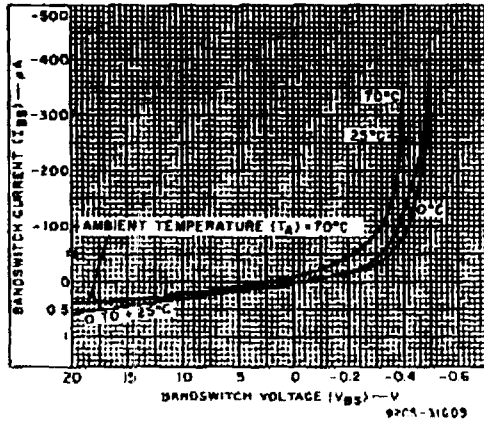


Fig. 7 - Typical bandswitch current as a function of bandswitch voltage and ambient temperature.

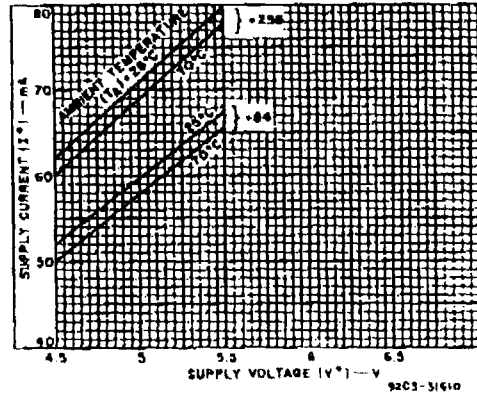


Fig. 8 - Supply current as a function of supply voltage and ambient temperature.

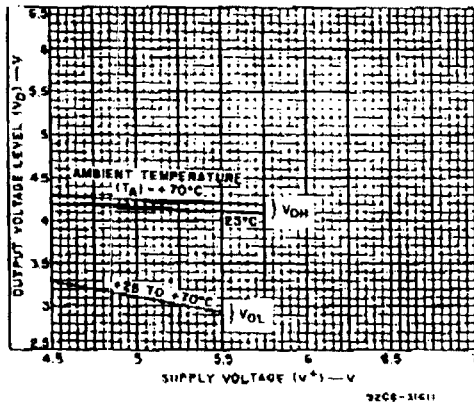
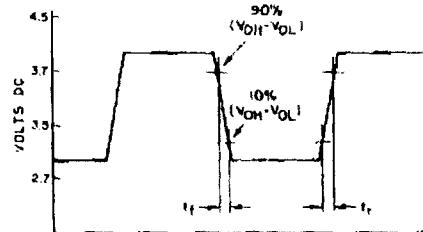


Fig. 9 - Typical output voltage level as a function of supply voltage and ambient temperature.



OUTPUT PULSE = 0.85 V<sub>D-P</sub> MIN., 1.6 V<sub>D-P</sub> MAX.  
t<sub>r, f</sub> = 40 ns MIN., 110 ns MAX.

Fig. 10 - Output pulse characteristics.

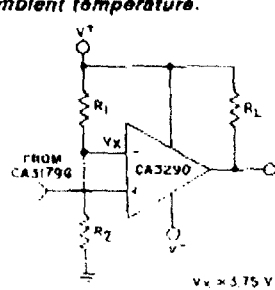


Fig. 11 - Typical bipolar interface circuit.

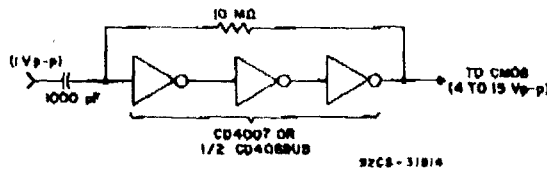
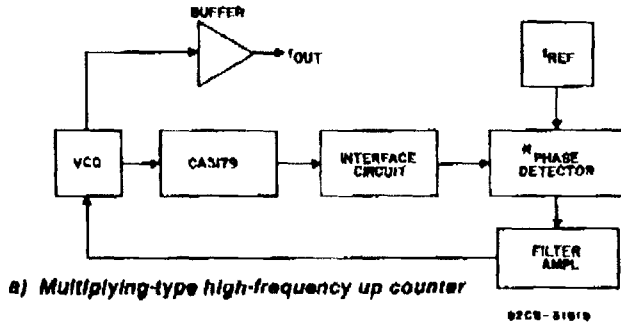
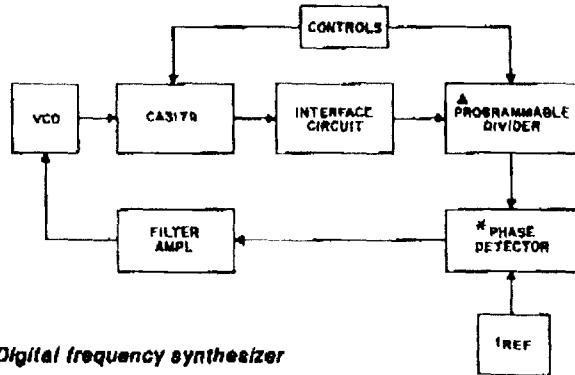


Fig. 12 - Typical CMOS interface circuit.



a) Multiplying-type high-frequency up counter

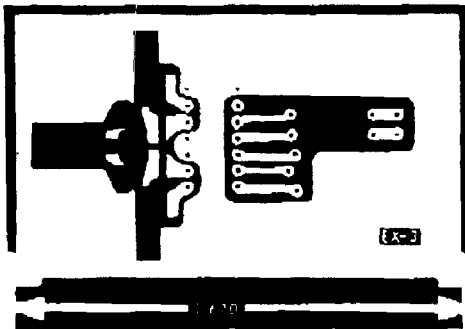
92CS-31819



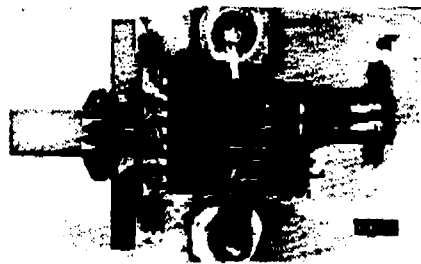
b) Digital frequency synthesizer

□ CD4046B, CD4020B, CD40709 OR EQUIVALENT  
 ▲ CD4018B, CD4029B, CD4059A, CD40102B, CD40103B OR EQUIVALENT  
 92CS-31620

Fig. 13 - Typical system configuration.



92CS-31624



92CS-31651

Fig. 14 - Printed-circuit board for the dynamic test circuit.

Fig. 15 - Printed-circuit board for the dynamic test circuit with components.

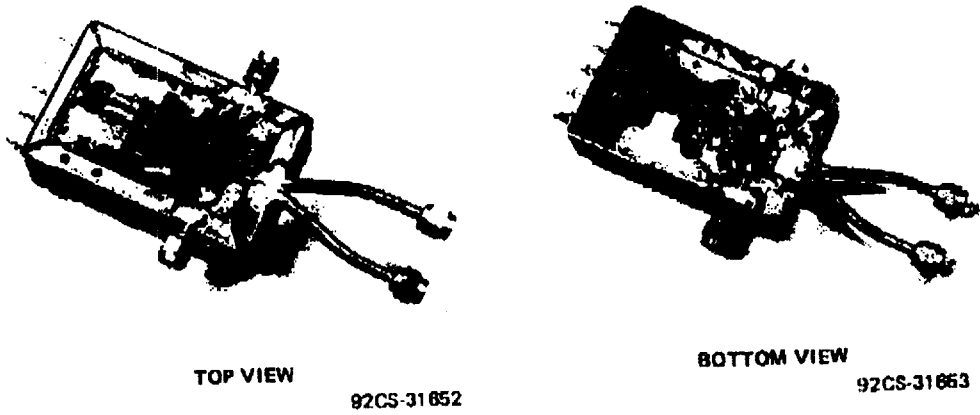


Fig. 16 - Dynamic test circuit fixture.

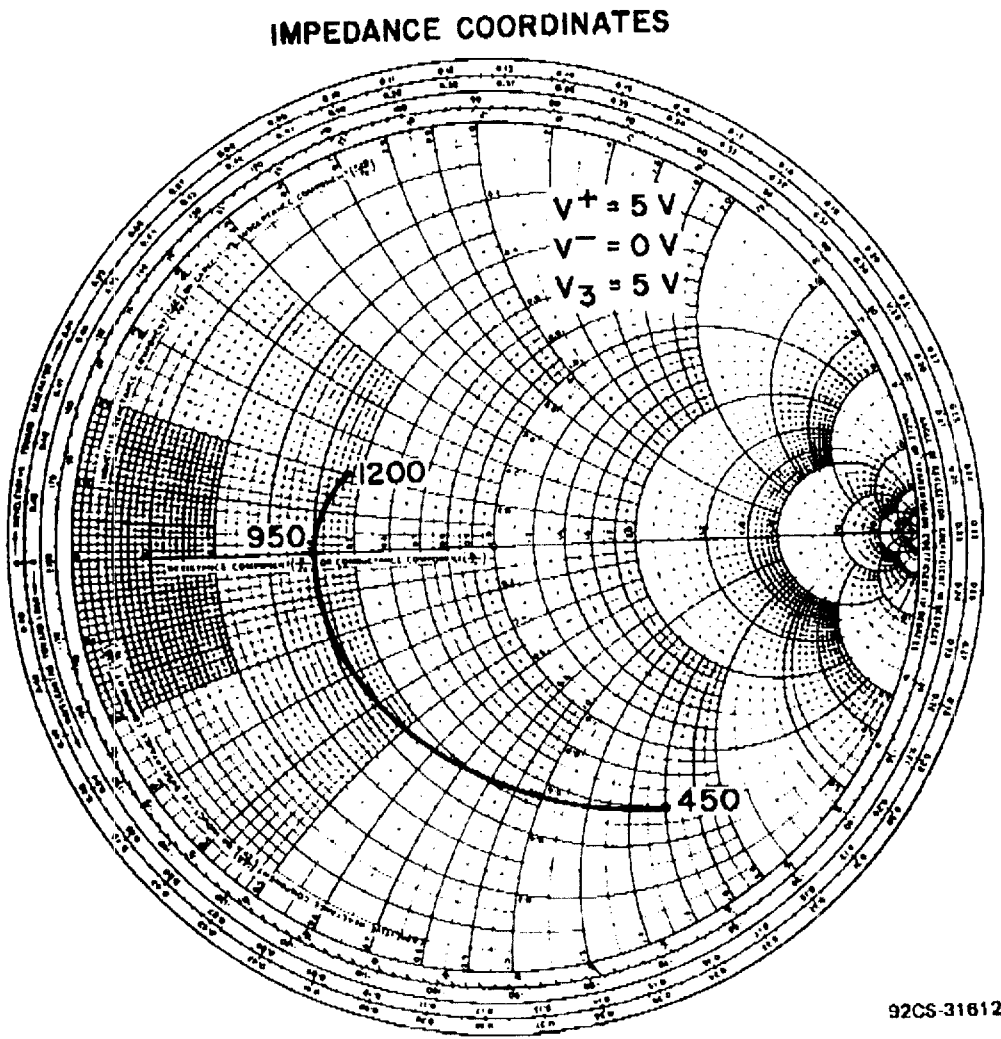


Fig. 17 - Impedance as a function of frequency.



High-frequency construction and design techniques must be followed if the operation of the CA3179 test circuit is to be stable and if the results of repeated tests are to be consistent. The dynamic test circuit is shown in Fig. 3, and a photo of the test fixture that houses it is shown in Fig. 16. Listed below are some precautionary construction considerations for the circuit and test fixture.

1. Supply the ground plane with frequent ground connections.
2. Use 50-Ω coaxial cable for input connections
3. Use a "dead bug" type socket to minimize lead lengths and reduce series inductances
4. Use input pads that reduce impedance mismatch at the generator-test and meter-test input interfaces
5. Use leadless ceramic disc capacitors wherever possible
6. Provide capacitor by-passing near active terminals where ac grounds are required

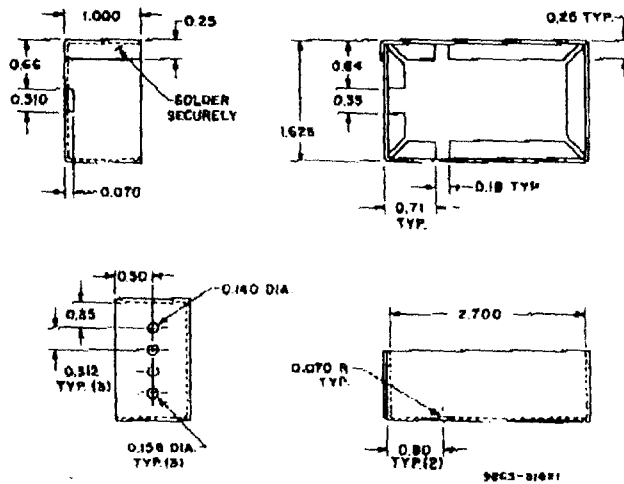
Specific applications may require changes in the procedures listed above. The socket, for instance, can be

eliminated by soldering the device directly to the p.c. board or by using individual board-mounted socket pins. Input and output interface connections and circuitry will also vary according to specific circuit requirements.

**Partial Parts List for the Dynamic Test Circuit and Fixture:**

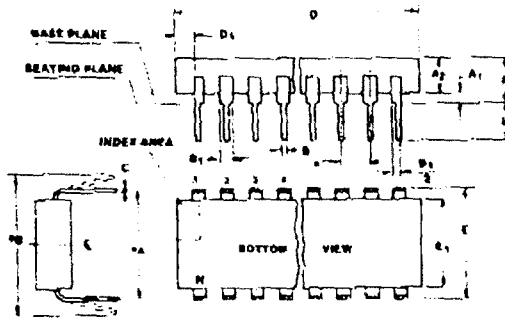
- 4 - Pasternac PE3493-6 SMA cable connectors and semi-rigid coaxial cable
- 1 - Chassis
- 1 - P.C. board
- 1 - 14-lead socket
- 2 - 1000-pF capacitors, Stettner Trush Inc. No. TEFIC-7
- 3 - 470-pF disc capacitors
- 3 - 1000-pF disc capacitors
- 2 - 33-pF feedthrough capacitors
- 3 - 1000-pF feedthrough capacitors
- 3 - Ferrite beads, 0.375 x 0.187 x 0.250
- 2 - Resistors, 390-Ω, 1/4-W, 2%
- 1 - Resistor, 56-Ω, 1/4-W, 5%
- 1 - Resistor, 110-Ω, 1/4-W, 5%
- 1 - Resistor, 9.1-Ω, 1/4-W, 5%
- 1 - Resistor, 510-Ω, 1/4-W, 5%

**Dimensions of Test Fixture**



DIMENSIONAL OUTLINE

E SUFFIX  
 14-Lead Dual-in-Line Plastic Package  
 JEDEC MS-001-AC



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A <sub>1</sub>	0.015	—	0.39	—	9
A <sub>2</sub>	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.566	
B <sub>1</sub>	0.045	0.070	1.16	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D <sub>1</sub>	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E <sub>1</sub>	0.240	0.290	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e <sub>A</sub>	0.300 BSC		7.62 BSC		9
e <sub>B</sub>	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	8
N	14		14		11

- Notes:
- M2CB-39901
- Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
  - Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
  - The dimension shown is for full leads. "Half" leads are optional at lead positions  $1, N, \frac{N}{2}, \frac{N}{2} + 1$ .
  - Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
  - E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
  - Dimension E<sub>1</sub> does not include mold flash or protrusions.
  - Package body and leads shall be symmetrical around center line shown in end view.
  - Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
  - This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e<sub>A</sub>.
  - e<sub>B</sub> is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
  - N is the maximum number of lead positions.
  - Dimension D<sub>1</sub> at the left end of the package must equal dimension D<sub>1</sub> at the right end of the package within 0.020 in. (0.76 mm).
  - For automatic insertion, any raised irregularity on the top surface (step, mess, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.