

## TLV6703 Micropower, 18-V Comparator With Integrated Reference

### 1 Features

- Wide supply voltage range: 1.8 V to 18 V
- Adjustable threshold: down to 400 mV
- High threshold accuracy:
  - 0.5% Max at 25°C
  - 1.0% Max over temperature
- Low quiescent current: 5.5  $\mu$ A (Typ)
- Open-drain output
- Internal hysteresis: 5.5 mV (Typ)
- Temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package: thin SOT-23-6
- WSON-6

### 2 Applications

- [Notebook PCs and tablets](#)
- [Smartphones](#)
- [Digital cameras](#)
- [Video game controllers](#)
- [Relays and circuit breakers](#)
- [Portable medical devices](#)
- [Door and window sensors](#)
- [Portable- and battery-powered products](#)

### 3 Description

The TLV6703 high voltage comparator operates over a 1.8-V to 18-V range. The TLV6703 has a high-accuracy comparator with an internal 400-mV reference and an open-drain output rated to 18 V for precision voltage detection. The monitored voltage can be set with the use of external resistors.

The OUT pin is driven low when the voltage at the SENSE pin drops below ( $V_{IT-}$ ), and goes high when the voltage returns above the respective threshold ( $V_{IT+}$ ). The comparator in the TLV6703 includes built-in hysteresis for filtering to reject brief glitches, thereby ensuring stable output operation without false triggering.

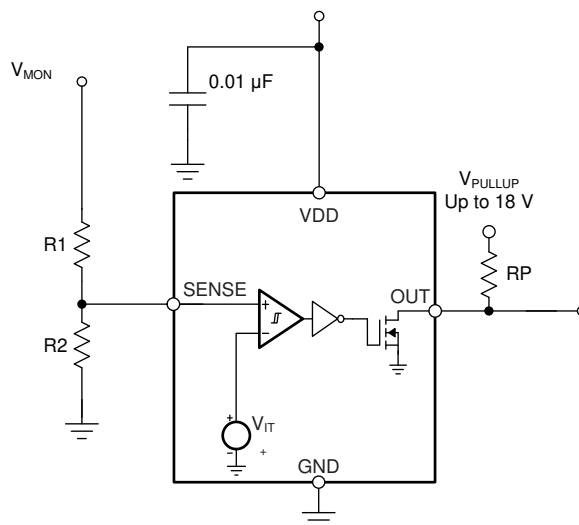
The TLV6703 is available in a Thin SOT-23-6 package and a leadless WSON-6; all package variants are specified over the junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

#### Device Information <sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV6703	SOT-23 (6)	2.90 mm $\times$ 1.60 mm
	WSON (6)	1.50 mm $\times$ 1.50 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

#### Simplified Block Diagram



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## 4 Revision History

<b>Changes from Revision A (April 2018) to Revision B</b>	<b>Page</b>
• Added WSON-6 package .....	<b>1</b>

<b>Changes from Original (Jan 2018) to Revision A</b>	<b>Page</b>
• Changed Advance Information to Production Data .....	<b>1</b>

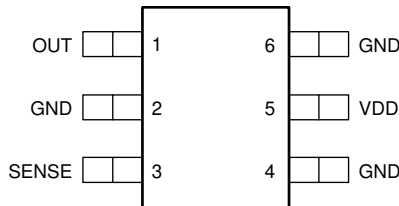
## 5 Device Comparison Table

**Table 1. TLV67xx Integrated Comparator Family**

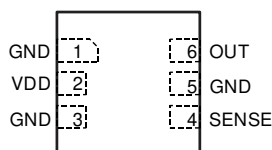
PART NUMBER	CONFIGURATION	OPERATING VOLTAGE RANGE	THRESHOLD ACCURACY OVER TEMPERATURE
<a href="#">TLV6700</a>	Window	1.8 V to 18 V	1%
<a href="#">TLV6703</a>	Non-Inverting Single Channel	1.8 V to 18 V	1%
<a href="#">TLV6710</a>	Window	1.8 V to 36 V	0.75%
<a href="#">TLV6713</a>	Non-Inverting Single Channel	1.8 V to 36 V	0.75%

## 6 Pin Configuration and Functions

**DDC Package  
SOT-23-6  
Top View**



**DSE Package  
WSO6-6  
Top View**



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DDC	DSE		
GND	2, 4, 6	1, 3, 5	—	Connect all three pins to ground.
OUT	1	6	O	SENSE comparator has an open-drain output. OUT is driven low when SENSE is below ( $V_{IT-}$ ). OUT goes high when SENSE returns above the respective threshold ( $V_{IT+}$ ).
SENSE	3	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage ( $V_{IT-}$ ), OUT is driven low.
VDD	5	2	I	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1- $\mu$ F ceramic capacitor close to this pin.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	VDD	-0.3	20	V
	OUT	-0.3	20	
	SENSE	-0.3	7	
Current	OUT (output sink current)		40	mA
Temperature	Operating junction, T <sub>J</sub>	-40	125	°C
	Storage, T <sub>stg</sub>	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground pin.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage	1.8		18	V
V <sub>I</sub>	Input voltage	0		6.5	V
V <sub>O</sub>	Output voltage	0		18	V

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TLV6703		UNIT	
	DDC (SOT)	DSE (WSON)		
	6 PINS	6 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	204.6	194.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.5	128.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	54.3	153.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.8	11.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	52.8	157.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor an IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

Over the operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $1.8\text{ V} < V_{DD} < 18\text{ V}$  (unless otherwise noted). Typical values are at  $T_J = 25^{\circ}\text{C}$  and  $V_{DD} = 5\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(POR)}$	Power-on reset voltage <sup>(1)</sup>	$V_{OLmax} = 0.2\text{ V}$ , output sink current = $15\ \mu\text{A}$			0.8	V
$V_{IT+}$	Positive-going input threshold voltage	$V_{DD} = 1.8\text{V}$ and $18\text{ V}$ , $T_J = 25^{\circ}\text{C}$	398	400	402.5	mV
		$V_{DD} = 1.8\text{V}$ and $18\text{ V}$ , $T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	396		404	
$V_{IT-}$	Negative-going input threshold voltage	$V_{DD} = 1.8\text{V}$ and $18\text{ V}$ , $T_J = 25^{\circ}\text{C}$	391.6	394.5	397.5	mV
		$V_{DD} = 1.8\text{V}$ and $18\text{ V}$ , $T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	387		400	
$V_{hys}$	Hysteresis voltage ( $hys = V_{IT+} - V_{IT-}$ )			5.5	12	mV
$I_{(SENSE)}$	Input current (at the SENSE pin)	$V_{DD} = 1.8\text{ V}$ and $18\text{ V}$ , $V_I = 6.5\text{ V}$	-25	1	25	nA
$V_{OL}$	Low-level output voltage	$V_{DD} = 1.3\text{ V}$ , output sink current = $0.4\text{ mA}$			250	mV
		$V_{DD} = 1.8\text{ V}$ , output sink current = $3\text{ mA}$			250	
		$V_{DD} = 5\text{ V}$ , output sink current = $5\text{ mA}$			250	
$I_{(kg(OD))}$	Open-drain output leakage-current	$V_{DD} = 1.8\text{ V}$ and $18\text{ V}$ , $V_O = V_{DD}$			300	nA
		$V_{DD} = 1.8\text{ V}$ , $V_O = 18\text{ V}$			300	
$I_{DD}$	Supply current	$V_{DD} = 1.8\text{ V}$ , no load		5.5	11	$\mu\text{A}$
		$V_{DD} = 5\text{ V}$		6	13	
		$V_{DD} = 12\text{ V}$		6	13	
		$V_{DD} = 18\text{ V}$		7	13	
UVLO	Undervoltage lockout <sup>(2)</sup>	$V_{DD}$ falling	1.3		1.7	V

(1) The lowest supply voltage ( $V_{DD}$ ) at which output is active;  $t_{r(VDD)} > 15\ \mu\text{s/V}$ . Below  $V_{(POR)}$ , the output cannot be determined.

(2) When  $V_{DD}$  falls below UVLO, OUT is driven low. The output cannot be determined below  $V_{(POR)}$ .

## 7.6 Timing Requirements

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay <sup>(1)</sup>		18		$\mu\text{s}$
$t_{pd(LH)}$	Low-to-high propagation delay <sup>(1)</sup>		29		$\mu\text{s}$
$t_{d(start)}$	Start-up delay <sup>(2)</sup>		150		$\mu\text{s}$

(1) High-to-low and low-to-high refers to the transition at the input pin (SENSE).

(2) During power on,  $V_{DD}$  must exceed 1.8 V for at least 150  $\mu\text{s}$  before the output is in a correct state.

## 7.7 Switching Characteristics

over operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output rise time $V_{DD} = 5\text{ V}$ , 10-mV input overdrive, $R_P = 10\text{ k}\Omega$ , $V_O = (0.1\text{ to }0.9) \times V_{DD}$		2.2		$\mu\text{s}$
$t_f$	Output fall time $V_{DD} = 5\text{ V}$ , 10-mV input overdrive, $R_P = 10\text{ k}\Omega$ , $V_O = (0.1\text{ to }0.9) \times V_{DD}$		0.22		$\mu\text{s}$

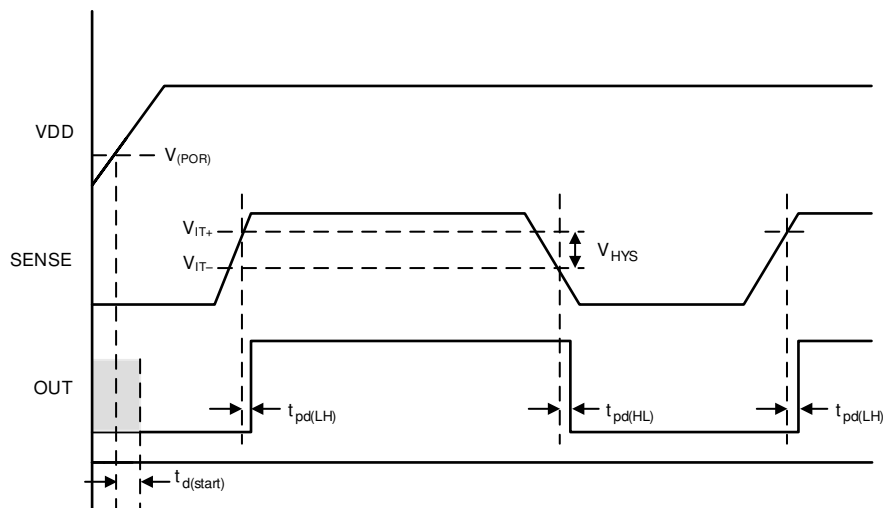


Figure 1. Timing Diagram

## 7.8 Typical Characteristics

at  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

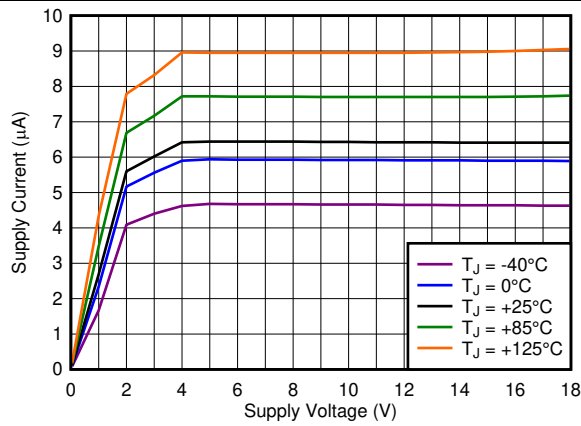


Figure 2. Supply Current ( $I_{DD}$ ) vs Supply Voltage ( $V_{DD}$ )

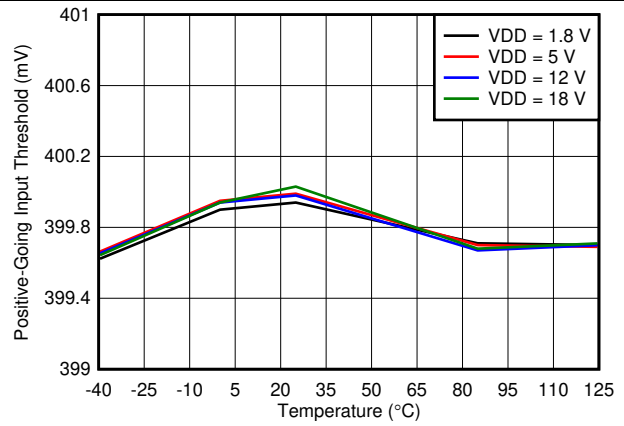


Figure 3. Rising Input Threshold Voltage ( $V_{IT+}$ ) vs Temperature

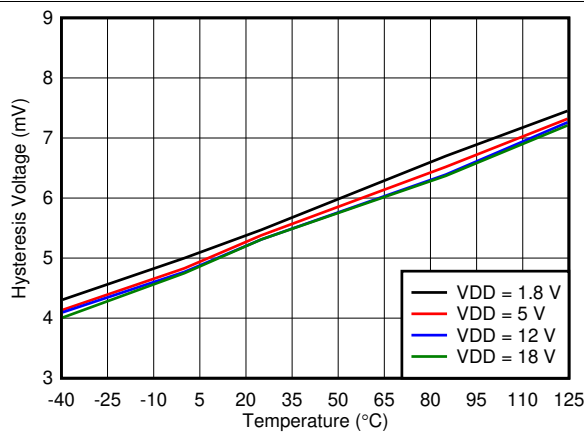


Figure 4. Hysteresis ( $V_{hys}$ ) vs Temperature

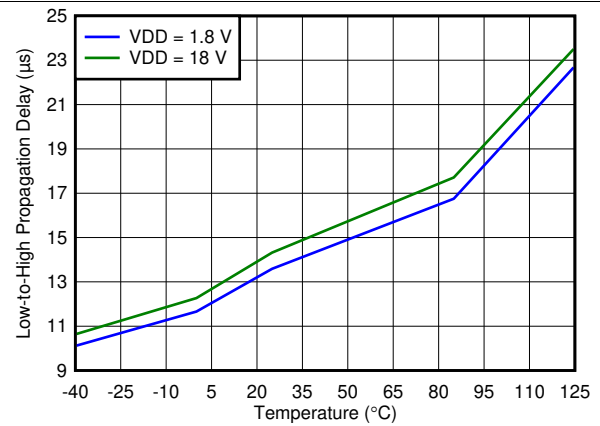


Figure 5. Propagation Delay vs Temperature (High-to-Low Transition at Sense)

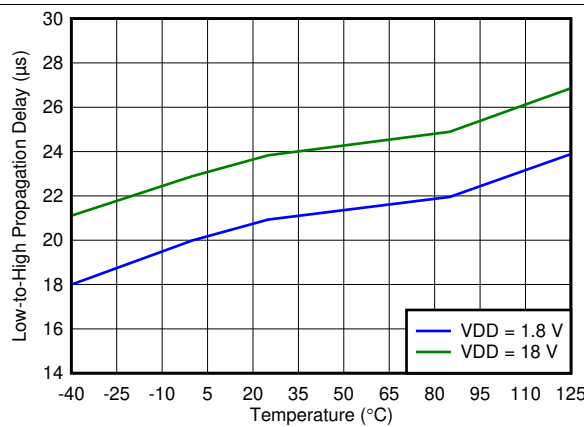


Figure 6. Propagation Delay vs Temperature (Low-to-High Transition at Sense)

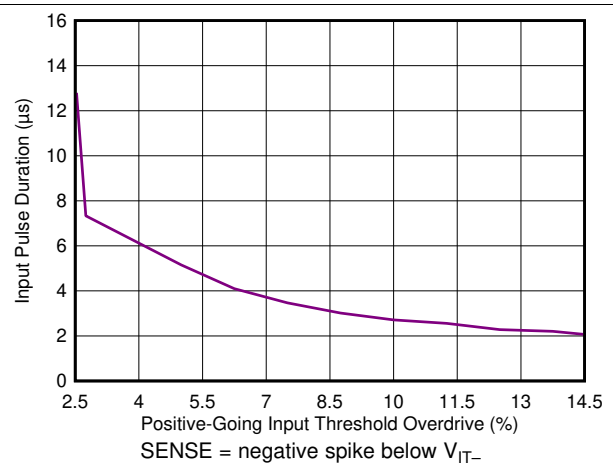


Figure 7. Minimum Pulse Width vs Threshold Overdrive Voltage  
SENSE = negative spike below  $V_{IT-}$

### Typical Characteristics (continued)

at  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

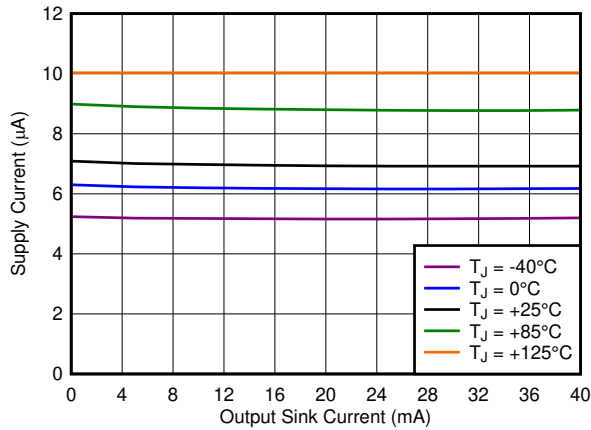


Figure 8. Supply Current ( $I_{DD}$ ) vs Output Sink Current

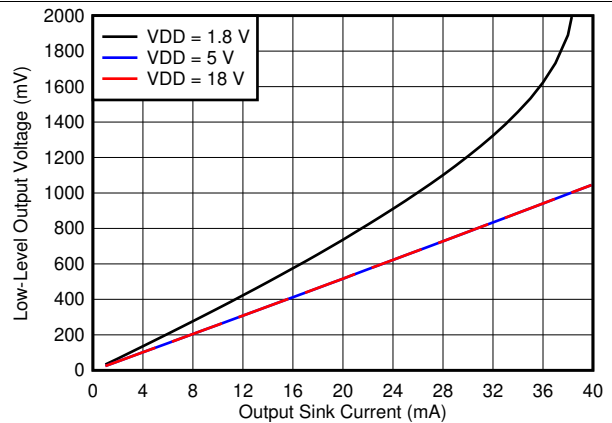


Figure 9. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $-40^\circ\text{C}$ )

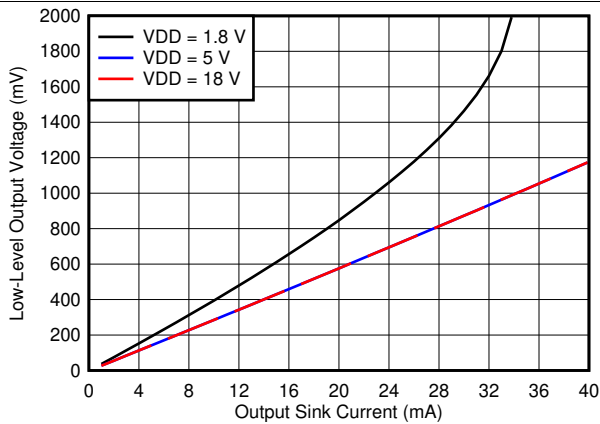


Figure 10. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $0^\circ\text{C}$ )

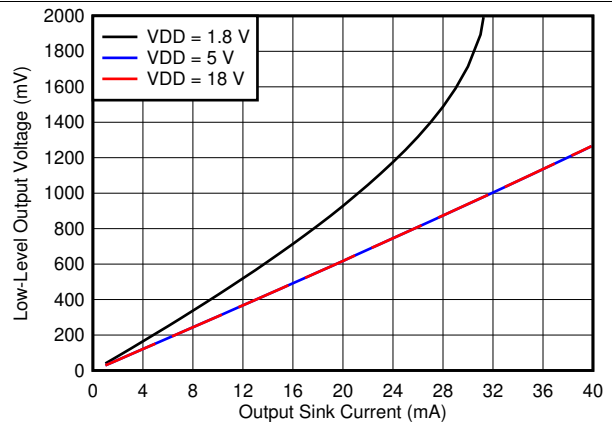


Figure 11. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $25^\circ\text{C}$ )

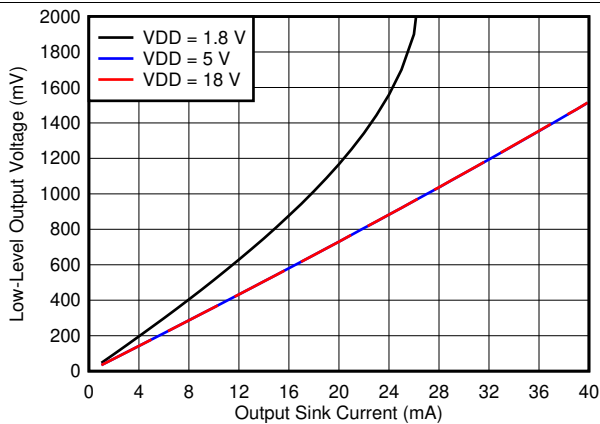


Figure 12. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $85^\circ\text{C}$ )

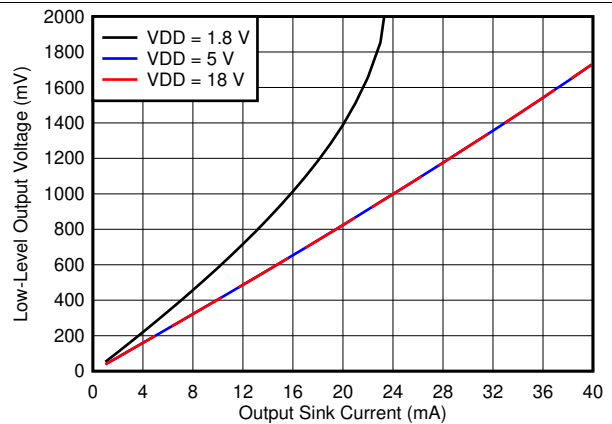


Figure 13. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $125^\circ\text{C}$ )



## 8 Detailed Description

### 8.1 Overview

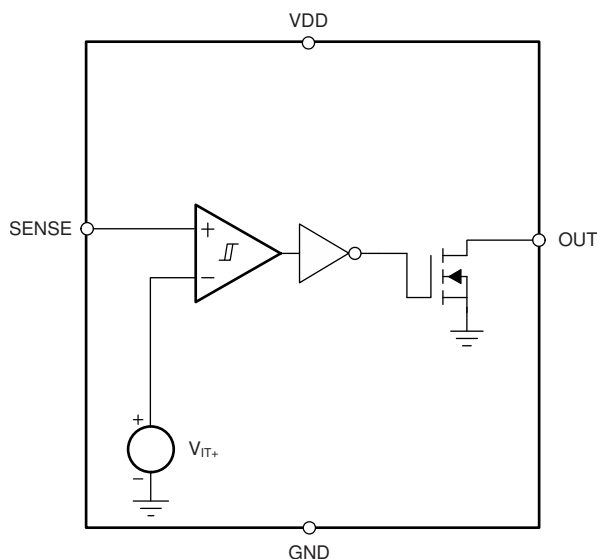
The TLV6703 provides precision voltage detection. The TLV6703 is a wide-supply voltage range (1.8 V to 18 V) comparator with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The output is also rated to 18 V, independent of supply voltage, and can sink up to 40 mA.

The TLV6703 asserts the output signal, as shown in Table 2. To monitor any voltage above 0.4 V, set the input using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. Broad voltage thresholds are supported that enable the device for use in a wide array of applications.

Table 2. TLV6703 Truth Table

CONDITION	OUTPUT	OUTPUT STATE
$\text{SENSE} > V_{IT+}$	OUT high	Output high impedance
$\text{SENSE} < V_{IT-}$	OUT low	Output sinking

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Input Pin (SENSE)

The TLV6703 comparator has two inputs: one external input, and one input internally connected to the internal 400mV reference. The comparator rising threshold is trimmed to be equal to the reference voltage (400 mV). The comparator also has a built-in falling hysteresis that makes the device less sensitive to supply-rail noise and provides stable operation.

The comparator input (SENSE) is able to swing from ground to 6.5 V, regardless of the device supply voltage. Although not required in most cases, to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor at the comparator input.

OUT is driven to logic low when the input SENSE voltage drops below ( $V_{IT-}$ ). When the voltage exceeds  $V_{IT+}$ , the output (OUT) goes to a high-impedance state; see [Figure 1](#).

### 8.3.2 Output Pin (OUT)

In a typical TLV6703 application, the output is connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6703 device provides an open-drain output (OUT). Use a pullup resistor to hold this line high when the output goes to high impedance (not asserted). To connect the output to another device at the correct interface-voltage level, connect a pullup resistor to the proper voltage rail. The TLV6703 output can be pulled up to 18 V, independent of the device supply voltage.

[Table 2](#) and the [Input Pin \(SENSE\)](#) section describe how the output is asserted or de-asserted. See [Figure 1](#) for a timing diagram that describes the relationship between threshold voltage and the respective output.

### 8.3.3 Immunity to Input-Pin Voltage Transients

The TLV6703 is relatively immune to short voltage transient spikes on the sense pin. Sensitivity to transients depends on both transient duration and amplitude; see [Figure 7](#), *Minimum Pulse Width vs Threshold Overdrive Voltage*.

## 8.4 Device Functional Modes

### 8.4.1 Normal Operation ( $V_{DD} > UVLO$ )

When the voltage on  $V_{DD}$  is greater than 1.8 V for at least 150  $\mu$ s, the OUT signal correspond to the voltage on SENSE as listed in [Table 2](#).

### 8.4.2 Undervoltage Lockout ( $V_{(POR)} < V_{DD} < UVLO$ )

When the voltage on  $V_{DD}$  is less than the device UVLO voltage, and greater than the power-on reset voltage,  $V_{(POR)}$ , the OUT signal is asserted regardless of the voltage on SENSE.

### 8.4.3 Power-On Reset ( $V_{DD} < V_{(POR)}$ )

When the voltage on  $V_{DD}$  is lower than the required voltage to internally pull the asserted output to GND ( $V_{(POR)}$ ), SENSE is in a high-impedance state.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TLV6703 device is a wide-supply voltage comparator that operates over a  $V_{DD}$  range of 1.8 V to 18 V. The device has a high-accuracy comparator with an internal 400-mV reference and an open-drain output rated to 18 V for precision voltage detection. The device can be used as a voltage monitor. The monitored voltage are set with the use of external resistors.

#### 9.1.1 $V_{PULLUP}$ to a Voltage Other Than $V_{DD}$

The output is often tied to  $V_{DD}$  through a resistor. However, some applications may require the output to be pulled up to a higher or lower voltage than  $V_{DD}$  to correctly interface with the reset and enable pins of other devices.

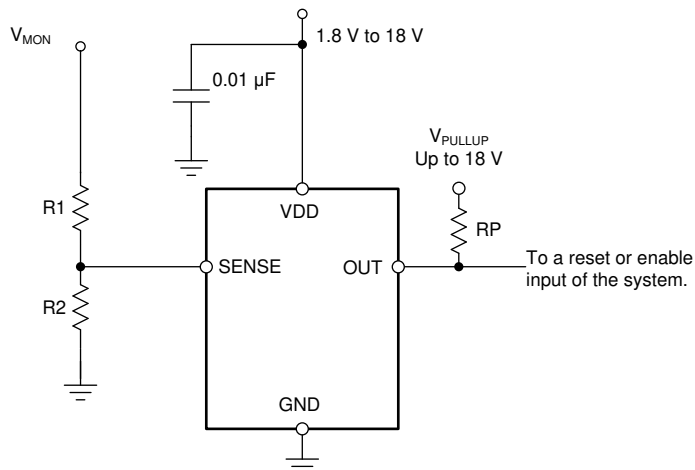


Figure 14. Interfacing to a Voltage Other Than  $V_{DD}$

## Application Information (continued)

### 9.1.2 Monitoring $V_{DD}$

Many applications monitor the same rail that is powering  $V_{DD}$ . In these applications the resistor divider is simply connected to the  $V_{DD}$  rail.

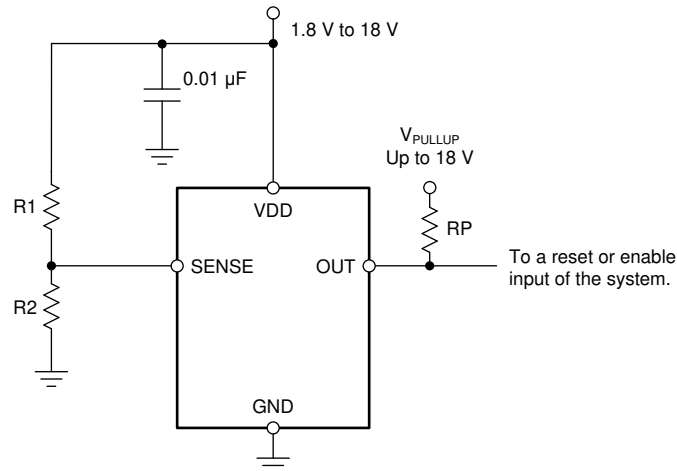
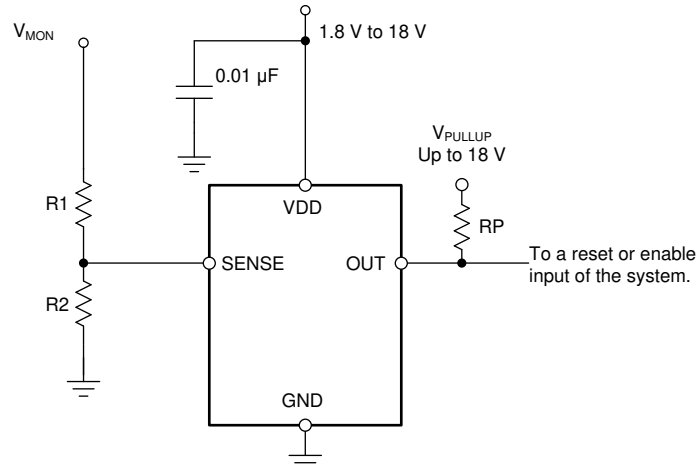


Figure 15. Monitoring the Same Voltage as  $V_{DD}$

### 9.1.3 Monitoring a Voltage Other Than $V_{DD}$

Some applications monitor rails other than the one that is powering  $V_{DD}$ . In these types of applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.

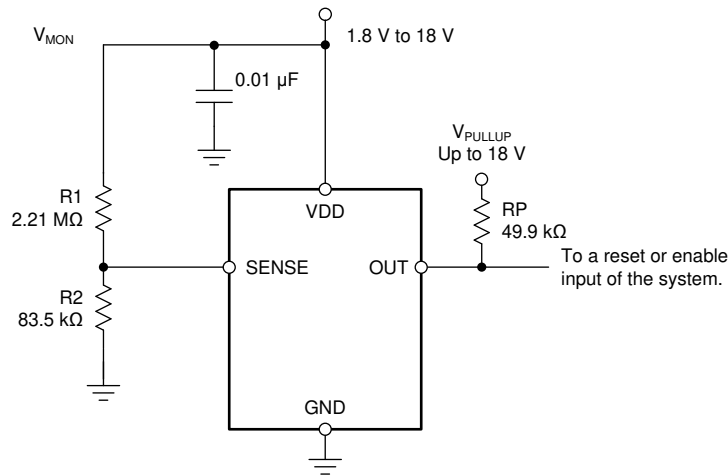


NOTE: The input can monitor a voltage greater than maximum  $V_{DD}$  with the use of an external resistor divider network.

Figure 16. Monitoring a Voltage Other Than  $V_{DD}$

## 9.2 Typical Application

The TLV6703 device is a wide-supply voltage comparator that operates over a  $V_{DD}$  range of 1.8 to 18 V. The monitored voltage is set with the use of external resistors, so the device can be used either as a precision voltage monitor.



**Figure 17. Wide VIN Voltage Monitor**

### 9.2.1 Design Requirements

For this design example, use the values summarized in [Table 3](#) as the input parameters.

**Table 3. Design Parameters**

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	12-V nominal rail with maximum falling threshold of 10%	$V_{MON(UV)} = 10.99 \text{ V (8.33\%)}$

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using [Equation 1](#) to determine  $V_{MON(UV)}$ .

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-} \quad (1)$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins
- $V_{MON(UV)}$  is the target voltage at which an undervoltage condition is detected

Choose  $R_{TOTAL}$  ( $= R1 + R2$ ) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, refer to application report [SLVA450, Optimizing Resistor Dividers at a Comparator Input](#), available for download from [www.ti.com](http://www.ti.com).

### 9.2.2.2 Pullup Resistor Selection

To ensure the proper voltage level, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current ( $I_{lk(OD)}$ ) multiplied by the resistor is greater than the desired logic-high voltage. These values are specified in the [Electrical Characteristics](#).

Use [Equation 2](#) to calculate the value of the pullup resistor.

$$\frac{(V_{HI} - V_{PU})}{I_{lk(OD)}} \geq R_{PU} \geq \frac{V_{PU}}{I_O} \quad (2)$$

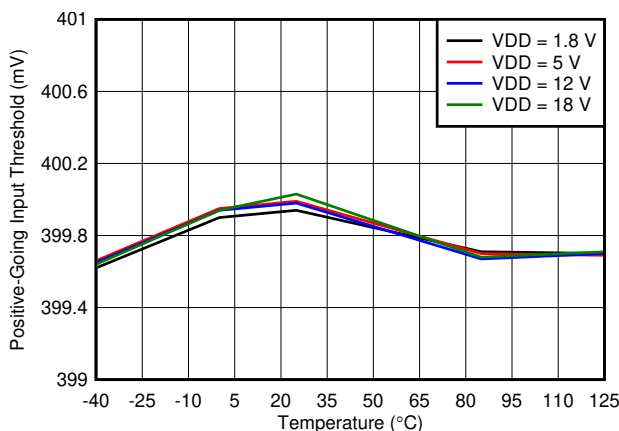
### 9.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 0.1- $\mu$ F low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

### 9.2.2.4 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor from the comparator input (SENSE) to the GND pin for good analog design practice. This capacitor placement reduces device sensitivity to transients.

## 9.2.3 Application Curves



**Figure 18. Rising Input Threshold Voltage ( $V_{IT+}$ ) vs Temperature**

## 9.3 Dos and Don'ts

Do connect a 0.1- $\mu$ F decoupling capacitor from  $V_{DD}$  to GND for best system performance.

If the monitored rail is noisy, do connect a decoupling capacitor from the comparator input (sense) to GND.

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the effect to the accuracy.

Don't use a pullup resistor that is too small, because the larger current sunk by the output then exceeds the desired low-level output voltage ( $V_{OL}$ ).

## 10 Power-Supply Recommendations

These devices operate from an input voltage supply range between 1.8 V and 18 V.

## 11 Layout

### 11.1 Layout Guidelines

Placing a 0.1- $\mu\text{F}$  capacitor close to the VDD pin to reduce the input impedance to the device is good analog design practice.

### 11.2 Layout Example

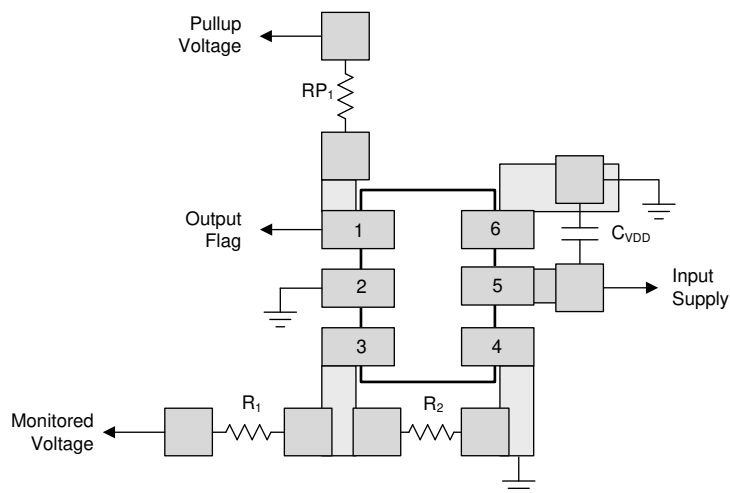


Figure 19. Layout Example

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

The [DIP Adapter Evaluation Module](#) allows conversion of the SOT-23-6 package to a standard DIP-6 pinout for ease of prototyping and bench evaluation.

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV6703DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MR1	<a href="#">Samples</a>
TLV6703DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MR1	<a href="#">Samples</a>
TLV6703DSER	ACTIVE	WSO	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HE	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV6703 :**

- Automotive: [TLV6703-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6703DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6703DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6703DSER	WSO8	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

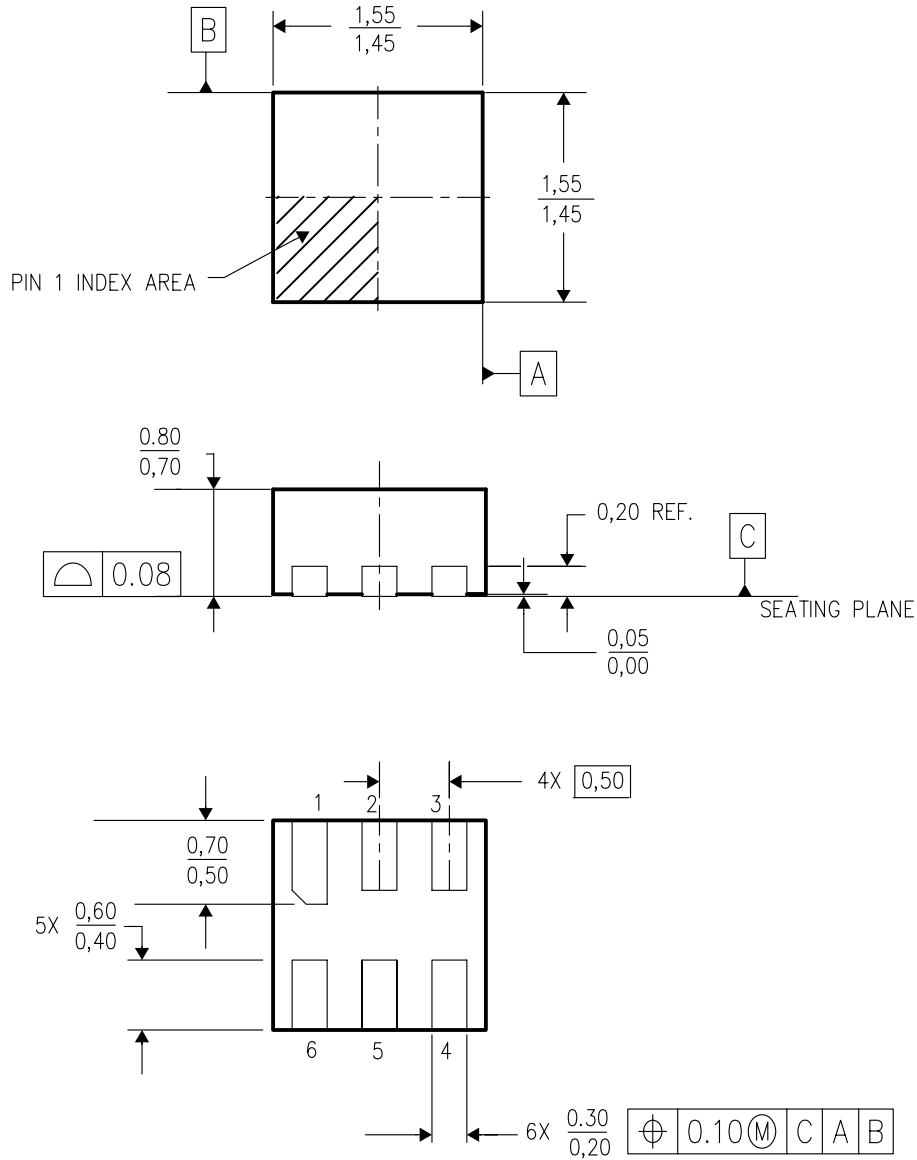
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6703DDCR	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TLV6703DDCT	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0
TLV6703DSER	WSON	DSE	6	3000	205.0	200.0	33.0

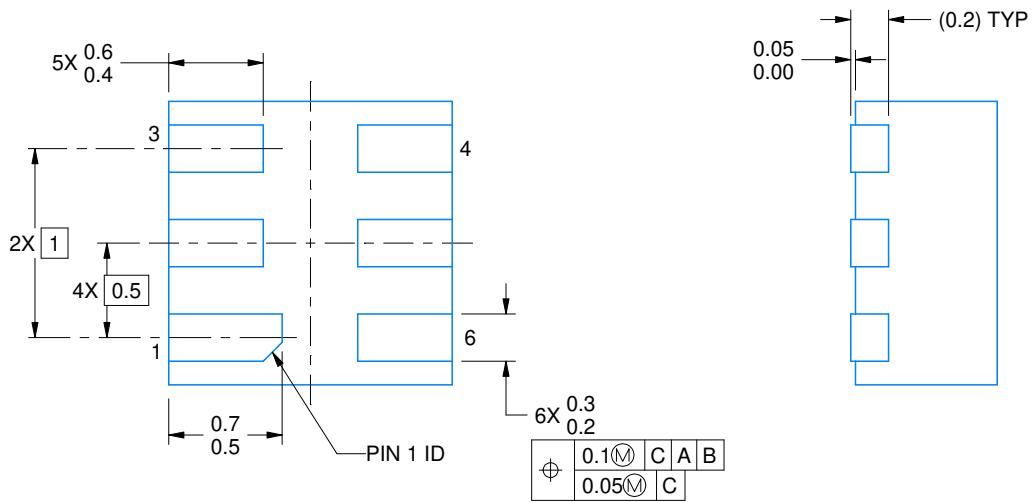
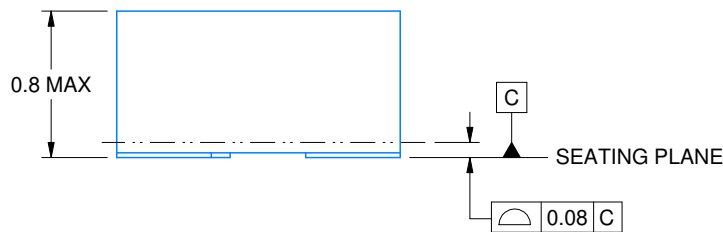
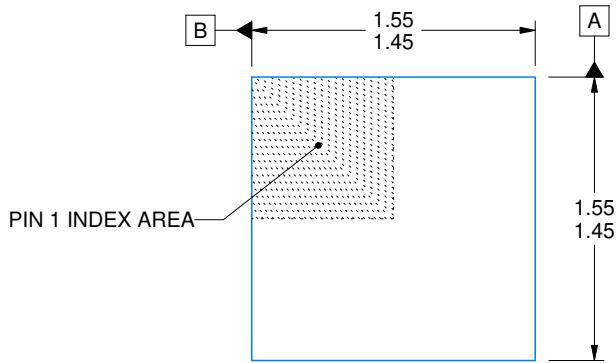
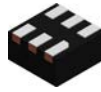
DSE (S-PDSO-N6)

PLASTIC SMALL OUTLINE



4207810/A 03/06

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - D. This package is lead-free.



4220552/A 04/2021

NOTES:

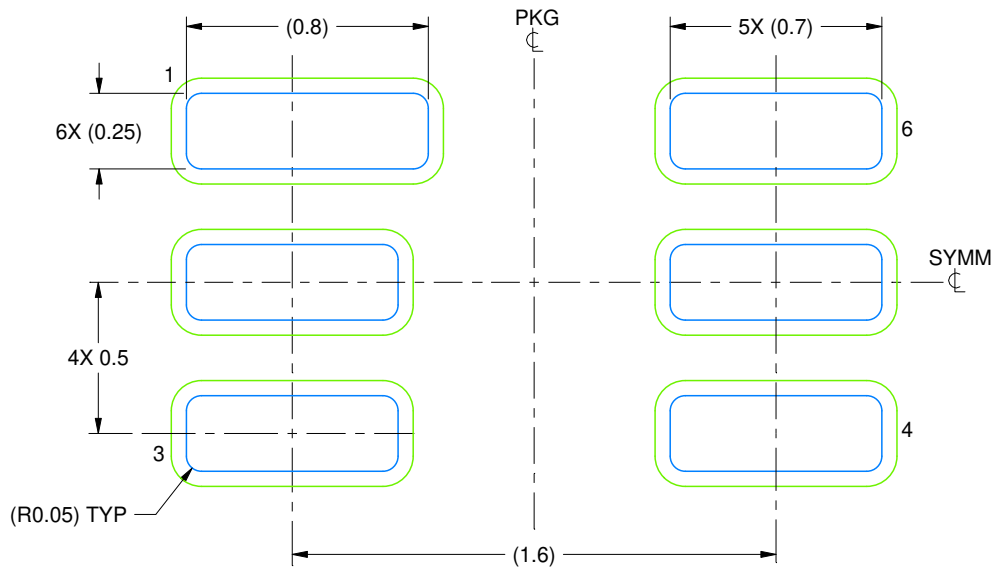
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

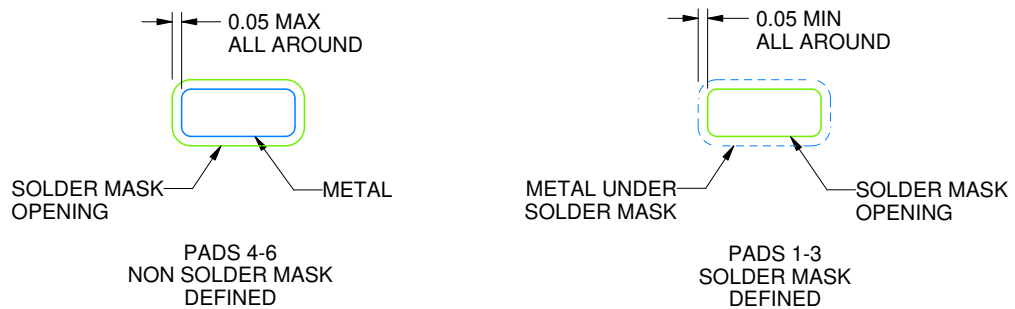
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS

4220552/A 04/2021

NOTES: (continued)

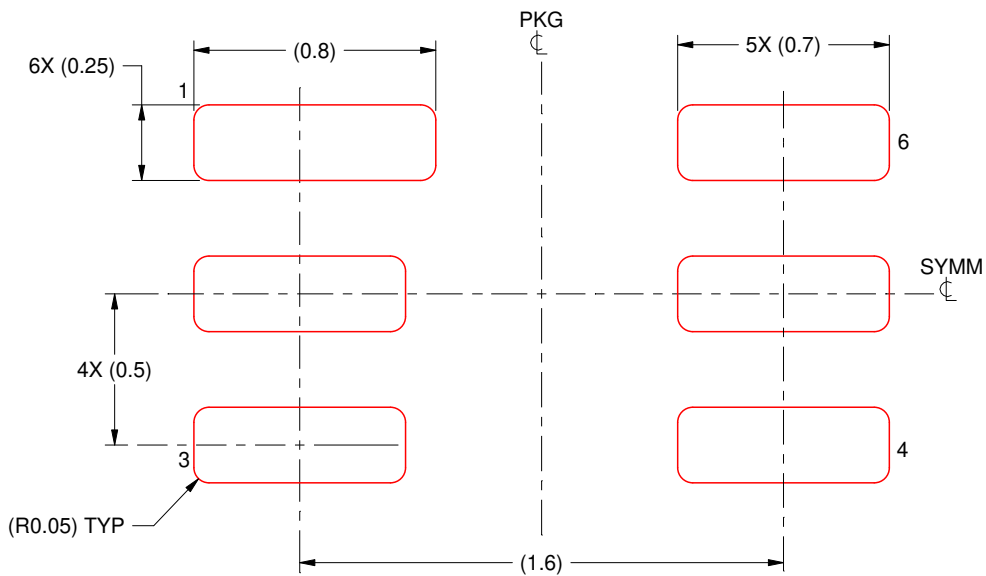
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

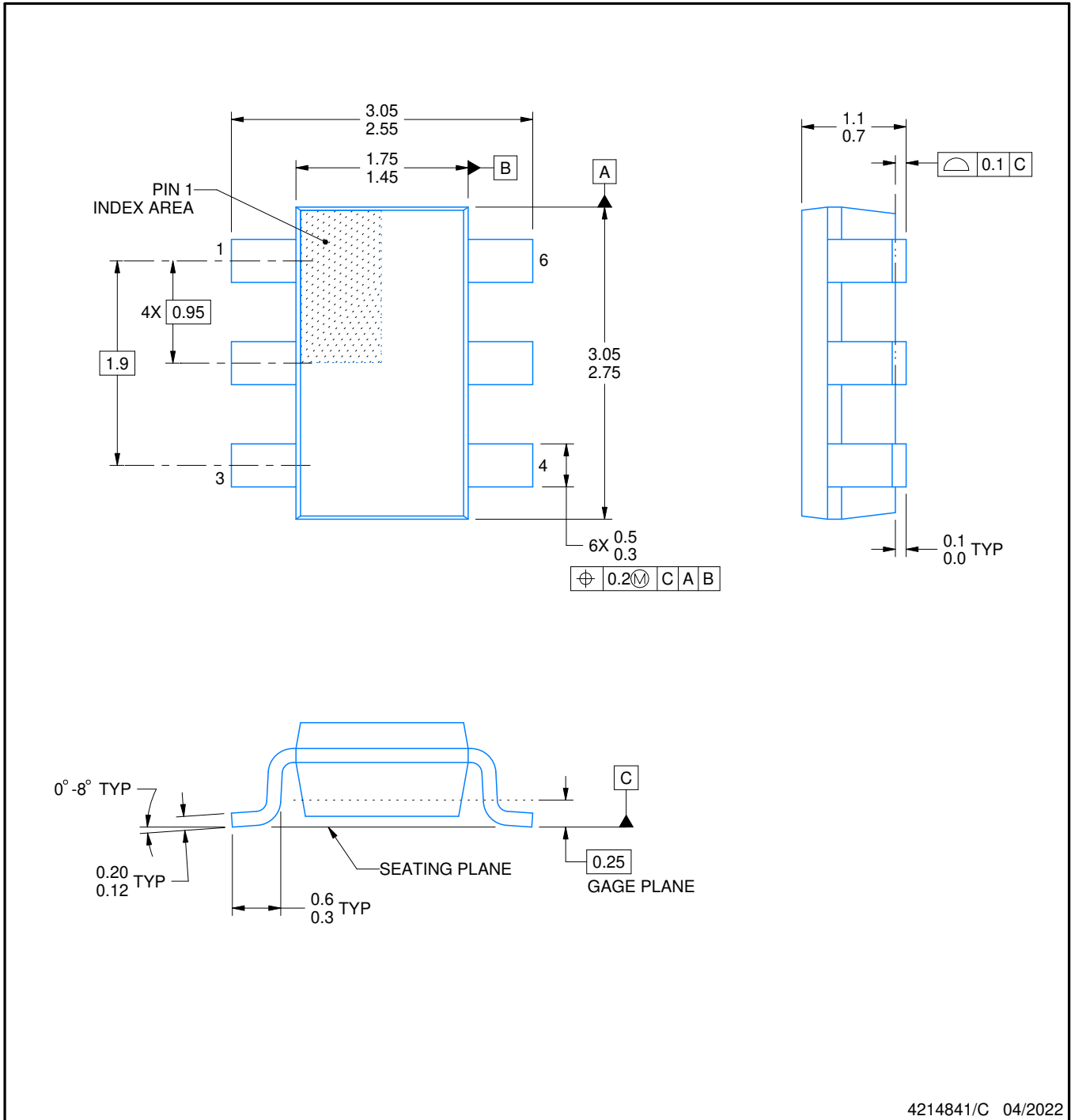


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





4214841/C 04/2022

NOTES:

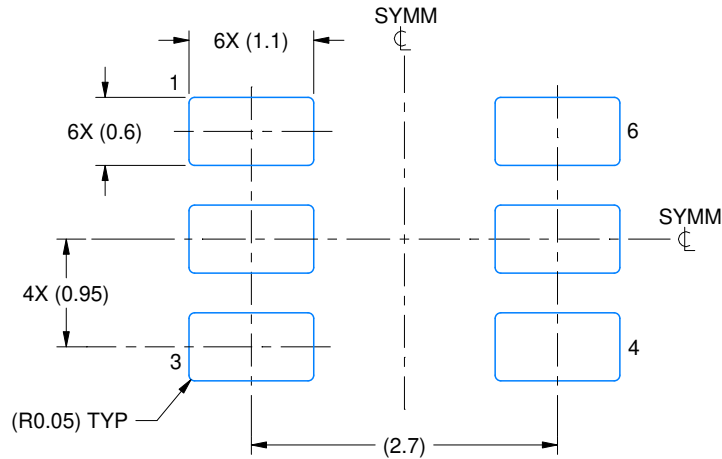
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

# EXAMPLE BOARD LAYOUT

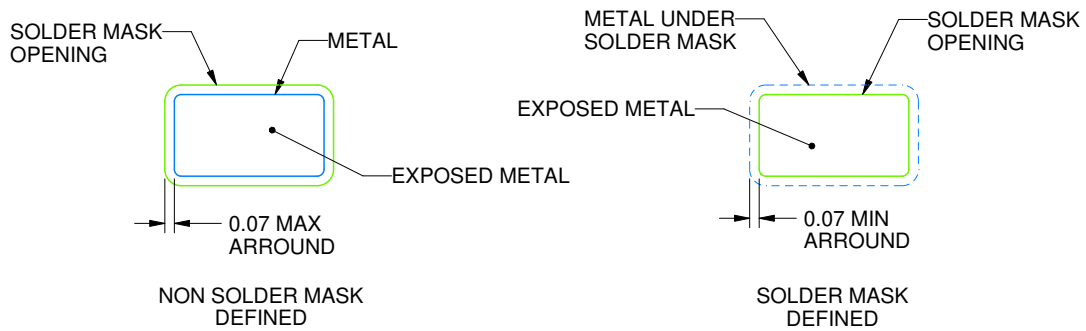
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X



SOLDEMASK DETAILS

4214841/C 04/2022

NOTES: (continued)

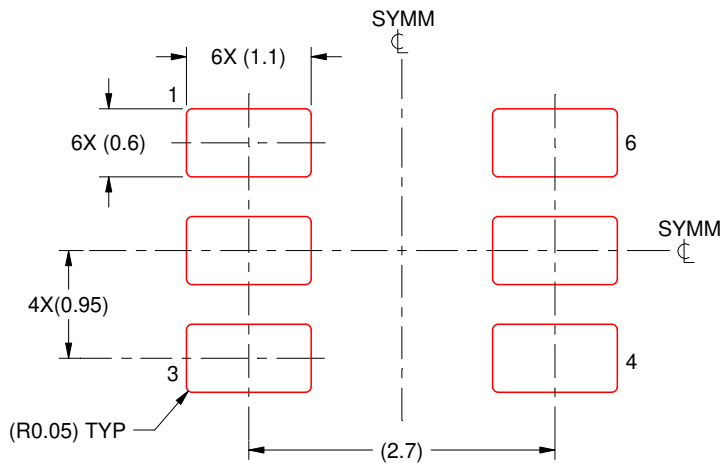
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214841/C 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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