

Memory FRAM

1 M Bit (128 K × 8)

MB85R1001A

■ DESCRIPTIONS

The MB85R1001A is an FRAM (Ferroelectric Random Access Memory) chip consisting of 131,072 words × 8 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85R1001A is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85R1001A can be used for 10^{10} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E²PROM.

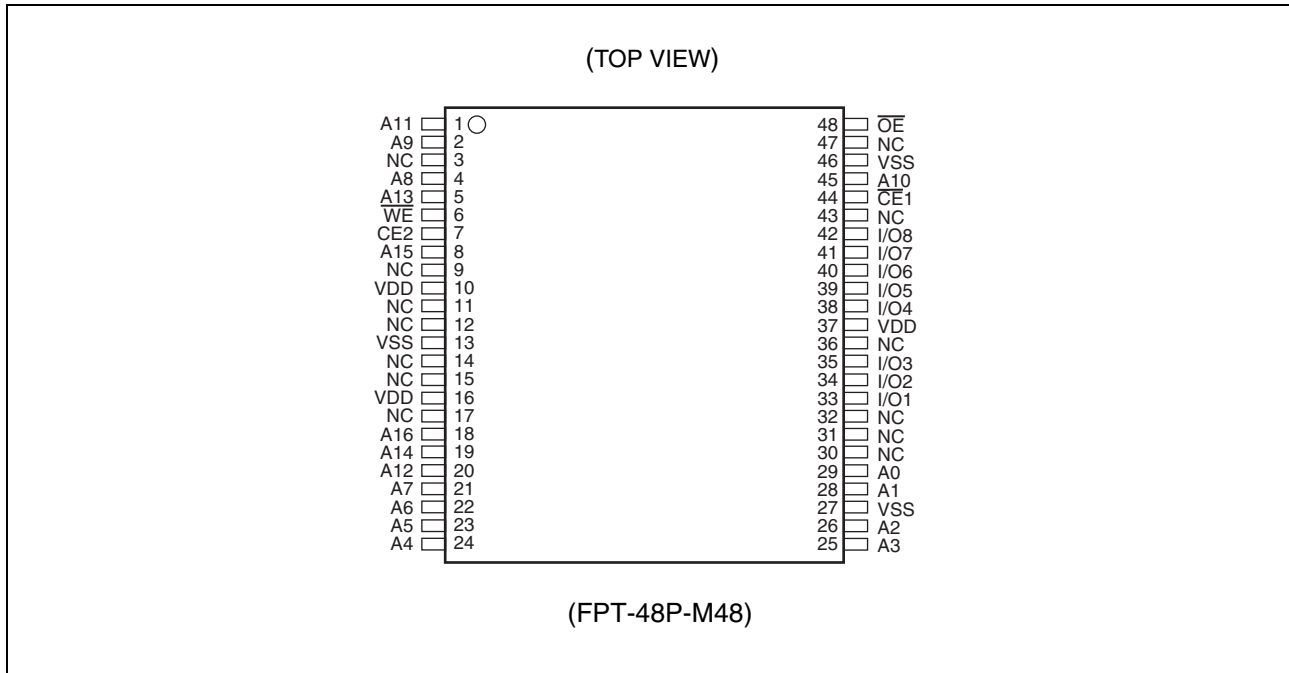
The MB85R1001A uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

■ FEATURES

- Bit configuration : 131,072 words × 8 bits
- Read/write endurance : 10^{10} times
- Operating power supply voltage : 3.0 V to 3.6 V
- Operating temperature range : - 40 °C to + 85 °C
- Data retention : 10 years (+ 55 °C)
- Package : 48-pin plastic TSOP (1)

MB85R1001A

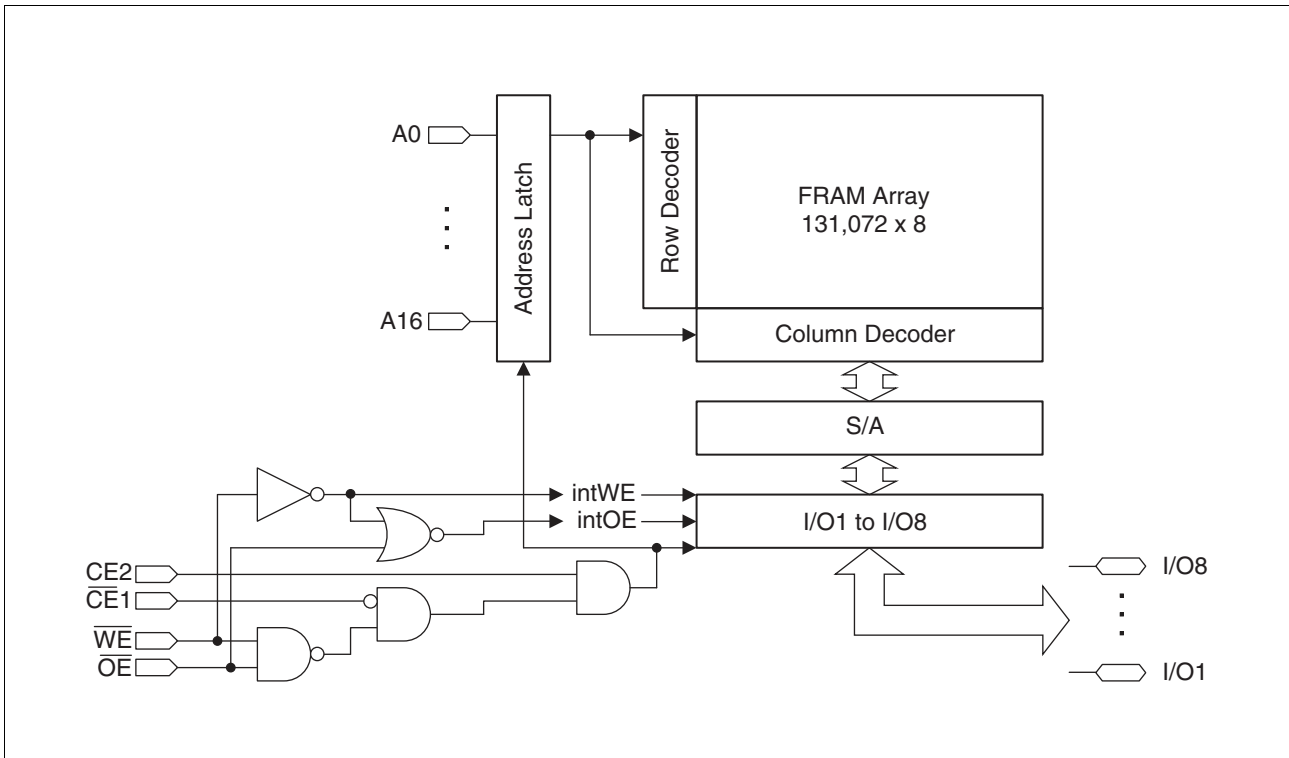
■ PIN ASSIGNMENTS



■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1, 2, 4, 5, 8, 18 to 26, 28, 29, 45	A0 to A16	Address Input pins
33 to 35, 38 to 42	I/O1 to I/O8	Data Input/Output pins
44	$\overline{CE}1$	Chip Enable 1 Input pin
7	CE2	Chip Enable 2 Input pin
6	\overline{WE}	Write Enable Input pin
48	\overline{OE}	Output Enable Input pin
10, 16, 37	VDD	Supply Voltage pins Connect all three pins to the power supply.
13, 27, 46	VSS	Ground pins Connect all three pins to ground.
3, 9, 11, 12, 14, 15, 17, 30 to 32, 36, 43, 47	NC	No Connect pins

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Operation Mode	$\overline{CE1}$	CE2	\overline{WE}	\overline{OE}	I/O1 to I/O8	Supply Current
Standby Precharge	H	X	X	X	Hi-Z	Standby (I _{SB})
	X	L	X	X		
	X	X	H	H		
Read	\downarrow	H	H	L	Data Output	Operation (I _{CC})
	L	\uparrow				
Read (Pseudo-SRAM, \overline{OE} control*1)	L	H	H	\downarrow		
Write	\downarrow	H	L	H	Data Input	
	L	\uparrow				
Write (Pseudo-SRAM, \overline{WE} control*2)	L	H	\downarrow	H		

Note: L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, Hi-Z = High Impedance

\downarrow : Latch address and latch data at falling edge, \uparrow : Latch address and latch data at rising edge

*1 : \overline{OE} control of the Pseudo-SRAM means the valid address at the falling edge of \overline{OE} to read.

*2 : \overline{WE} control of the Pseudo-SRAM means the valid address and data at the falling edge of \overline{WE} to write.

MB85R1001A

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V _{CC}	- 0.5	+ 4.0	V
Input Pin Voltage*	V _{IN}	- 0.5	V _{CC} + 0.5 (≤ 4.0)	V
Output Pin Voltage*	V _{OUT}	- 0.5	V _{CC} + 0.5 (≤ 4.0)	V
Operating Temperature	T _A	- 40	+ 85	°C
Storage Temperature	T _{STG}	- 40	+ 125	°C

* : All voltages are referenced to VSS = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage*	V _{CC}	3.0	3.3	3.6	V
High Level Input Voltage*	V _{IH}	V _{CC} × 0.8	—	V _{CC} + 0.5 (≤ 4.0)	V
Low Level Input Voltage*	V _{IL}	- 0.5	—	+ 0.6	V
Operating Temperature	T _A	- 40	—	+ 85	°C

* : All voltages are referenced to VSS = 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$ I_{LI} $	$V_{IN} = 0 \text{ V to } V_{CC}$	—	—	10	μA
Output Leakage Current	$ I_{LO} $	$V_{OUT} = 0 \text{ V to } V_{CC}$, $\overline{CE1} = V_{IH}$ or $\overline{OE} = V_{IH}$	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CE1} = 0.2 \text{ V}$, $CE2 = V_{CC} - 0.2 \text{ V}$, $I_{out} = 0 \text{ mA}^{*1}$	—	10	15	mA
Standby Current	I_{SB}	$\overline{CE1} \geq V_{CC} - 0.2 \text{ V}$	—	10	50	μA
		$CE2 \leq 0.2 \text{ V}^{*2}$				
		$\overline{OE} \geq V_{CC} - 0.2 \text{ V}$, $\overline{WE} \geq V_{CC} - 0.2 \text{ V}^{*2}$				
High Level Output Voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$V_{CC} \times 0.8$	—	—	V
Low Level Output Voltage	V_{OL}	$I_{OL} = 2.0 \text{ mA}$	—	—	0.4	V

*1 : During the measurement of I_{CC} , the Address, Data In were taken to only change once per active cycle.
 I_{out} : output current

*2 : All pins other than setting pins should be input at the CMOS level voltages such as $H \geq V_{CC} - 0.2 \text{ V}$, $L \leq 0.2 \text{ V}$.

MB85R1001A

2. AC Characteristics

• AC Test Conditions

Supply Voltage	: 3.0 V to 3.6 V
Operating Temperature	: -40 °C to +85 °C
Input Voltage Amplitude	: 0.3 V to 2.7 V
Input Rising Time	: 5 ns
Input Falling Time	: 5 ns
Input Evaluation Level	: 2.0 V / 0.8 V
Output Evaluation Level	: 2.0 V / 0.8 V
Output Impedance	: 50 pF

(1) Read Cycle

(within recommended operating conditions)

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle Time	t _{RC}	150	—	ns
CE1 Active Time	t _{CA1}	120	—	ns
CE2 Active Time	t _{CA2}	120	—	ns
OE Active Time	t _{RP}	120	—	ns
Precharge Time	t _{PC}	20	—	ns
Address Setup Time	t _{AS}	0	—	ns
Address Hold Time	t _{AH}	50	—	ns
OE Setup Time	t _{ES}	0	—	ns
Output Hold Time	t _{OH}	0	—	ns
Output Set Time	t _{LZ}	30	—	ns
CE1 Access Time	t _{CE1}	—	100	ns
CE2 Access Time	t _{CE2}	—	100	ns
OE Access Time	t _{OE}	—	100	ns
Output Floating Time	t _{OHZ}	—	20	ns

(2) Write Cycle

(within recommended operating conditions)

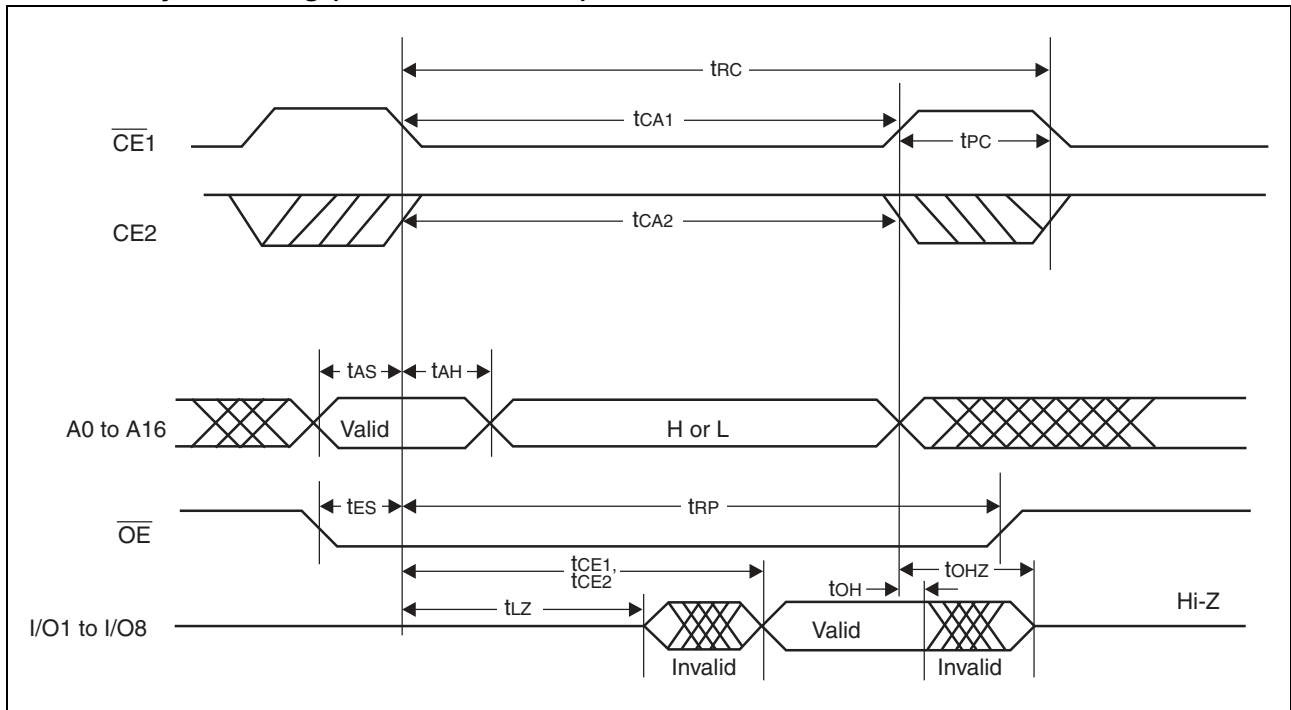
Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t _{WC}	150	—	ns
CE1 Active Time	t _{CA1}	120	—	ns
CE2 Active Time	t _{CA2}	120	—	ns
Precharge Time	t _{PC}	20	—	ns
Address Setup Time	t _{AS}	0	—	ns
Address Hold Time	t _{AH}	50	—	ns
Write Pulse Width	t _{WP}	120	—	ns
Data Setup Time	t _{DS}	0	—	ns
Data Hold Time	t _{DH}	50	—	ns
Write Setup Time	t _{WS}	0	—	ns

3. Pin Capacitance

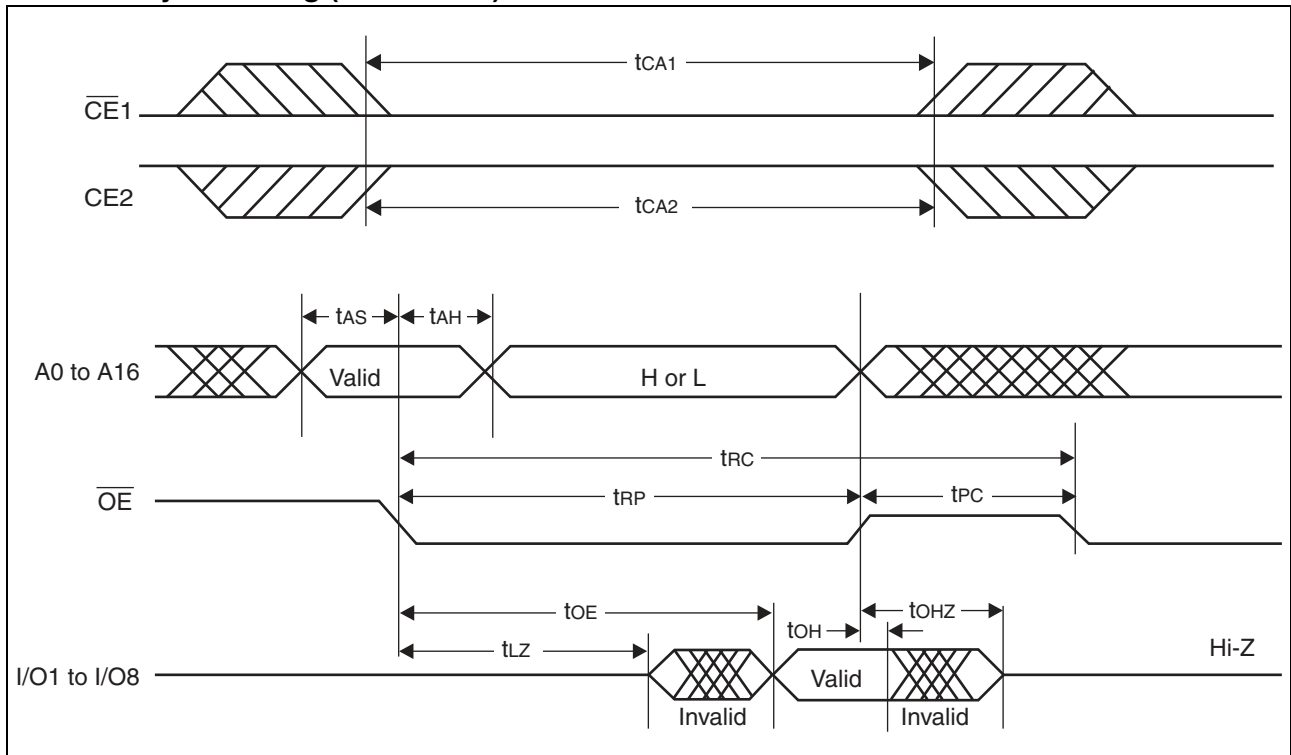
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	$V_{IN} = V_{OUT} = 0\text{ V}$, $f = 1\text{ MHz}$, $T_A = +25\text{ °C}$	—	—	10	pF
Output Capacitance	C_{OUT}		—	—	10	pF

■ TIMING DIAGRAMS

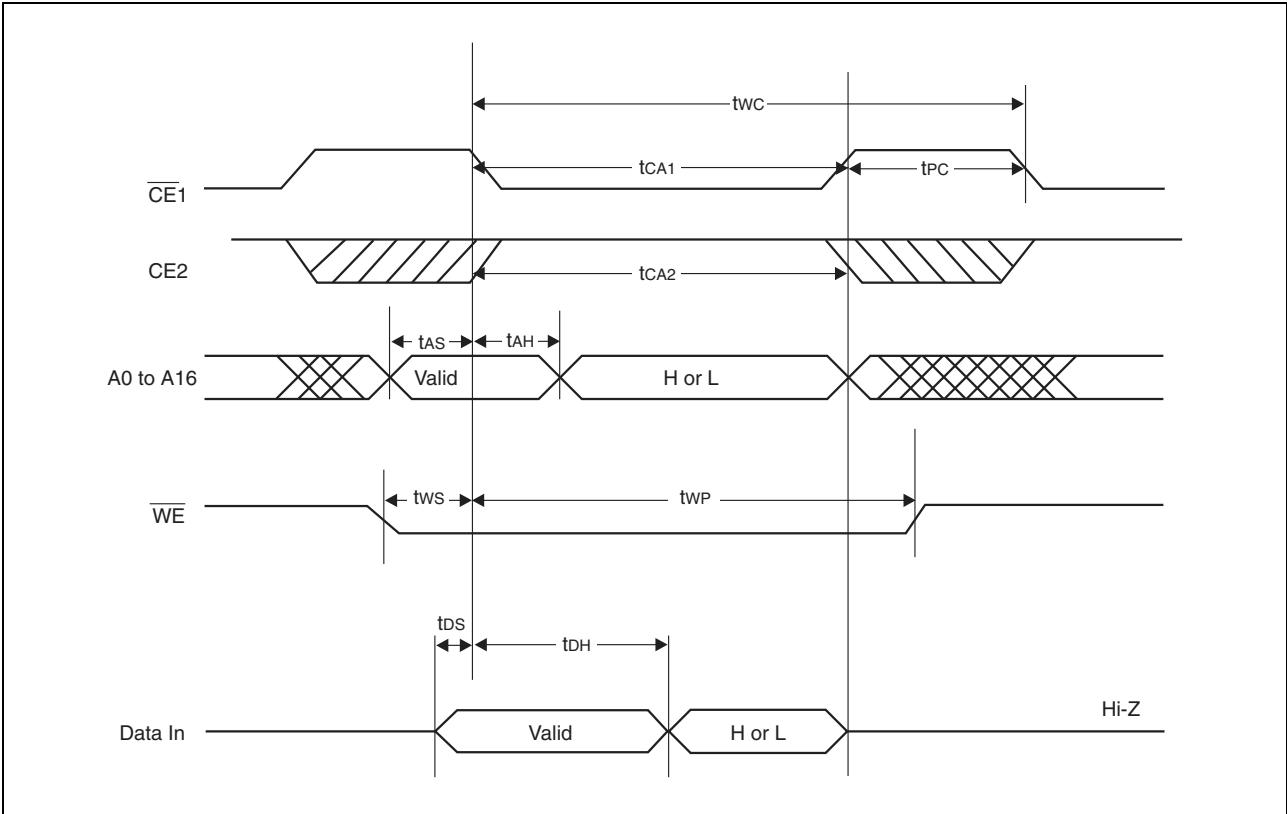
1. Read Cycle Timing ($\overline{CE1}$, CE2 Control)



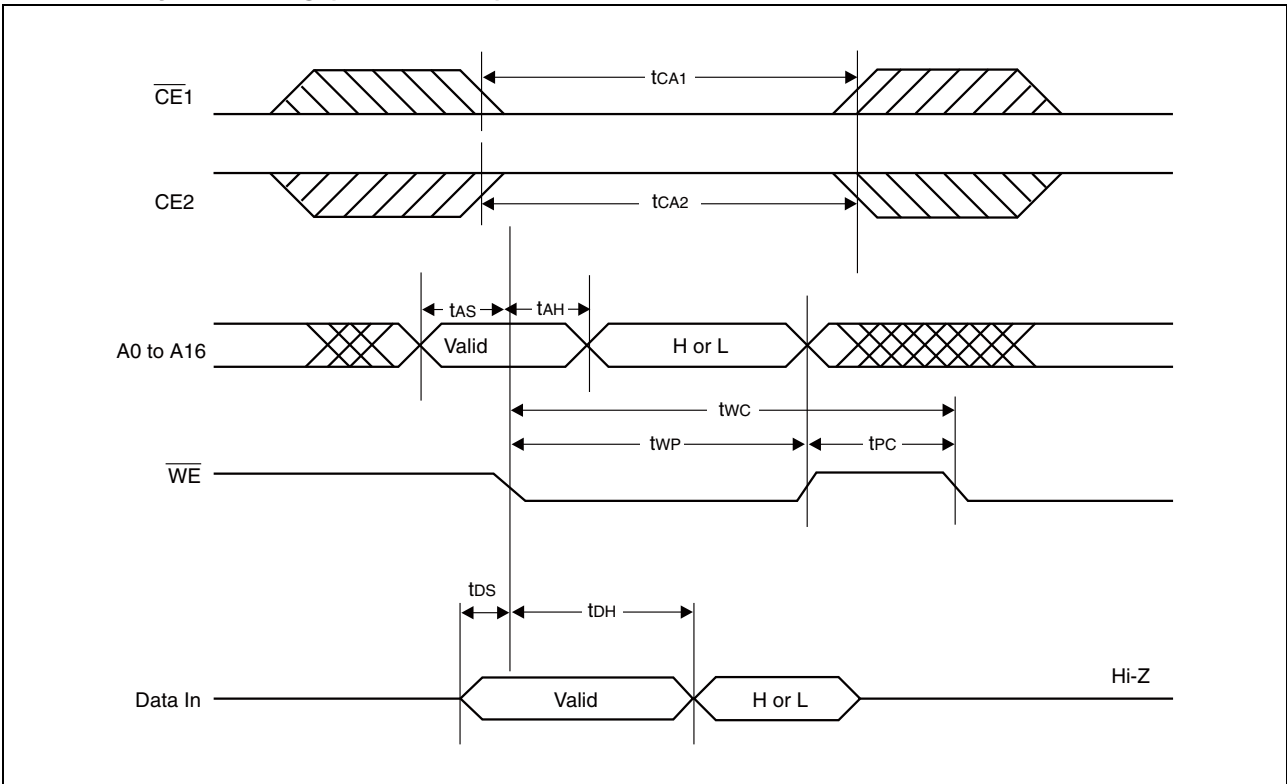
2. Read Cycle Timing (\overline{OE} Control)



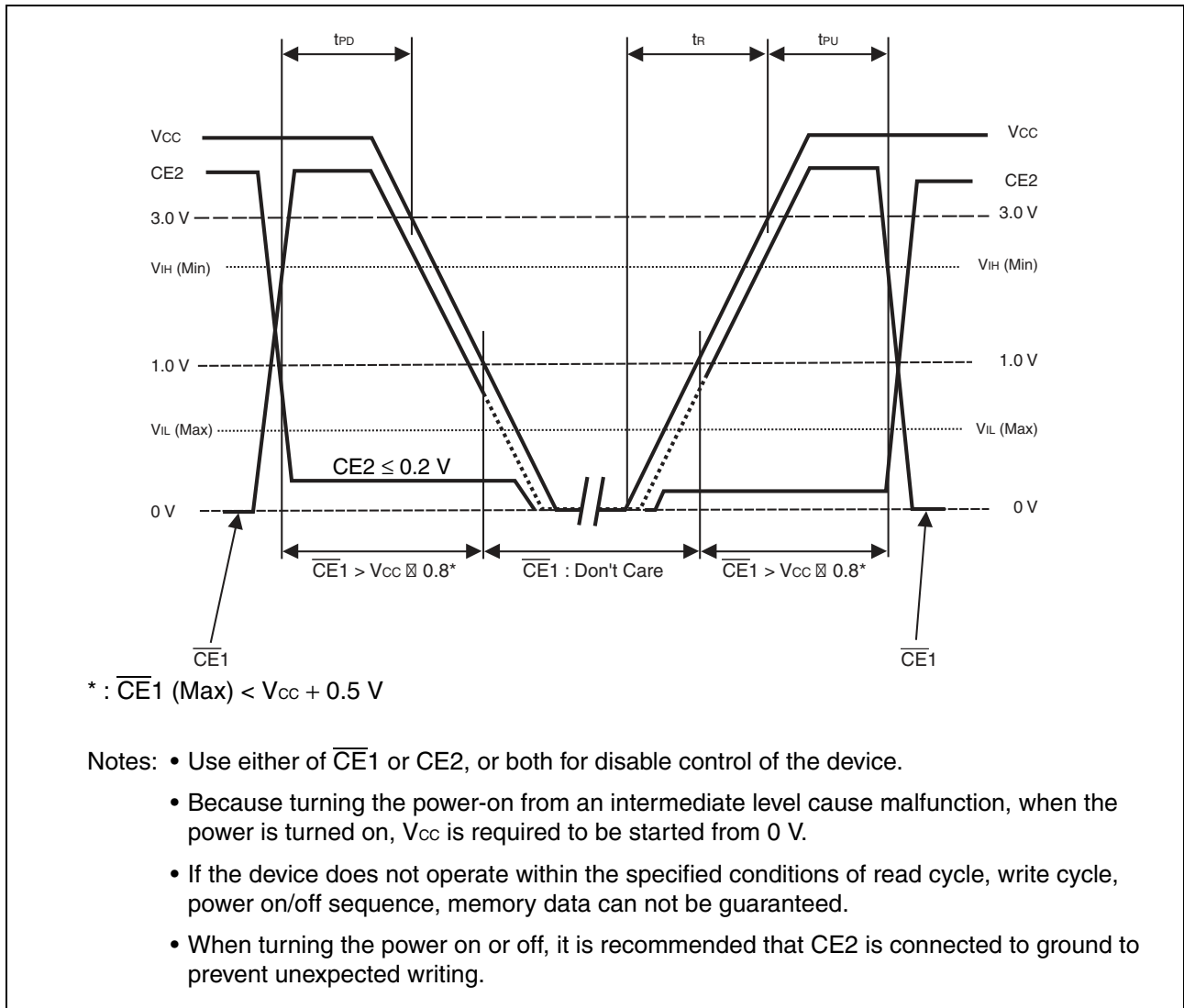
3. Write Cycle Timing ($\overline{CE1}$, CE2 Control)



4. Write Cycle Timing (\overline{WE} Control)



POWER ON/OFF SEQUENCE



(within recommended operating conditions)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CE1}$ level hold time for Power OFF	t_{PD}	85	—	—	ns
$\overline{CE1}$ level hold time for Power ON	t_{PU}	85	—	—	ns
Power supply rising time	t_R	0.05	—	200	ms

NOTES ON USE

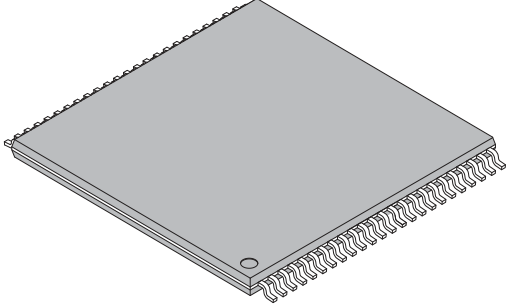
After the IR reflow completed, it is not guaranteed to hold the data written prior to the IR reflow.

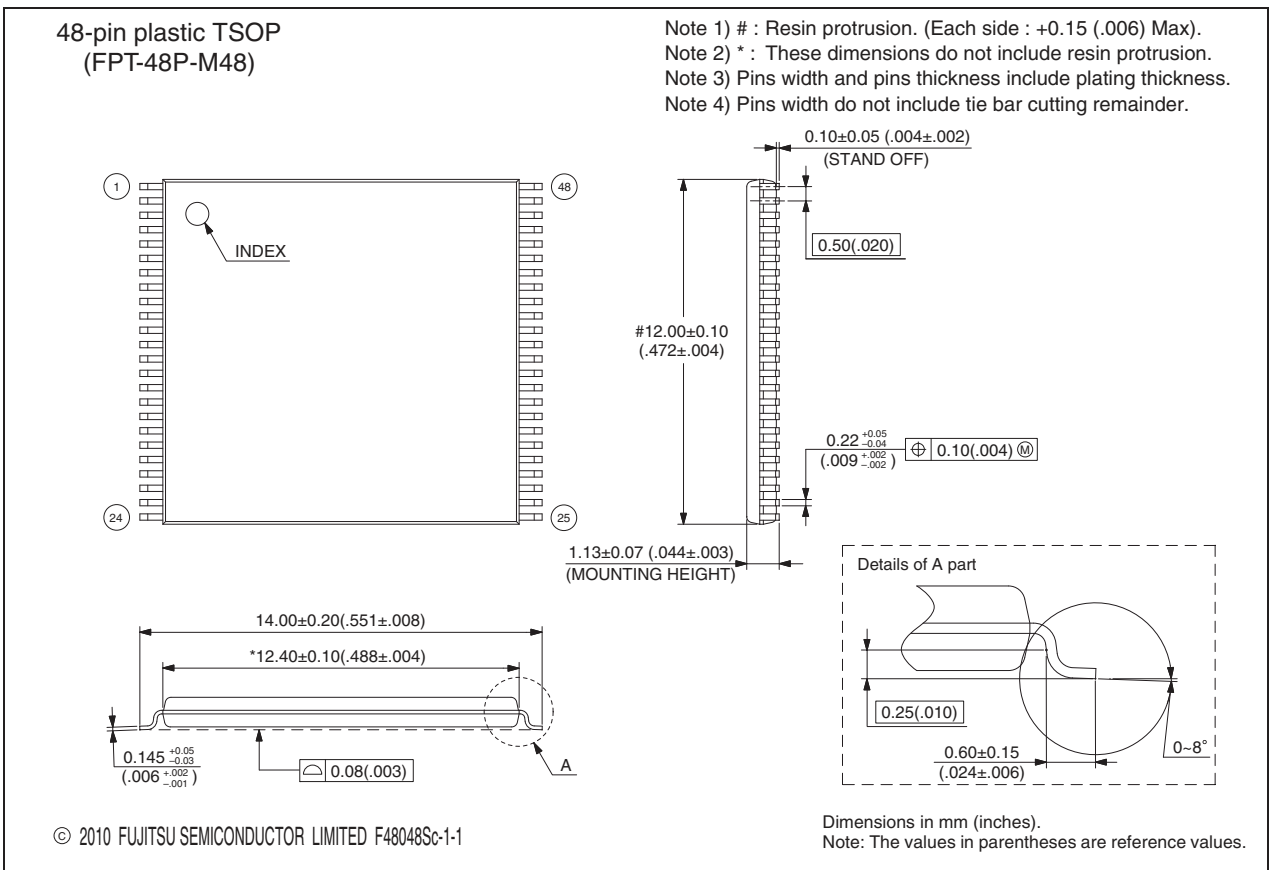
■ ORDERING INFORMATION

Part Number	Package
MB85R1001ANC-GE1	48-pin plastic TSOP(1) (FPT-48P-M48)

MB85R1001A

PACKAGE DIMENSIONS

 <p>48-pin plastic TSOP</p> <p>(FPT-48P-M48)</p>	Lead pitch	0.50 mm
	Package width × package length	12.00 mm × 12.40 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.36 g



Please check the latest package dimension at the following URL.
<http://edevice.fujitsu.com/package/en-search/>

MEMO

MEMO

MEMO

MB85R1001A

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan

Tel: +81-45-415-5858

<http://jp.fujitsu.com/fsl/en/>

For further information please contact:

North and South America

FUJITSU SEMICONDUCTOR AMERICA, INC.

1250 E. Arques Avenue, M/S 333

Sunnyvale, CA 94085-5401, U.S.A.

Tel: +1-408-737-5600 Fax: +1-408-737-5999

<http://us.fujitsu.com/micro/>

Asia Pacific

FUJITSU SEMICONDUCTOR ASIA PTE. LTD.

151 Lorong Chuan,

#05-08 New Tech Park 556741 Singapore

Tel : +65-6281-0770 Fax : +65-6281-0220

<http://sg.fujitsu.com/semiconductor/>

Europe

FUJITSU SEMICONDUCTOR EUROPE GmbH

Pittlerstrasse 47, 63225 Langen, Germany

Tel: +49-6103-690-0 Fax: +49-6103-690-122

<http://emea.fujitsu.com/semiconductor/>

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.

Rm. 3102, Bund Center, No.222 Yan An Road (E),

Shanghai 200002, China

Tel : +86-21-6146-3688 Fax : +86-21-6335-1605

<http://cn.fujitsu.com/fss/>

Korea

FUJITSU SEMICONDUCTOR KOREA LTD.

902 Kosmo Tower Building, 1002 Daechi-Dong,

Gangnam-Gu, Seoul 135-280, Republic of Korea

Tel: +82-2-3484-7100 Fax: +82-2-3484-7111

<http://kr.fujitsu.com/fsk/>

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.

10/F., World Commerce Centre, 11 Canton Road,

Tsimshatsui, Kowloon, Hong Kong

Tel : +852-2377-0226 Fax : +852-2376-3269

<http://cn.fujitsu.com/fsp/>

Specifications are subject to change without notice. For further information please contact each office.

All Rights Reserved.

The contents of this document are subject to change without notice.

Customers are advised to consult with sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU SEMICONDUCTOR device; FUJITSU SEMICONDUCTOR does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.

FUJITSU SEMICONDUCTOR assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU SEMICONDUCTOR or any third party or does FUJITSU SEMICONDUCTOR warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU SEMICONDUCTOR assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that FUJITSU SEMICONDUCTOR will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.

The company names and brand names herein are the trademarks or registered trademarks of their respective owners.

Edited: Sales Promotion Department