MCP1710

Ultra Low Quiescent Current LDO Regulator

Features

- Ultra Low 20 nA (typical) Quiescent Current
- Ultra Low Shutdown Supply Current: 0.1 nA (typical)
- 200 mA Output Current Capability for $V_R \leq 3.5V$
- 100 mA Output Current Capability for $V_R > 3.5V$
- Input Operating Voltage Range: 2.5V to 5.5V
- Standard Output Voltages (V_R):
  - 1.2V, 1.5V, 1.8V, 2.0V, 2.5V, 3.0V, 3.3V, 4.2V
- Low Dropout Voltage: 450 mV Maximum at 200 mA
- Stable with 1.0 µF Ceramic Output Capacitor
- Overcurrent Protection
- Space-Saving, 8-Lead Plastic 2 x 2 VDFN

Applications

- Energy Harvesting
- Long Life Battery-Powered Applications
- Smart Cards
- Ultra Low Consumption “Green” Products
- Portable Electronics

Description

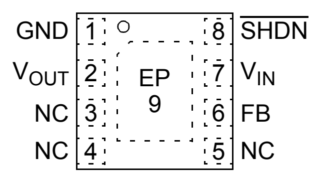
The MCP1710 is a 200 mA for $V_R \leq 3.5V$, 100 mA for $V_R > 3.5V$, Low Dropout (LDO) linear regulator that provides high-current and low-output voltages, while maintaining an ultra low 20 nA of quiescent current during device operation. In addition, the MCP1710 can be shut down for an even lower 0.1 nA (typical) supply current draw. The MCP1710 comes in eight standard, fixed output voltage versions: 1.2V, 1.5V, 1.8V, 2V, 2.5V, 3V, 3.3V and 4.2V. The 200 mA output current capability, combined with the low-output voltage capability, make the MCP1710 a good choice for new ultra long life LDO applications that have high-current demands, but require ultra low-power consumption during Sleep states.

The MCP1710 is stable using ceramic output capacitors that inherently provide lower output noise, and reduce the size and cost of the entire regulator solution. Only 1 µF (2.2 µF recommended) of output capacitance is needed to stabilize the LDO.

The MCP1710 device’s ultra low quiescent and shutdown current allows it to be paired with other ultra low-current draw devices, such as Microchip’s XLP technology devices, for a complete ultra low-power solution.

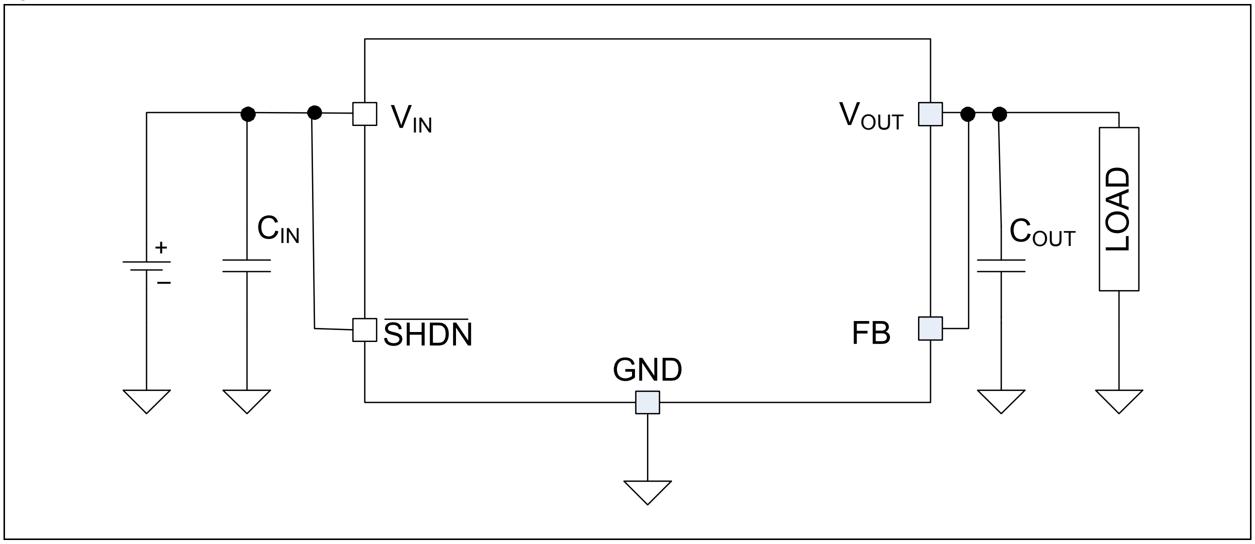
Package Type

MCP1710
2x2 VDFN*

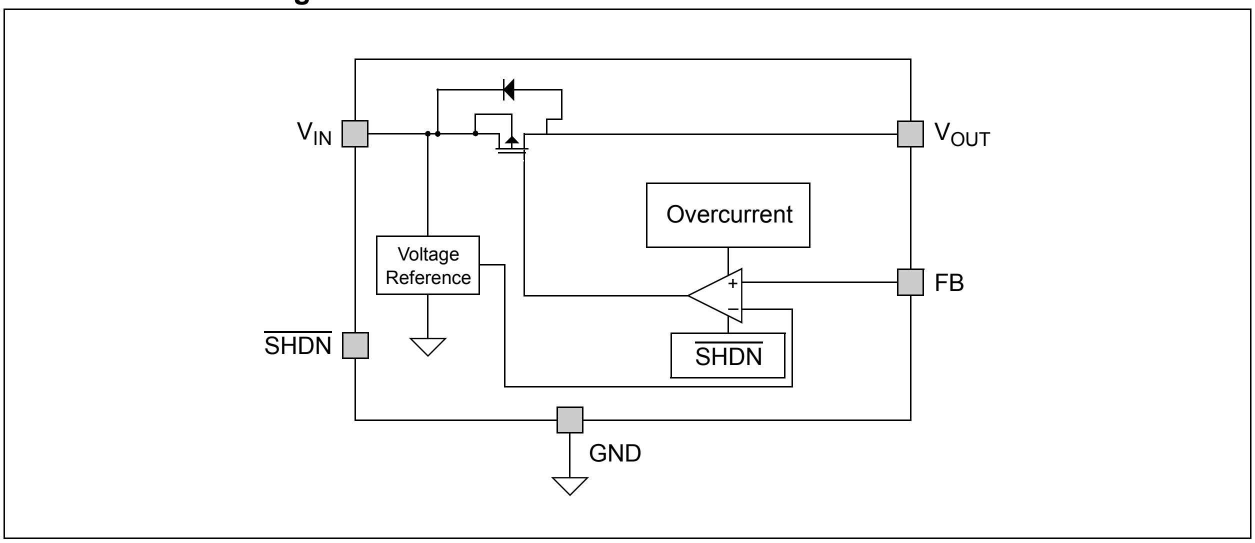


* Includes Exposed Thermal Pad (EP); see Table 3-1.

Typical Application



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Input voltage, V_{IN} 6.0V
Maximum voltage on any pin – GND .... 0.3V to 6.0V
Output short-circuit duration...Unlimited
Storage temperature .... -65°C to +150°C
Maximum junction temperature, T_J ....+150°C
Operating junction temperature, T_J...................................-40°C to +85°C
ESD protection on all pins (HBM) .... ≥ 2 kV

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R + 800$ mV (**Note 1**), I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 2.2 µF (X7R Ceramic), T_A = +25°C. **Boldface** type applies for junction temperatures T_J of **-40°C to +85°C** (**Note 4**).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Operating Voltage	V_{IN}	**2.7**	—	**5.5**	V	
		2.5	—	**5.5**	V	$V_R < 2.5V$
Output Voltage Range	V_{OUT}	**1.2**	—	**4.2**	V	
Input Quiescent Current	I_Q	—	20	—	nA	V_{IN} = 2.5V to 5.5V, I_{OUT} = 0
Input Quiescent Current for $\overline{SHDN}$ Mode	$I_{\overline{SHDN}}$	—	0.1	—	nA	$\overline{SHDN}$ = GND
Maximum Continuous Output Current	I_{OUT}	—	—	**200**	mA	$V_R \le 3.5V$
		—	—	**100**	mA	$V_R > 3.5V$
Current Limit	I_{OUT}	—	250	—	mA	$V_{OUT} = 0.9 \times V_R$, $V_R \le 3.5V$
		—	175	—	mA	$V_{OUT} = 0.9 \times V_R$, $V_R > 3.5V$
Output Voltage Regulation	V_{OUT}	**V_R – 4%**	—	**V_R + 4%**	V	$V_R < 1.8V$ (**Note 2**)
		V_R – 2%	—	**V_R + 2%**	V	$V_R \ge 1.8V$ (**Note 2**)
Line Regulation	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{IN})$	—	0.5	**4**	%	$V_{IN} = V_{IN(Min)}$ to 5.5V, $V_R \ge 1.8V$, I_{OUT} = 50 mA (**Note 1**)
		—	—	**4**	%	$V_{IN} = V_{IN(Min)}$ to 5.5V, $V_R < 1.8V$, I_{OUT} = 50 mA (**Note 1**)

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \ge V_{IN(Min)}$ and $V_{IN} \ge V_R + V_{DROPOUT(Max)}$.
2: V_R is the nominal regulator output voltage. V_R = 1.2V, 2.5V, etc.
3: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 3% below its nominal value that was measured with an input voltage of $V_{IN} = V_{OUT(Max)} + V_{DROPOUT(Max)}$.
4: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R + 800$ mV (**Note 1**), I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 2.2 µF (X7R Ceramic), T_A = +25°C. **Boldface** type applies for junction temperatures T_J of **-40°C to +85°C** (**Note 4**).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	1	**3**	%	$V_{IN} = (V_{IN(Min)} + V_{IN(Max)})/2$, I_{OUT} = 0.02 mA to 200 mA (**Note 1**)
Dropout Voltage	$V_{DROPOUT}$	—	—	**450**	mV	I_{OUT} = 200 mA, $V_R \le 3.5V$ (**Note 3**)
		—	—	**400**	mV	I_{OUT} = 100 mA, $V_R > 3.5V$ (**Note 3**)
Shutdown Input						
Logic High Input	$V_{SHDN\text{-}HIGH}$	**70**	—	—	$\%V_{IN}$	$V_{IN} = V_{IN(Min)}$ to 5.5V (**Note 1**)
Logic Low Input	$V_{SHDN\text{-}LOW}$	—	—	**30**	$\%V_{IN}$	$V_{IN} = V_{IN(Min)}$ to 5.5V (**Note 1**)
AC Performance						
Output Delay From $\overline{SHDN}$	T_{OR}	—	30	—	ms	$\overline{SHDN}$ = GND to V_{IN}, V_{OUT} = GND to 95% V_R
Output Noise	e_N	—	0.37	—	µV/√Hz	I_{OUT} = 50 mA, f = 1 kHz, C_{OUT} = 2.2 µF (X7R Ceramic), V_R = 2.5V
Power Supply Ripple Rejection Ratio	PSRR	—	22	—	dB	f = 100 Hz, I_{OUT} = 10 mA, V_{INAC} = 200 mV pk-pk, C_{IN} = 0 µF

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \ge V_{IN(Min)}$ and $V_{IN} \ge V_R + V_{DROPOUT(Max)}$.

2: V_R is the nominal regulator output voltage. V_R = 1.2V, 2.5V, etc.

3: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 3% below its nominal value that was measured with an input voltage of $V_{IN} = V_{OUT(Max)} + V_{DROPOUT(Max)}$.

4: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R + 800$ mV, (**Note 1**), I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 2.2 µF (X7R Ceramic), T_A = +25°C. **Boldface** type applies for junction temperatures, T_J of **-40°C to +85°C** (**Note 4**)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	**-40**	—	**+85**	°C	Steady state
Maximum Junction Temperature	T_J	—	—	**+150**	°C	Transient
Storage Temperature Range	T_A	**-65**	—	**+150**	°C	
Thermal Package Resistances						
Thermal Resistance, 2 x 2 VDFN-8	θ_{JA}	—	73.1	—	°C/W	JEDEC® standard FR4 board with 1 oz copper and thermal vias
	θ_{JC}	—	10.7	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF Ceramic (X7R), C_{IN} = 2.2 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

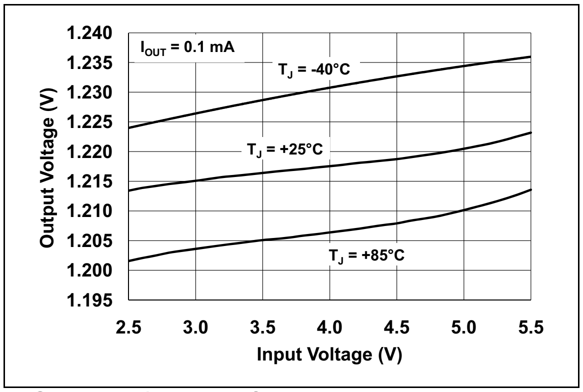


FIGURE 2-1: *Output Voltage vs. Input Voltage (V_R = 1.2V).*

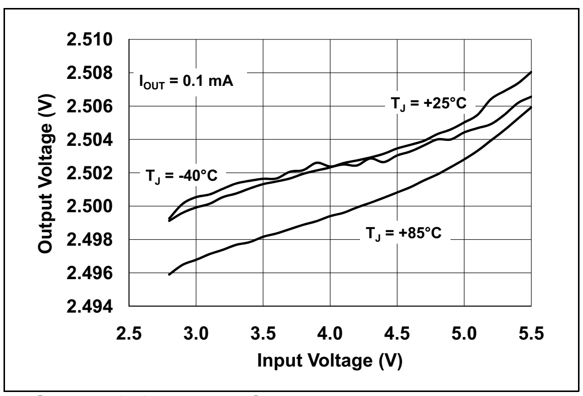


FIGURE 2-2: *Output Voltage vs. Input Voltage (V_R = 2.5V).*

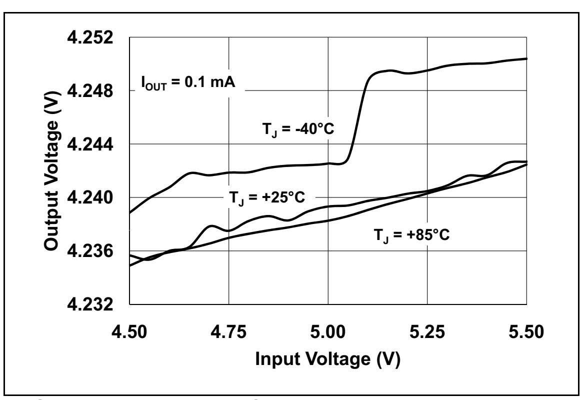


FIGURE 2-3: *Output Voltage vs. Input Voltage (V_R = 4.2V).*

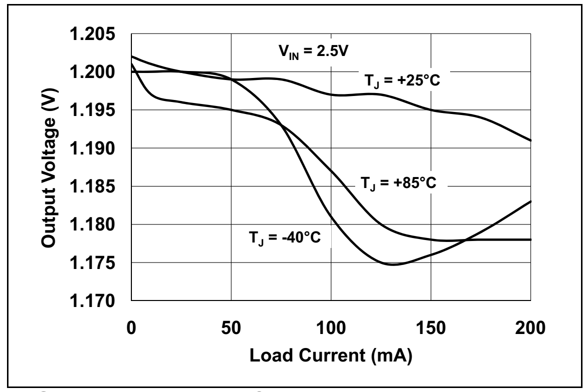


FIGURE 2-4: *Output Voltage vs. Load Current (V_R = 1.2V).*

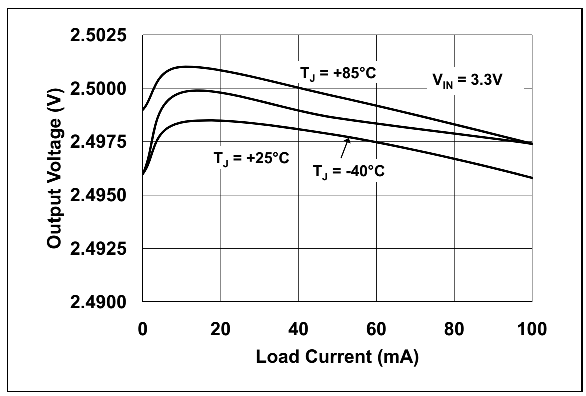


FIGURE 2-5: *Output Voltage vs. Load Current (V_R = 2.5V).*

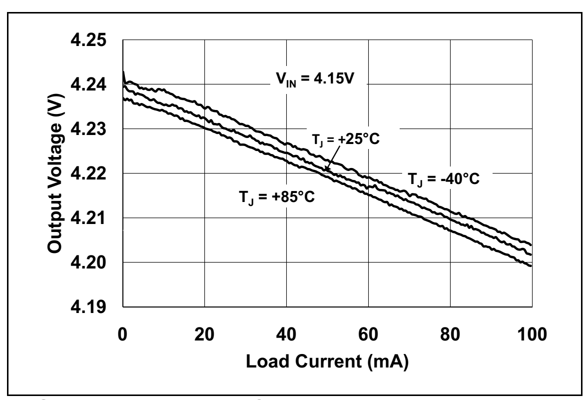


FIGURE 2-6: *Output Voltage vs. Load Current (V_R = 4.2V).*

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF Ceramic (X7R), C_{IN} = 2.2 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

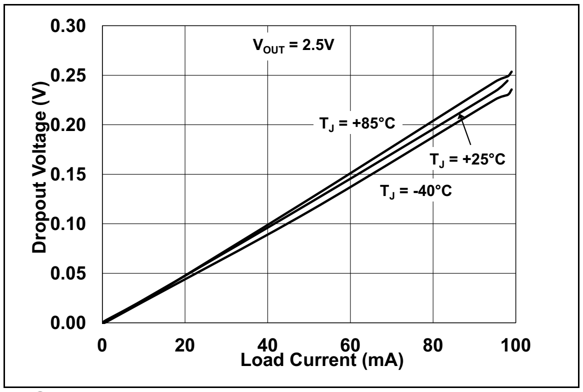


FIGURE 2-7: *Dropout Voltage vs. Load Current (V_R = 2.5V).*

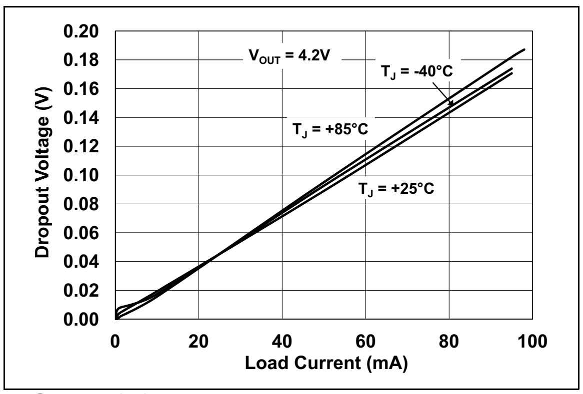


FIGURE 2-8: *Dropout Voltage vs. Load Current (V_R = 4.2V).*

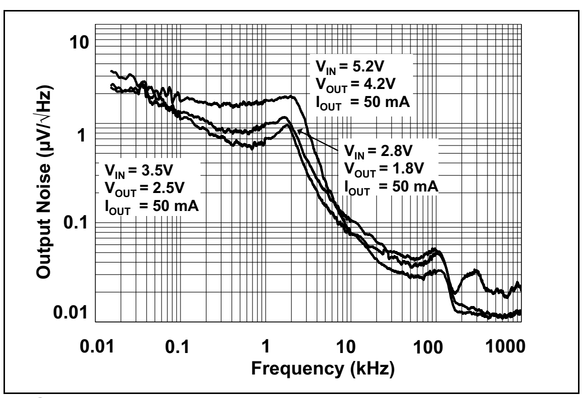


FIGURE 2-9: *Noise vs. Frequency.*

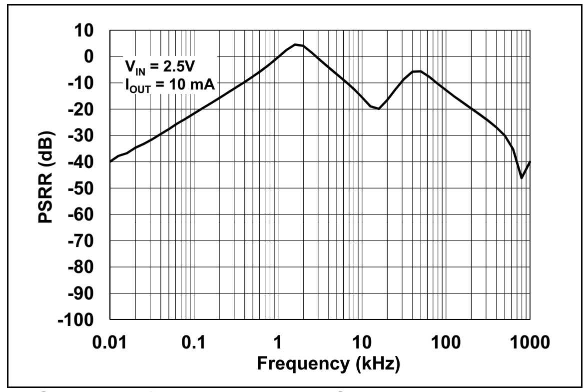


FIGURE 2-10: *Power Supply Ripple Rejection vs. Frequency (V_R = 1.2V).*

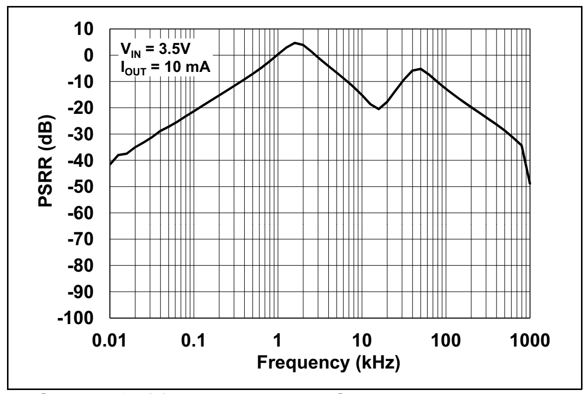


FIGURE 2-11: *Power Supply Ripple Rejection vs. Frequency (V_R = 2.5V).*

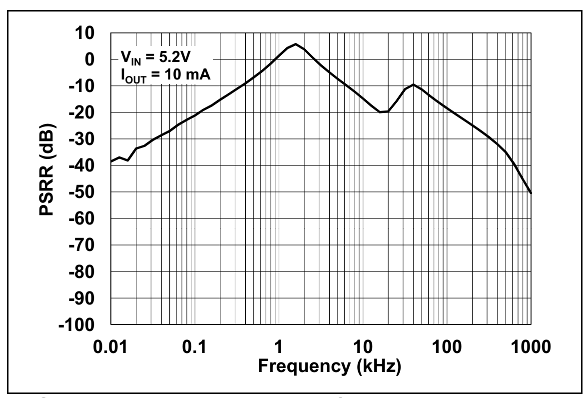


FIGURE 2-12: *Power Supply Ripple Rejection vs. Frequency (V_R = 4.2V).*

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF Ceramic (X7R), C_{IN} = 2.2 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

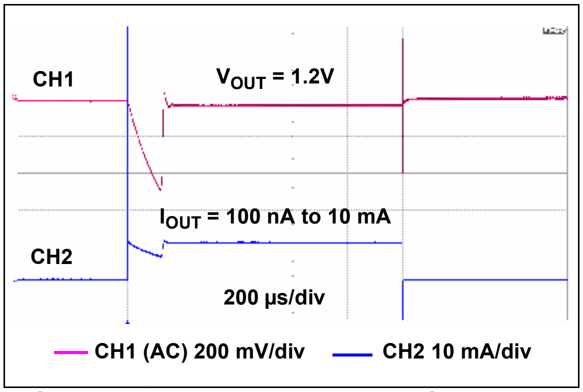


FIGURE 2-13: *Dynamic Load Step (V_R = 1.2V).*

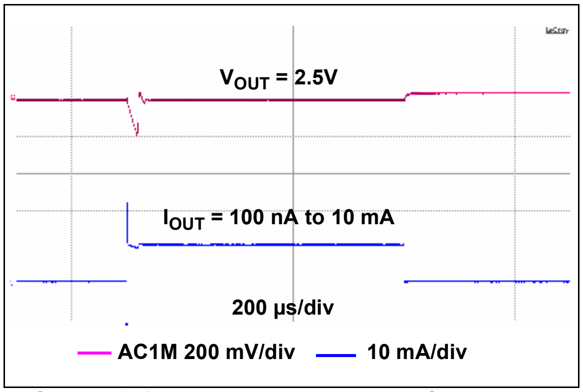


FIGURE 2-14: *Dynamic Load Step (V_R = 2.5V).*

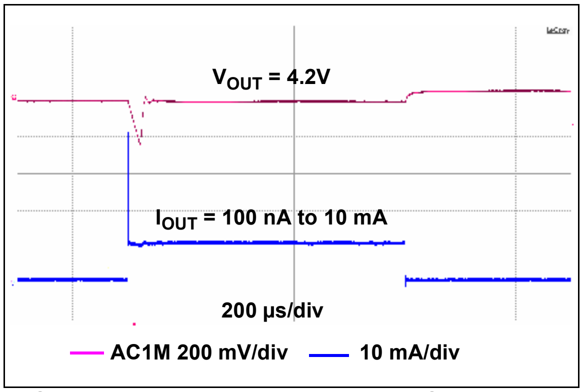


FIGURE 2-15: *Dynamic Load Step (V_R = 4.2V).*

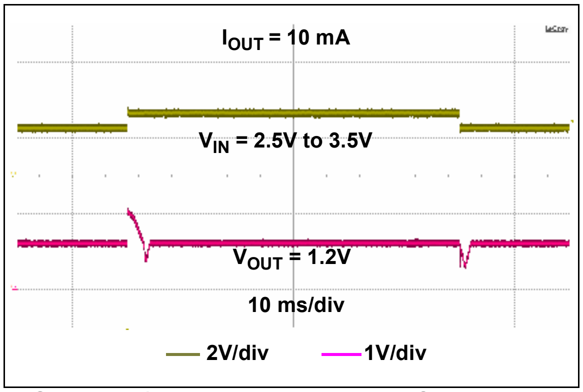


FIGURE 2-16: *Dynamic Line Step (V_R = 1.2V).*

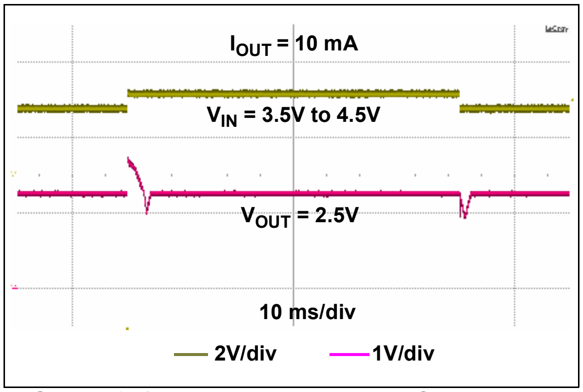


FIGURE 2-17: *Dynamic Line Step (V_R = 2.5V).*

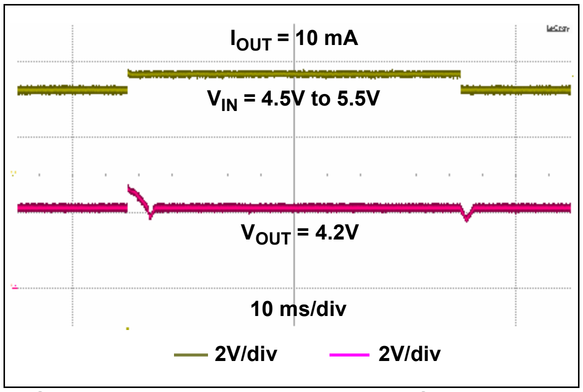


FIGURE 2-18: *Dynamic Line Step (V_R = 4.2V).*

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF Ceramic (X7R), C_{IN} = 2.2 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

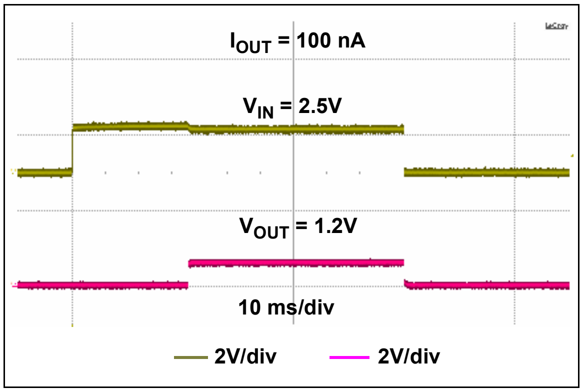


FIGURE 2-19: *Start-up from V_{IN} (V_R = 1.2V).*

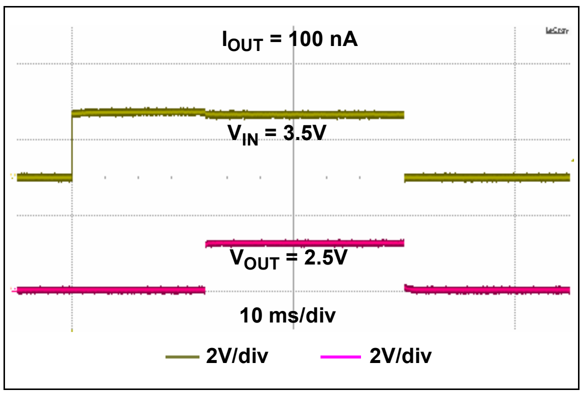


FIGURE 2-20: *Start-up from V_{IN} (V_R = 2.5V).*

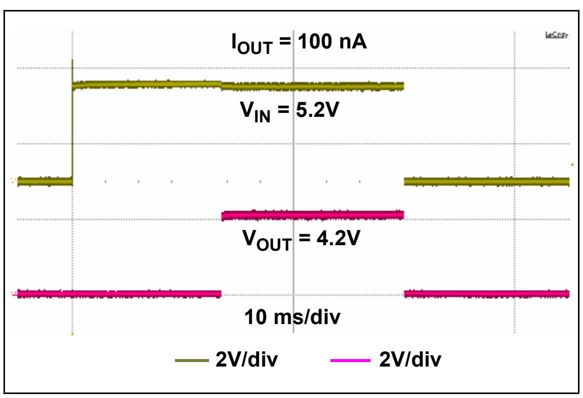


FIGURE 2-21: *Start-up from V_{IN} (V_R = 4.2V).*

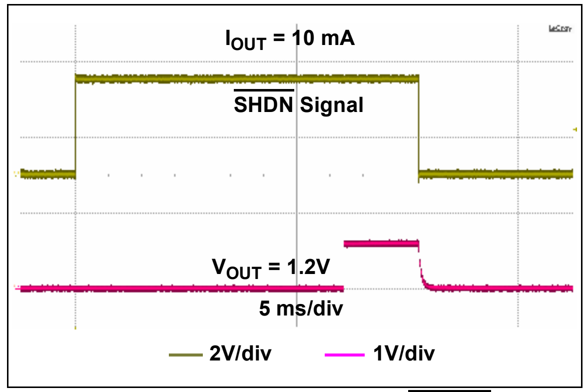


FIGURE 2-22: *Start-up from $\overline{SHDN}$ (V_R = 1.2V).*

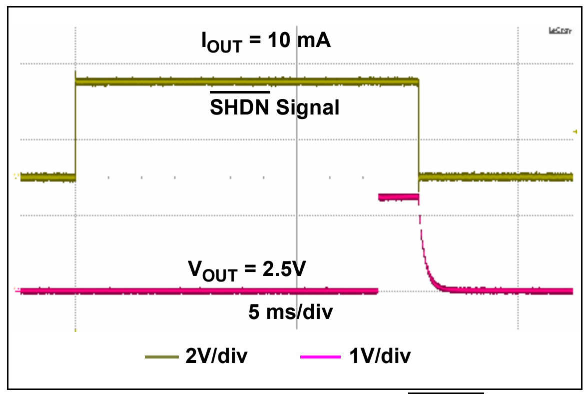


FIGURE 2-23: *Start-up from $\overline{SHDN}$ (V_R = 2.5V).*

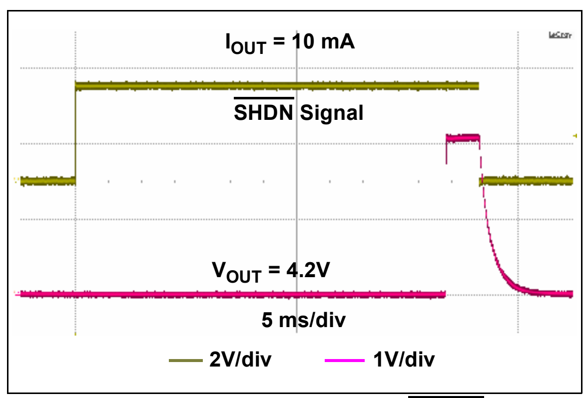


FIGURE 2-24: *Start-up from $\overline{SHDN}$ (V_R = 4.2V).*

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF Ceramic (X7R), C_{IN} = 2.2 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, $V_{IN} = V_R + 0.8V$, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

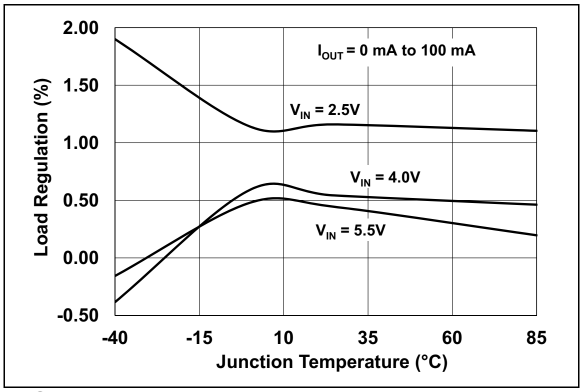


FIGURE 2-25: Load Regulation vs. Junction Temperature (V_R = 1.2V).

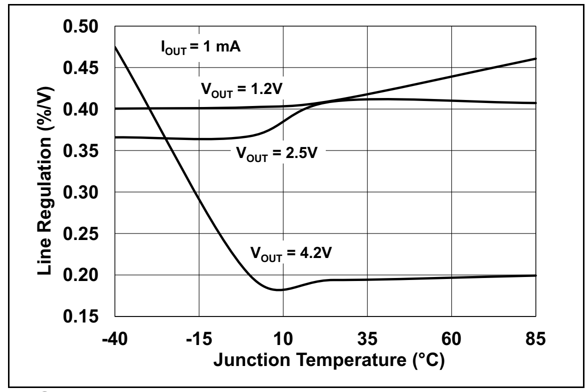


FIGURE 2-28: Line Regulation vs. Junction Temperature.

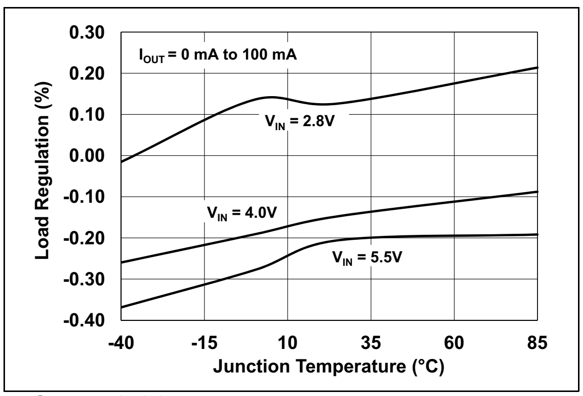


FIGURE 2-26: Load Regulation vs. Junction Temperature (V_R = 2.5V).

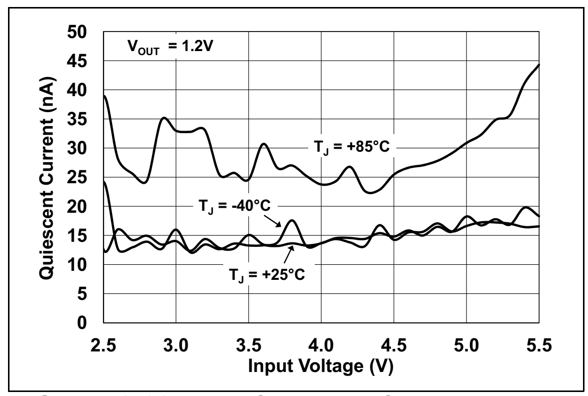


FIGURE 2-29: Quiescent Current vs. Input Voltage.

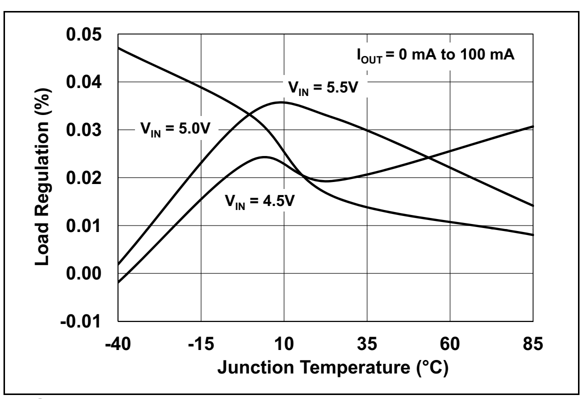


FIGURE 2-27: Load Regulation vs. Junction Temperature (V_R = 4.2V).

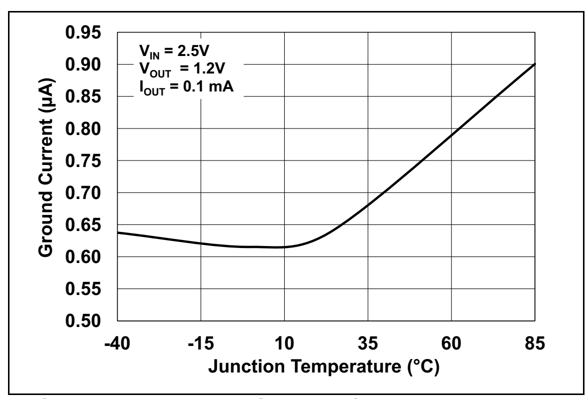


FIGURE 2-30: Ground Current vs. Junction Temperature.

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF Ceramic (X7R), C_{IN} = 2.2 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

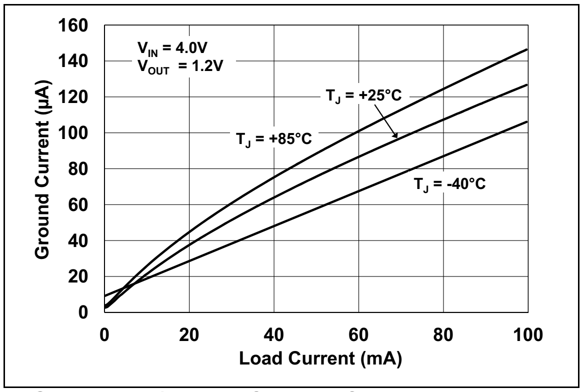


FIGURE 2-31: *Ground Current vs. Load Current.*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP1710 VDFN	Name	Description
1	GND	Ground
2	V_{OUT}	Regulated Output Voltage
3, 4, 5	NC	Not Connected pins (should either be left floated or connected to ground)
6	FB	Output Voltage Feedback Input
7	V_{IN}	Input Voltage Supply
8	$\overline{SHDN}$	Shutdown Control Input (active-low)
9	EP	Exposed Thermal Pad, Connected to GND

3.1 Ground Pin (GND)

For optimal noise and Power Supply Rejection Ratio (PSRR) performance, the GND pin of the LDO should be tied to an electrically quiet circuit ground. This will help the LDO Power Supply Rejection Ratio and noise performance. The GND pin of the LDO only conducts the ground current, so a heavy trace is not required. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower the inductance and voltage spikes caused by fast transient load currents.

3.2 Regulated Output Voltage Pin (V_{OUT})

The V_{OUT} pin is the regulated output voltage of the LDO. A minimum output capacitance of 1.0 µF is required for LDO stability. The MCP1710 is stable with ceramic, tantalum and aluminum-electrolytic capacitors. See **Section 4.2 “Output Capacitor”** for output capacitor selection guidance.

3.3 Feedback Pin (FB)

The output voltage is connected to the FB input. This sets the output voltage regulation value.

3.4 Input Voltage Supply Pin (V_{IN})

Connect the unregulated or regulated input voltage source to V_{IN}. If the input voltage source is located several inches away from the LDO, or the input source is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 1 µF to 10 µF should be sufficient for most applications (2.2 µF, typical). The type of capacitor used can be ceramic, tantalum, or aluminum-electrolytic. The low-ESR characteristics of the ceramic capacitor will yield better noise and PSRR performance at high frequency.

3.5 Shutdown Control Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the LDO output voltage on and off. When the $\overline{SHDN}$ input is at a logic high level, the LDO output voltage is enabled. When the $\overline{SHDN}$ input is pulled to a logic low level, the LDO output voltage is disabled. When the $\overline{SHDN}$ input is pulled low, the LDO enters a low quiescent current shutdown state, where the typical quiescent current is 0.1 nA.

3.6 Exposed Thermal Pad (EP)

The VDFN-8 package has an exposed thermal pad on the bottom of the package. The exposed thermal pad gives the device better thermal characteristics by providing a good thermal path to either the Printed Circuit Board (PCB), or heat sink, to remove heat from the device. The exposed pad of the package is at ground potential.

NOTES:

4.0 DEVICE OVERVIEW

The MCP1710 is a 100 mA/200 mA output current, Low Dropout (LDO) voltage regulator. The Low Dropout voltage of 450 mV maximum, at 200 mA of current, makes it ideal for battery-powered applications. The input voltage ranges from 2.5V to 5.5V. The MCP1710 adds a shutdown control input pin. The MCP1710 is available in eight standard fixed output voltage options: 1.2V, 1.5V, 1.8V, 2V, 2.5V, 3.0V, 3.3V and 4.2V. The MCP1710 uses a proprietary voltage reference and sensing scheme to maintain the ultra low 20 nA quiescent current.

4.1 Output Current and Current Limiting

The MCP1710 LDO is tested and ensured to supply a minimum of 200 mA of output current for the 1.2V to 3.5V output range, and 100 mA of output current for the 3.5V to 4.2V output range. The MCP1710 has no minimum output load, so the output load current can go to 0 mA and the LDO will continue to regulate the output voltage within the specified tolerance.

The MCP1710 also incorporates an output current limit. The current limit is set to 250 mA, typical, for the $1.2V \le V_R \le 3.5V$ range, and 175 mA, typical, for the $3.5V < V_R \le 5.5V$ range.

4.2 Output Capacitor

The MCP1710 requires a minimum output capacitance of 1 µF for output voltage stability. Ceramic capacitors are recommended because of their size, cost and robust environmental qualities.

Aluminum-electrolytic and tantalum capacitors can be used on the LDO output as well. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials, X7R and X5R, have low-temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 50 mΩ.

4.3 Input Capacitor

Low input source impedance is necessary for the LDO output to operate properly. When operating from batteries, or in applications with long lead length (>10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 µF to 4.7 µF is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides a low-impedance source of current for the LDO to use for dynamic load changes. This allows the LDO to respond quickly to the output load step. For good step response performance, the input capacitor should be of equivalent or higher value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO, as well as the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

4.4 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is an active-low input signal that turns the LDO on and off. The $\overline{SHDN}$ threshold is a percentage of the input voltage. The maximum input low logic level is 30% of V_{IN} and the minimum high logic level is 70% of V_{IN}.

On the rising edge of the $\overline{SHDN}$ input, the shutdown circuitry has a 30 ms (typical) delay before allowing the LDO output to turn on. This delay helps to reject any false turn-on signal or noise on the $\overline{SHDN}$ input signal. After the 30 ms delay, the LDO output enters its current-limited soft start period as it rises from 0V to its final regulation value. If the $\overline{SHDN}$ input signal is pulled low during the 30 ms delay period, the timer will be reset and the delay time will start over again on the next rising edge of the $\overline{SHDN}$ input. The total time from the $\overline{SHDN}$ input going high (turn on) to the LDO output being in regulation is typically 30 ms. See Figure 4-1 for a timing diagram of the $\overline{SHDN}$ input.

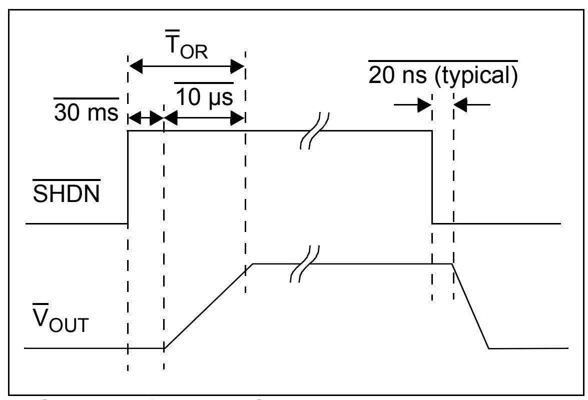


FIGURE 4-1: Shutdown Input Timing Diagram.

4.5 Dropout Voltage

Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 3% below the nominal value that was measured with a V_R + 0.8V differential applied. The MCP1710 LDO has a Low Dropout voltage specification of 450 mV for the $1.2V \le V_R \le 3.5V$ range (typical) at 200 mA out, and 400 mV for the $3.5V < V_R \le 5.5V$ range (typical) at 100 mA out. See **Section 1.0 "Electrical Characteristics"** for maximum dropout voltage specifications.

NOTES:

5.0 APPLICATION CIRCUITS/ISSUES

5.1 Typical Application

The MCP1710 is used for applications that require ultra low quiescent current draw.

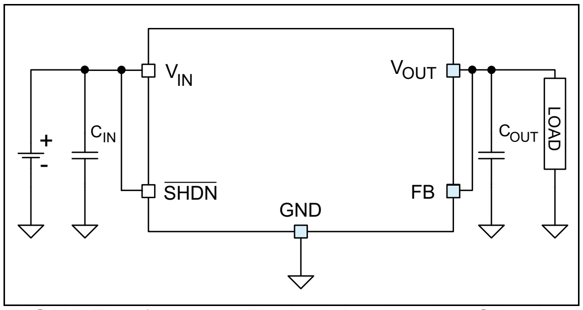


FIGURE 5-1: *Typical Application Circuit.*

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation within the MCP1710 is a function of input voltage, output voltage, output current and quiescent current. Equation 5-1 can be used to calculate the internal power dissipation for the LDO.

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

Where:

P_{LDO} = Internal power dissipation of the LDO pass device

$V_{IN(MAX)}$ = Maximum input voltage

$V_{OUT(MIN)}$ = LDO minimum output voltage

$I_{OUT(MAX)}$ = Maximum output current

In addition to the LDO pass element power dissipation, there is power dissipation within the MCP1710 as a result of quiescent or ground current. The power dissipation as a result of the ground current can be calculated using Equation 5-2:

EQUATION 5-2:

$$P_{I(GND)} = V_{IN(MAX)} \times I_{GND}$$

Where:

$P_{I(GND)}$ = Power dissipation due to the quiescent current of the LDO

$V_{IN(MAX)}$ = Maximum input voltage

I_{GND} = Current flowing in the GND pin

The total power dissipated within the MCP1710 is the sum of the power dissipated in the LDO pass device and the $P(I_{GND})$ term. Because of the CMOS construction, the typical I_{GND} for the MCP1710 is 200 µA at full load. Operating at a maximum V_{IN} of 5.5V results in a power dissipation of 1.1 mW. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1710 is +85°C. To estimate the internal junction temperature of the MCP1710, the total internal power dissipation is multiplied by the thermal resistance from junction-to-ambient ($R\theta_{JA}$) of the device. The thermal resistance from junction-to-ambient for the 2 x 2 VDFN-8 package is estimated at 73.1°C/W.

EQUATION 5-3:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{A(MAX)}$$

Where:

$T_{J(MAX)}$ = Maximum continuous junction temperature

P_{TOTAL} = Total power dissipation of the device

$R\theta_{JA}$ = Thermal resistance from junction to ambient

$T_{A(MAX)}$ = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. Equation 5-4 can be used to determine the package maximum internal power dissipation.

EQUATION 5-4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

Where:

$P_{D(MAX)}$ = Maximum power dissipation of the device

$T_{J(MAX)}$ = Maximum continuous junction temperature

$T_{A(MAX)}$ = Maximum ambient temperature

$R\theta_{JA}$ = Thermal resistance from junction-to-ambient

EQUATION 5-5:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

$T_{J(RISE)}$	=	Rise in the device’s junction temperature over the ambient temperature
$P_{D(MAX)}$	=	Maximum power dissipation of the device
$R\theta_{JA}$	=	Thermal resistance from junction-to-ambient

EQUATION 5-6:

$$T_J = T_{J(RISE)} + T_A$$

T_J	=	Junction temperature
$T_{J(RISE)}$	=	Rise in the device’s junction temperature over the ambient temperature
T_A	=	Ambient temperature

5.3 Typical Application Examples

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

5.3.1 POWER DISSIPATION EXAMPLES

EXAMPLE 5-1:

Package	
Package Type =	2 x 2 VDFN-8
Input Voltage	
V_{IN} =	3.3V ± 5%
LDO Output Voltage and Current	
V_{OUT} =	2.5V
I_{OUT} =	200 mA
Maximum Ambient Temperature	
$T_{A(MAX)}$ =	+60°C
Internal Power Dissipation	
$P_{LDO(MAX)}$ =	$(V_{IN(MAX)} – V_{OUT(MIN)})$ x $I_{OUT(MAX)}$
P_{LDO} =	((3.3V x 1.05) – (2.5V x 0.975)) x 200 mA
P_{LDO} =	0.206 Watts

5.3.1.1 Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance, from junction-to-ambient, for the application. The thermal resistance, from junction-to-ambient ($R\theta_{JA}$), is derived from the EIA/JEDEC standards for measuring thermal resistance. The EIA/JEDEC specification is JESD51. The standard describes the test method and board specifications for measuring the thermal resistance from junction-to-ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, *“A Method to Determine How Much Power a SOT23 Can Dissipate in an Application”* (DS00792), for more information regarding this subject.

EXAMPLE 5-2:

$T_{J(RISE)}$ =	P_{TOTAL} x $R\theta_{JA}$
$T_{J(RISE)}$ =	0.206W x 73.1°C/W
$T_{J(RISE)}$ =	15.1°C

5.3.1.2 Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below:

EXAMPLE 5-3:

T_J =	$T_{J(RISE)}$ + $T_{A(MAX)}$
T_J =	15.1°C + 60.0°C
T_J =	75.1°C

5.3.1.3 Maximum Package Power Dissipation at +60°C Ambient Temperature

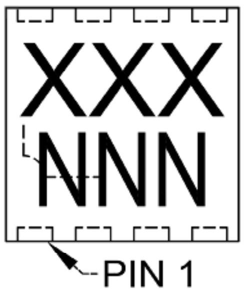
EXAMPLE 5-4:

2x2 VDFN-8 (73.1°C/W $R\theta_{JA}$):	
$P_{D(MAX)}$ =	(85°C – 60°C)/73.1°C/W
$P_{D(MAX)}$ =	0.342W

6.0 PACKAGING INFORMATION

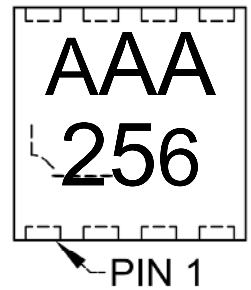
6.1 Package Marking Information

8-Lead VDFN (2 x 2 x 0.9)



Part Number	Code
MCP1710T-12I/LZ	AAA
MCP1710T-15I/LZ	AAF
MCP1710T-18I/LZ	AAB
MCP1710T-20I/LZ	AAG
MCP1710T-25I/LZ	AAC
MCP1710T-30I/LZ	AAH
MCP1710T-33I/LZ	AAD
MCP1710T-42I/LZ	AAE

Example

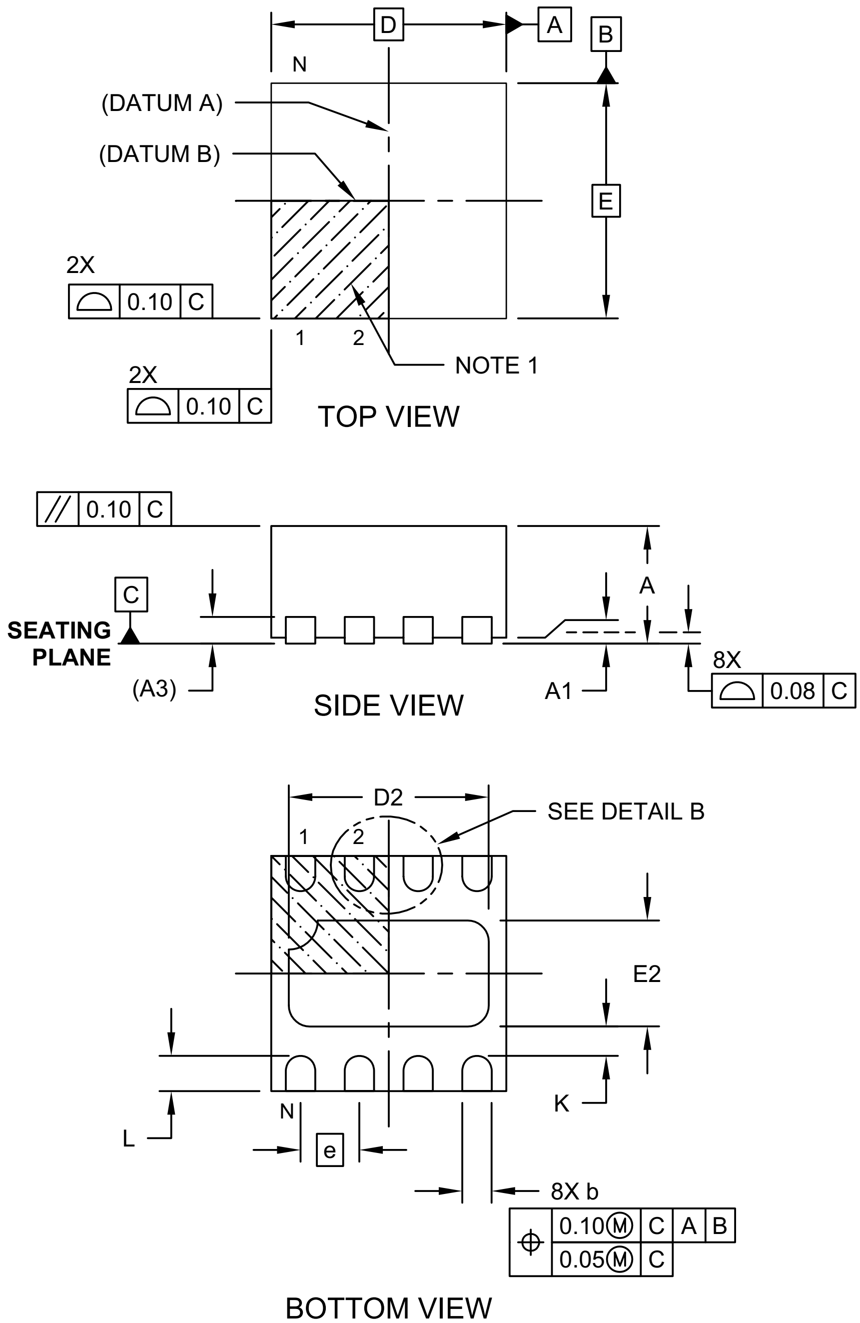


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8- Lead Very Thin Dual Flatpack No-Lead (LZ) – 2x2x0.9 mm Body [VDFN]

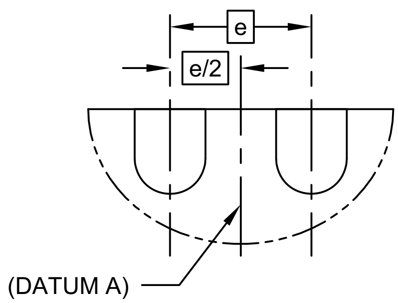
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

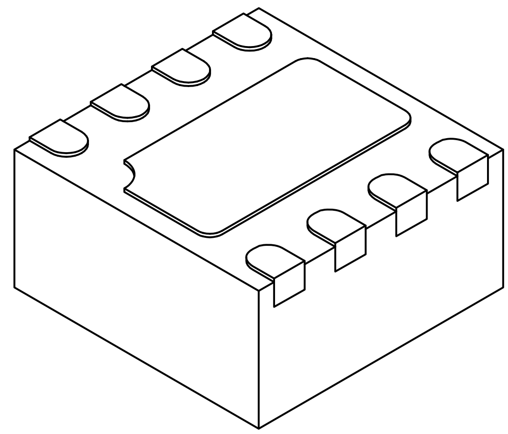


Microchip Technology Drawing C04-198B Sheet 1 of 2

8- Lead Very Thin Dual Flatpack No-Lead (LZ) – 2x2x0.9 mm Body [VDFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness (REF)	(A3)		0.20 (REF)	
Overall Width	D		2.00 BSC	
Exposed Pad Width	D2	1.55	1.70	1.80
Overall Length	E		2.00 BSC	
Exposed Pad Length	E2	0.75	0.90	1.00
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.20	0.30	0.40
Terminal-to-Exposed Pad	K	0.20	-	-

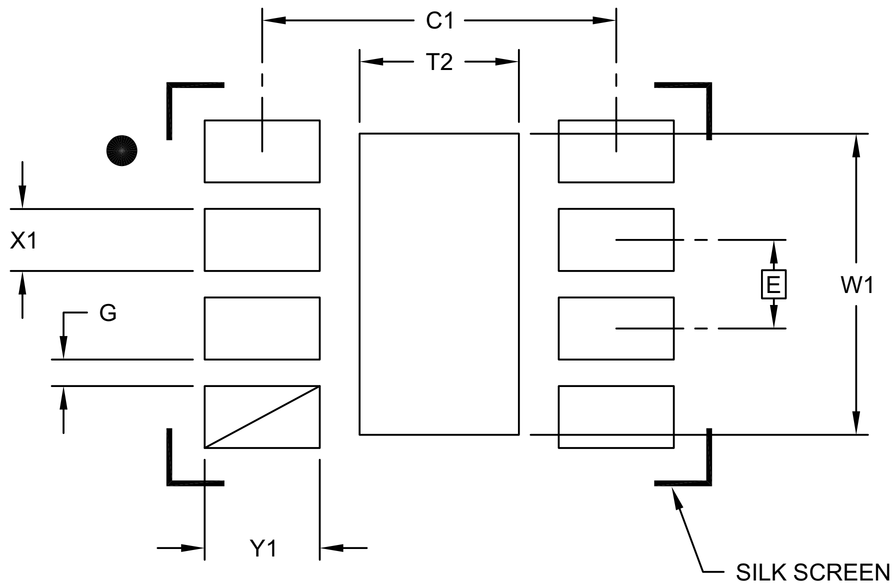
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-198B Sheet 2 of 2

8-Lead Plastic Very Thin Flat, No Lead Package (LZ) - 2x2 mm Body [VDFN] With 0.55mm Contact Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W1			1.70
Optional Center Pad Length	T2			0.90
Contact Pad Spacing	C1		2.00	
Contact Pad Width (X28)	X1			0.35
Contact Pad Length (X28)	Y1			0.65
Distance Between Pads	G	0.15		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2198A

APPENDIX A: REVISION HISTORY

Revision D (May 2015)

- Changed minimum input voltage to 2.5V.
- Updated the **Package Type** figure.
- Updated the **AC/DC Characteristics** table.
- Updated **Section 3.0 "Pin Description"**.

Revision C (July 2014)

The following is the list of modifications:

1. Added the information related to the 1.5V, 2V and 3V devices throughout the document.
2. Updated package markings and drawings in **Section 6.0 "Packaging Information"**.
3. Minor typographical changes.

Revision B (November 2012)

- Updated the performance curves for Dynamic Load Step, Dynamic Line Step, Startup from V_{IN}, and Startup from $\overline{SHDN}$ (Figure 2-13-Figure 2-24).

Revision A (September 2012)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	T(1)	-XX	X/	XX
Device	Tape and Reel	Output Voltage	Temp.	Package

Device:	MCP1710T: 200 mA Low Dropout Regulator Tape and Reel
Tape and Reel Option:	Blank = Standard Packaging (tube or tray) T = Tape and Reel(1)
Output Voltage*:	12 = 1.2V “Standard” 15 = 1.5V “Standard” 18 = 1.8V “Standard” 20 = 2.0V “Standard” 25 = 2.5V “Standard” 30 = 3.0V “Standard” 33 = 3.3V “Standard” 42 = 4.2V “Standard” *Contact factory for other output voltage options
Temperature:	I = -40°C to +85°C (Industrial)
Package Type:	LZ = Very Thin Dual Flatpack, No Lead (VDFN), 8-Lead

Examples:

a) MCP1710T-12I/LZ: Tape and Reel, 1.2V Output Voltage, Industrial Temp., 8-LD VDFN Package

b) MCP1710T-15I/LZ: Tape and Reel, 1.5V Output Voltage, Industrial Temp., 8-LD VDFN Package

c) MCP1710T-18I/LZ: Tape and Reel, 1.8V Output Voltage, Industrial Temp., 8-LD VDFN Package

d) MCP1710T-20I/LZ: Tape and Reel, 2.0V Output Voltage, Industrial Temp., 8-LD VDFN Package

e) MCP1710T-25I/LZ: Tape and Reel, 2.5V Output Voltage, Industrial Temp., 8-LD VDFN Package

f) MCP1710T-30I/LZ: Tape and Reel, 3.0V Output Voltage, Industrial Temp., 8-LD VDFN Package

g) MCP1710T-33I/LZ: Tape and Reel, 3.3V Output Voltage, Industrial Temp., 8-LD VDFN Package

h) MCP1710T-42I/LZ: Tape and Reel, 4.2V Output Voltage, Industrial Temp., 8-LD VDFN Package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package y with the Tape and Reel option.

ISBN: 978-1-63277-446-0

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