OptiMOS™-P Power-Transistor

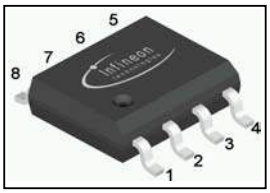
Features

- P-Channel
- Enhancement mode
- Logic level
- 150°C operating temperature
- Avalanche rated
- d*v*/d*t* rated
- Ideal for fast switching buck converter

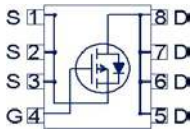
Product Summary

V_{DS}	-30	V
$R_{DS(on),max}$	20	mΩ
I_D	-9.1	A

P-DSO-8



Type	Package	Marking
BSO200P03S	P-DSO-8	200P3S



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			≤10 secs	steady state	
Continuous drain current	I_D	T_A=25 °C[1)]	-9.1	-7.4	A
		T_A=70 °C[1)]	-7.3	-5.9	
Pulsed drain current	$I_{D,pulse}$	T_A=25 °C[2)]	-37		
Avalanche energy, single pulse	E_{AS}	I_D=-9.1 A, R_{GS}=25 Ω	98		mJ
Reverse diode d*v*/d*t*	d*v*/d*t*	I_D=-9.1 A, V_{DS}=20 V, d*i*/d*t*=-200 A/µs, $T_{j,max}$=150 °C	-6		kV/µs
Gate source voltage	V_{GS}		±25		V
Power dissipation	P_{tot}	T_A=25 °C[1)]	2.36	1.56	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - soldering point	R_{thJS}		-	-	35	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, $t_p \leq 10$ s	-	-	110	
		minimal footprint, steady state	-	-	150	
		6 cm^2 cooling area[1)], $t_p \leq 10$ s	-	-	53	
		6 cm^2 cooling area[1)], steady state	-	-	80	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=-250µA	-30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, I_D=-100 µA	-1	-1.5		
Zero gate voltage drain current	I_{DSS}	V_{DS}=-30 V, V_{GS}=0 V, T_j=25 °C	-	-0.1	-1	µA
		V_{DS}=-30 V, V_{GS}=0 V, T_j=125 °C	-	-10	-100	
Gate-source leakage current	I_{GSS}	V_{GS}=-25 V, V_{DS}=0 V	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=-10 V, I_D=-9.1 A	-	16.7	20.0	
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=-7.3 A	11	21	-	S

[1)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

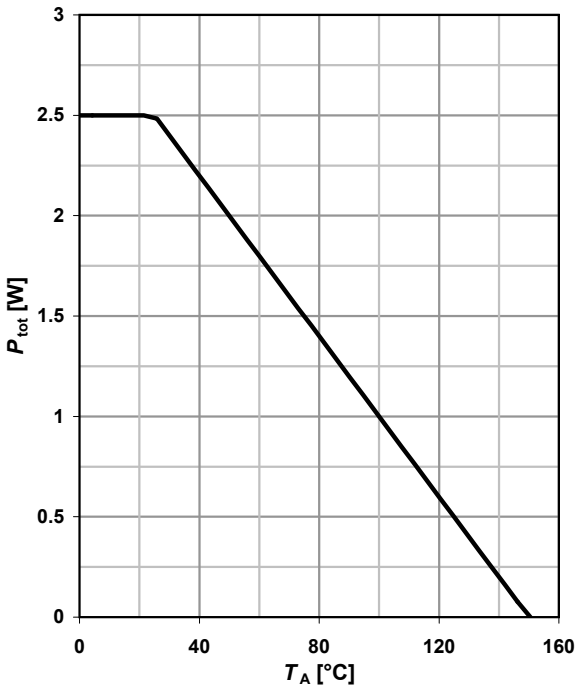
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=-25 V, f=1 MHz	-	1750	2330	pF
Output capacitance	C_{oss}		-	470	625	
Reverse transfer capacitance	C_{rss}		-	390	580	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-15 V, V_{GS}=-10 V, I_D=-1 A, R_G=6 Ω	-	10	53	ns
Rise time	t_r		-	11	17	
Turn-off delay time	$t_{d(off)}$		-	42	63	
Fall time	t_f		-	33	50	
Gate Charge Characteristics[3]						
Gate to source charge	Q_{gs}	V_{DD}=-24 V, I_D=9.1 A, V_{GS}=0 to -10 V	-	-4.8	-6.4	nC
Gate charge at threshold	$Q_{g(th)}$		-	-2.6	-3.5	
Gate to drain charge	Q_{gd}		-	-14		
Switching charge	Q_{sw}		-	-16	-24	
Gate charge total	Q_g		-	-40	-54	
Gate plateau voltage	$V_{plateau}$		-	-2.7	-	V
Output charge	Q_{oss}	V_{DD}=-15 V, V_{GS}=0 V	-	-14	-19	
Reverse Diode						
Diode continous forward current	I_S	T_A=25 °C	-	-	-2.1	A
Diode pulse current	$I_{S,pulse}$		-	-	-36.5	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=-9.1 A, T_j=25 °C	-	-0.88	-1.2	V
Reverse recovery time	t_{rr}	V_R=15 V, I_F=-9.1 A, di_F/dt=100 A/µs	-	19	24	ns
Reverse recovery charge	Q_{rr}		-	9	11	nC

[2] See figure 3

[3] See figure 16 for gate charge parameter definition

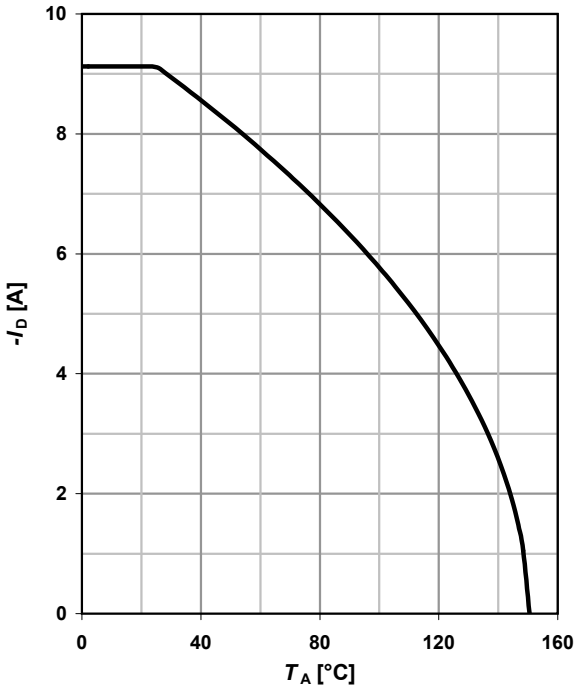
1 Power dissipation

$P_{tot}=f(T_A)$; $t_p \leq 10$ s



2 Drain current

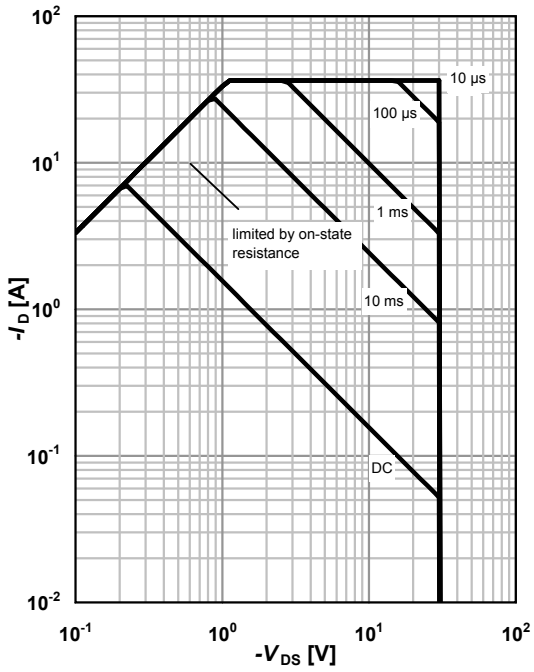
$I_D=f(T_A)$; $|V_{GS}| \geq 10$ V; $t_p \leq 10$ s



3 Safe operating area

$I_D=f(V_{DS})$; $T_A=25$ °C[1)]; $D=0$

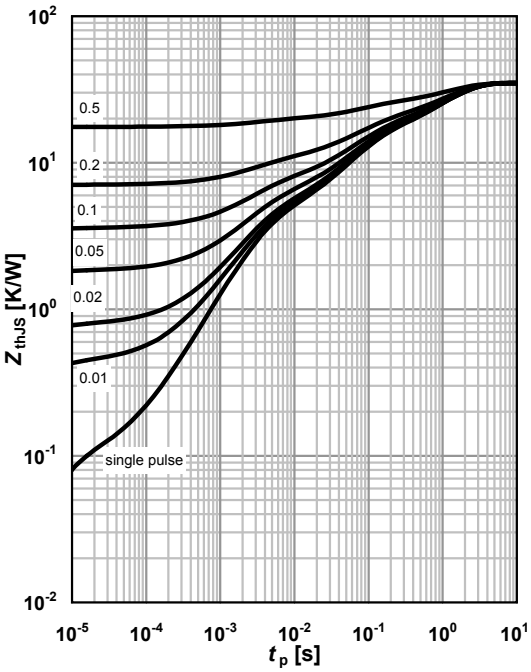
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJS}=f(t_p)$

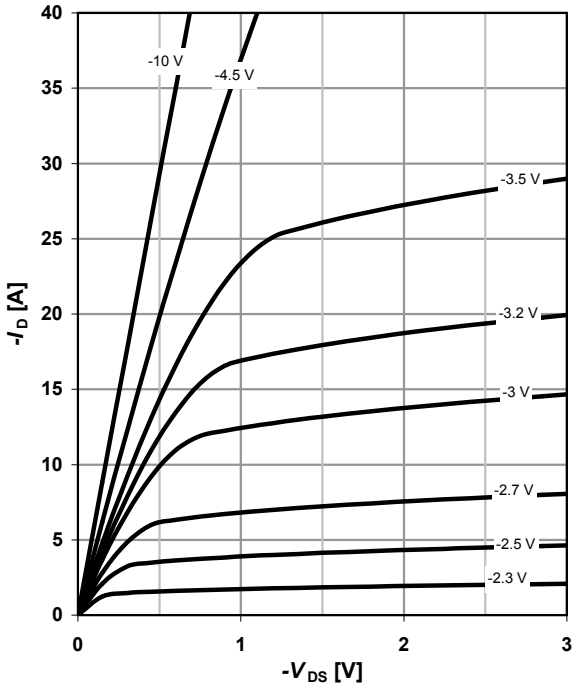
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

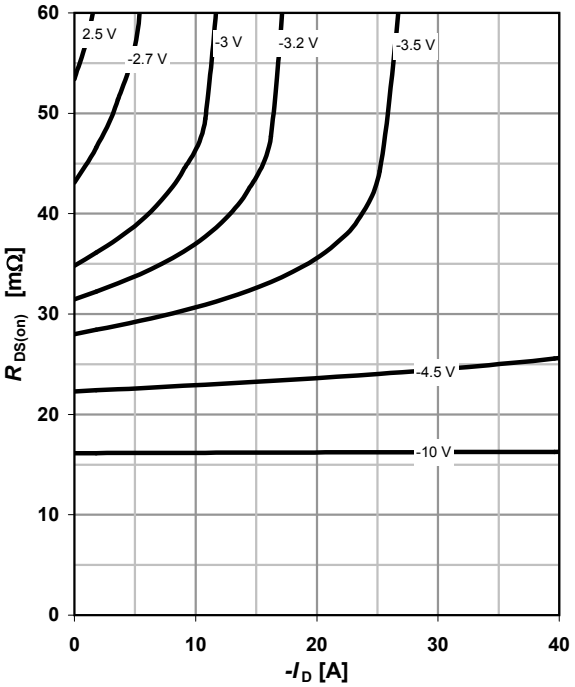
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

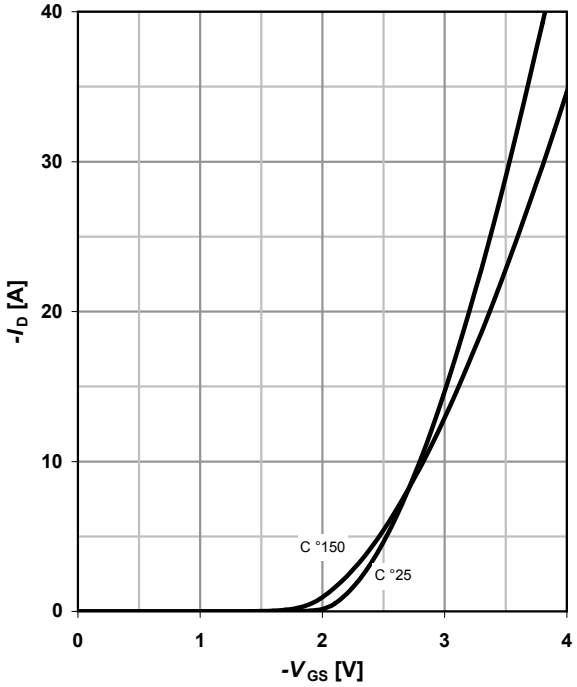
parameter: V_{GS}



7 Typ. transfer characteristics

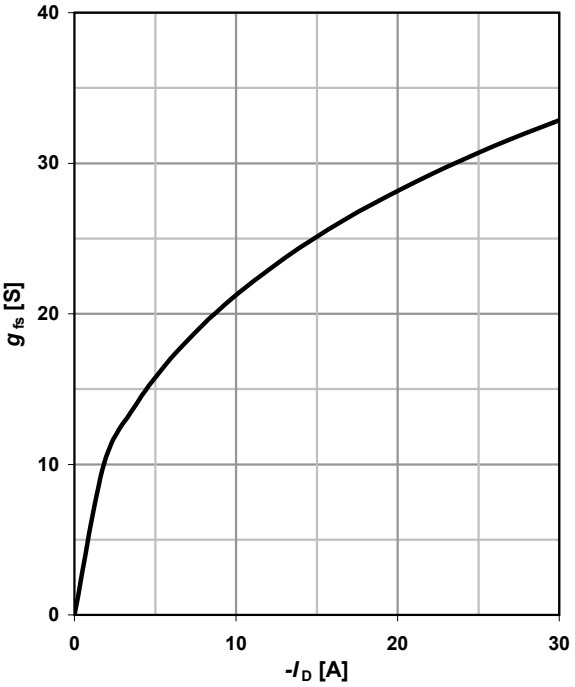
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



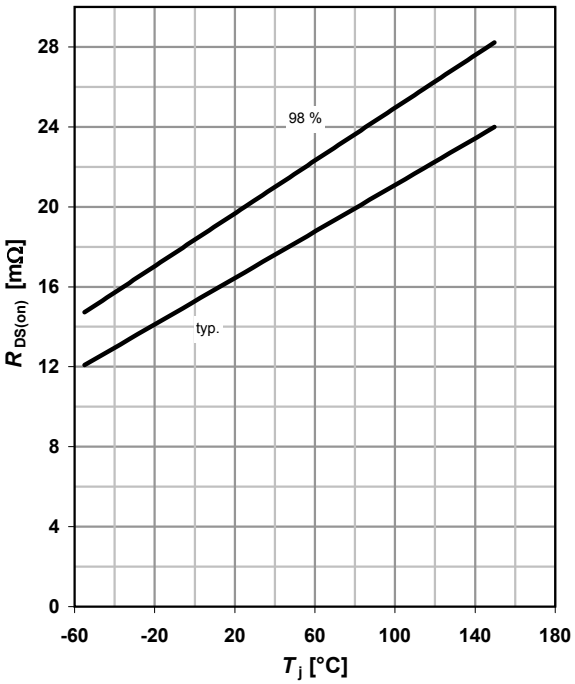
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



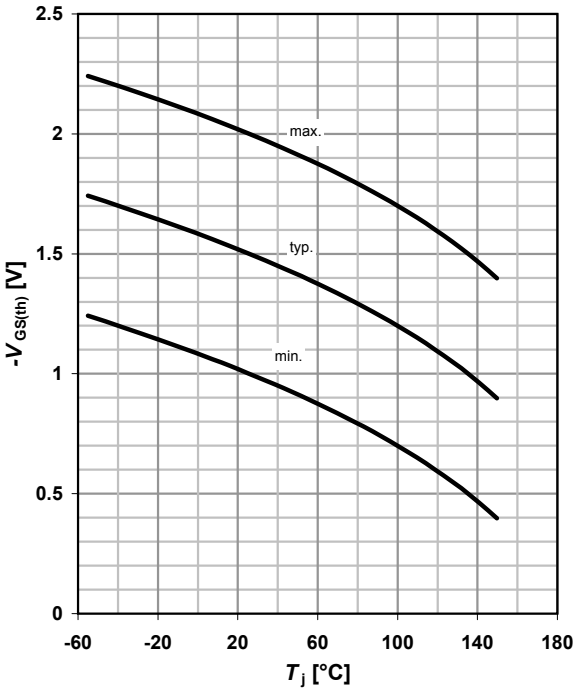
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=-9.1 A; V_{GS}=-10 V



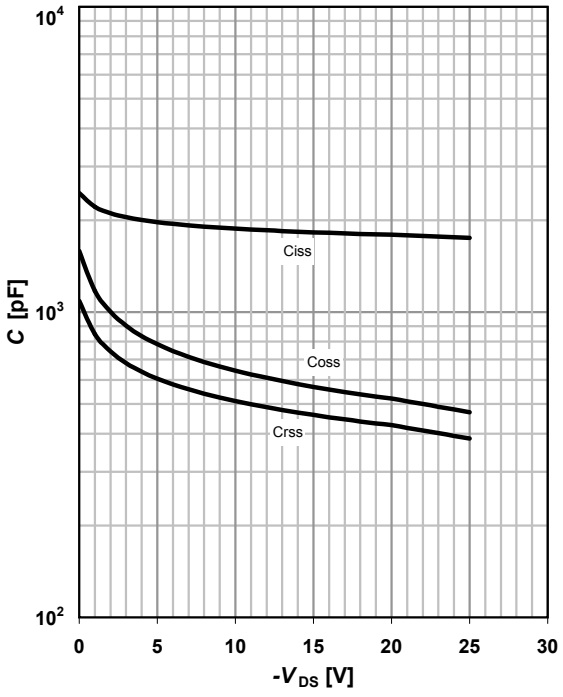
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=-100 µA



11 Typ. capacitances

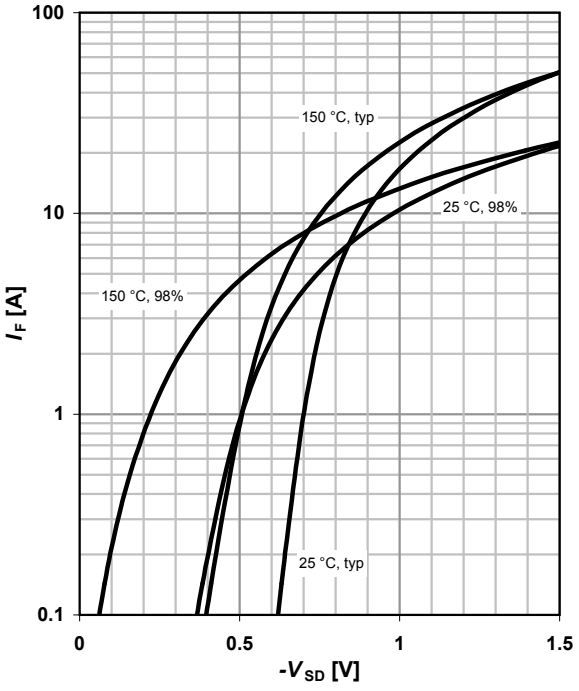
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

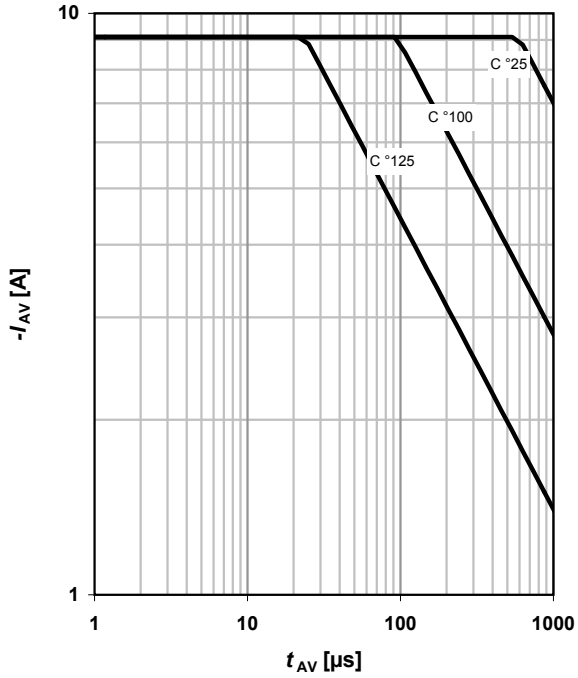
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

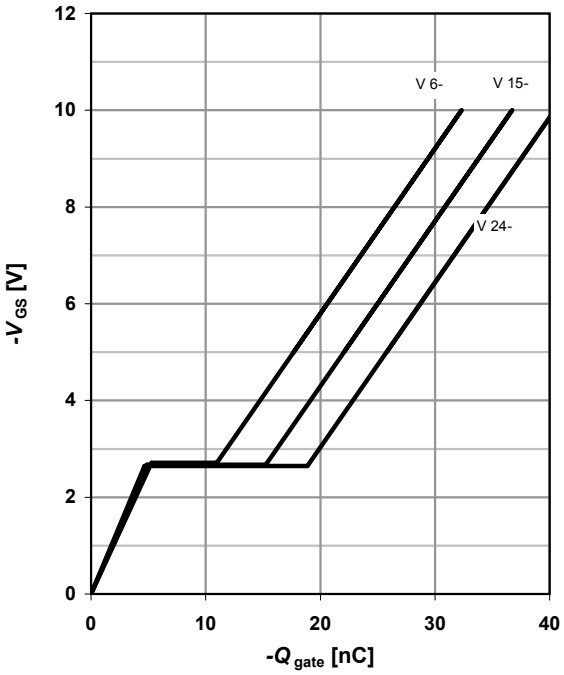
parameter: $T_{j(start)}$



14 Typ. gate charge

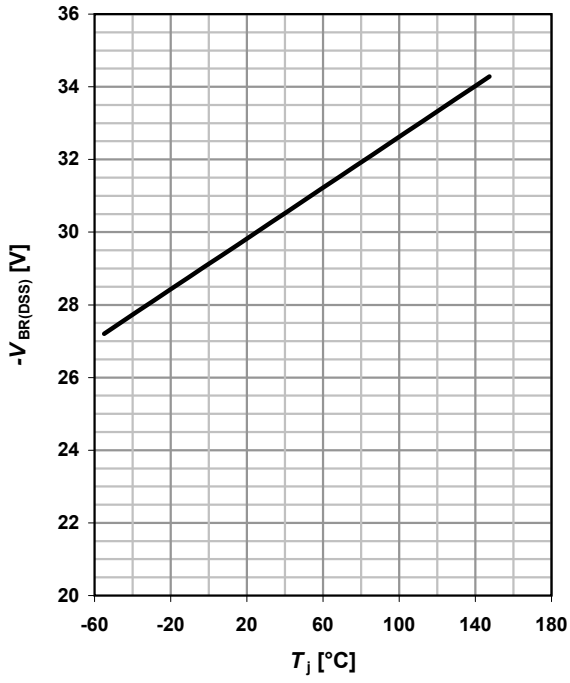
V_{GS}=f(Q_{gate}); I_D=-4.5 A pulsed

parameter: V_{DD}

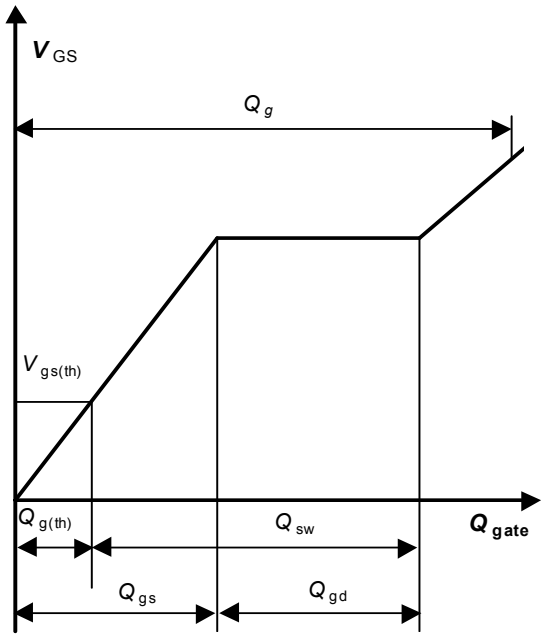


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=-250 µA

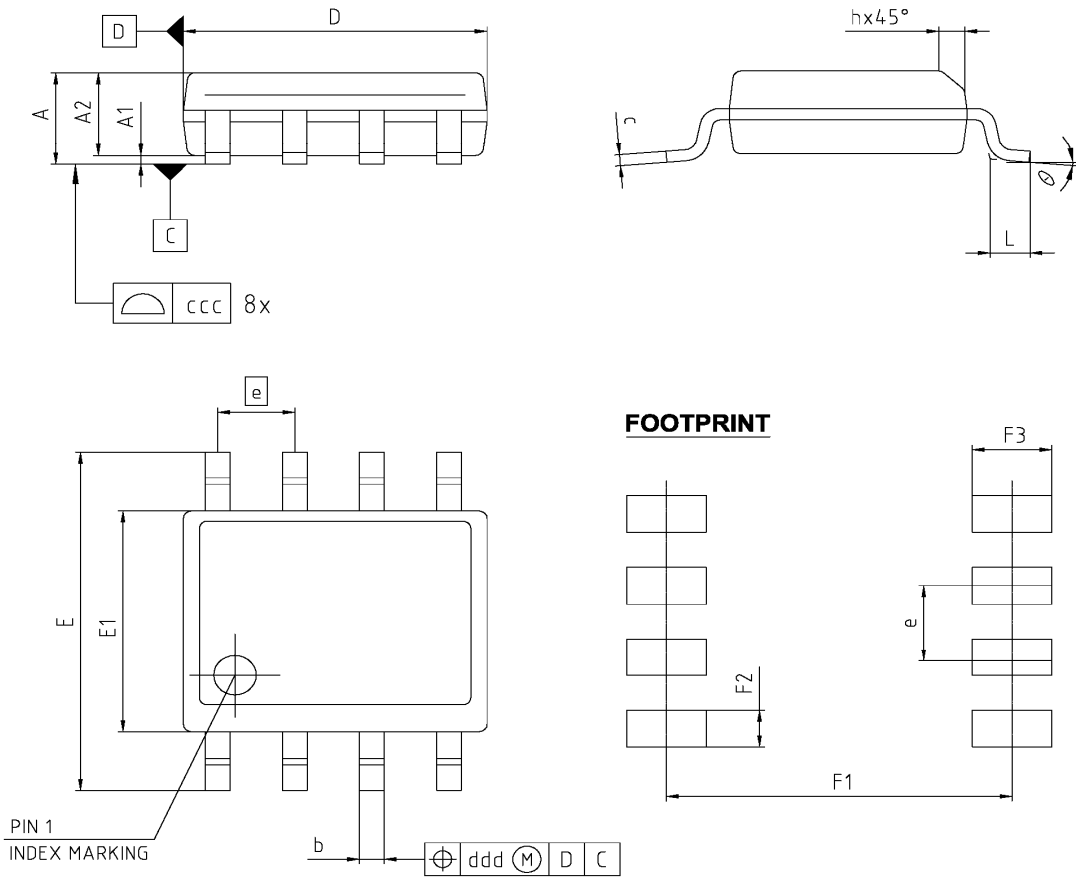


16 Gate charge waveforms



Package Outline

P-DSO-8: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.750	-	0.069
A1	0.100	-	0.004	-
A2	1.250	1.650	0.049	0.065
b	0.360	0.510	0.014	0.020
c	0.190	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270		0.050	
N	8		8	
L	0.390	0.890	0.015	0.035
h	0.250	0.410	0.010	0.016
θ	0°	8°	0°	8°
ccc	0.100		0.004	
ddd	0.200		0.008	
F1	5.590	5.790	0.220	0.228
F2	0.550	0.750	0.022	0.030
F3	1.210	1.410	0.048	0.056

REFERENCE	JEDEC / MS-012
SCALE	0, 1.0, 0, 1.0, 2mm
EUROPEAN PROJECTION	
ISSUE DATE	19-09-2005
FILE	DSO-8_1

Dimensions in mm

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