

N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD16325Q5](#)

FEATURES

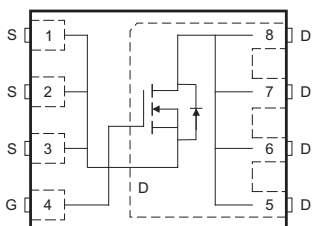
- Optimized for 5V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

APPLICATIONS

- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5V gate drive applications.

Top View


P0094-01

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25	V
Q_g	Gate Charge Total (4.5V)	18	nC
Q_{gd}	Gate Charge Gate to Drain	3.5	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	2.1 mΩ
		$V_{GS} = 4.5V$	1.7 mΩ
		$V_{GS} = 8V$	1.5 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

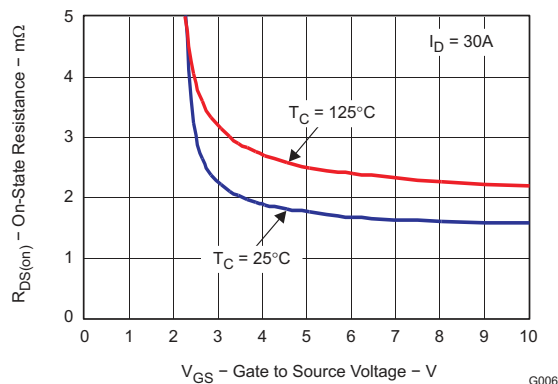
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16325Q5	SON 5-mm x 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

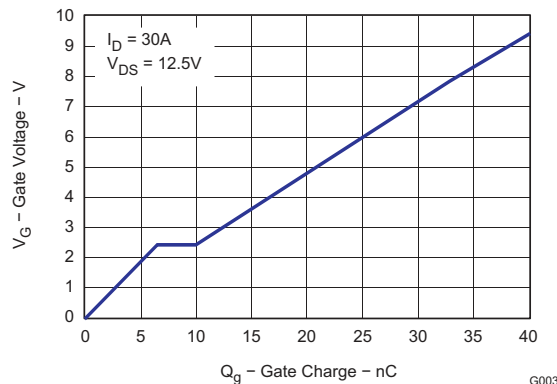
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current ⁽¹⁾	33	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	200	A
P_D	Power Dissipation ⁽¹⁾	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 100\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	500	mJ

- (1) Typical $R_{\theta JA} = 38^\circ\text{C/W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.
- (2) Pulse duration $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

 $R_{DS(on)}$ vs V_{GS}


G006

Gate Charge


G003



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NexFET is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

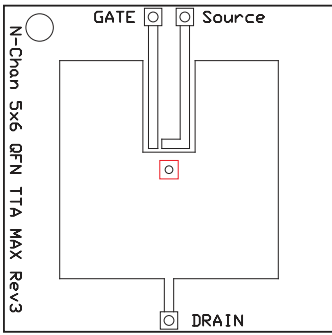
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
B _V DSS	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	25			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +10/-8V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	0.9	1.1	1.4	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 3V, I _D = 30A		2.1	2.9	mΩ
		V _{GS} = 4.5V, I _D = 30A		1.7	2.2	mΩ
		V _{GS} = 8V, I _D = 30A		1.5	2	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _D = 30A		159		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 12.5V, f = 1MHz		3070	4000	pF
C _{oss}	Output Capacitance			2190	2850	pF
C _{rss}	Reverse Transfer Capacitance			120	150	pF
R _G	Series Gate Resistance			1.6	3.2	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 12.5V, I _{DS} = 30A		18	25	nC
Q _{gd}	Gate Charge – Gate to Drain			3.5		nC
Q _{gs}	Gate Charge – Gate to Source			6.6		nC
Q _{g(th)}	Gate Charge at V _{th}			3.3		nC
Q _{oss}	Output Charge	V _{DS} = 13V, V _{GS} = 0V		43		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 12.5V, V _{GS} = 4.5V, I _{DS} = 30A, R _G = 2Ω		10.5		ns
t _r	Rise Time			16		ns
t _{d(off)}	Turn Off Delay Time			32		ns
t _f	Fall Time			12		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{DS} = 30A, V _{GS} = 0V		0.8	1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 10V, I _F = 30A, di/dt = 300A/μs		63		nC
t _{rr}	Reverse Recovery Time	V _{DD} = 10V, I _F = 30A, di/dt = 300A/μs		47		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

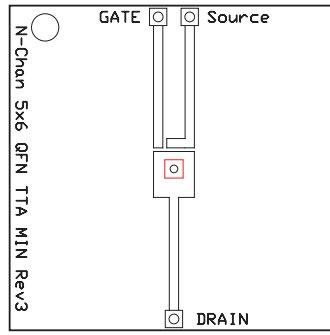
PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			1	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ^{(1) (2)}			50	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

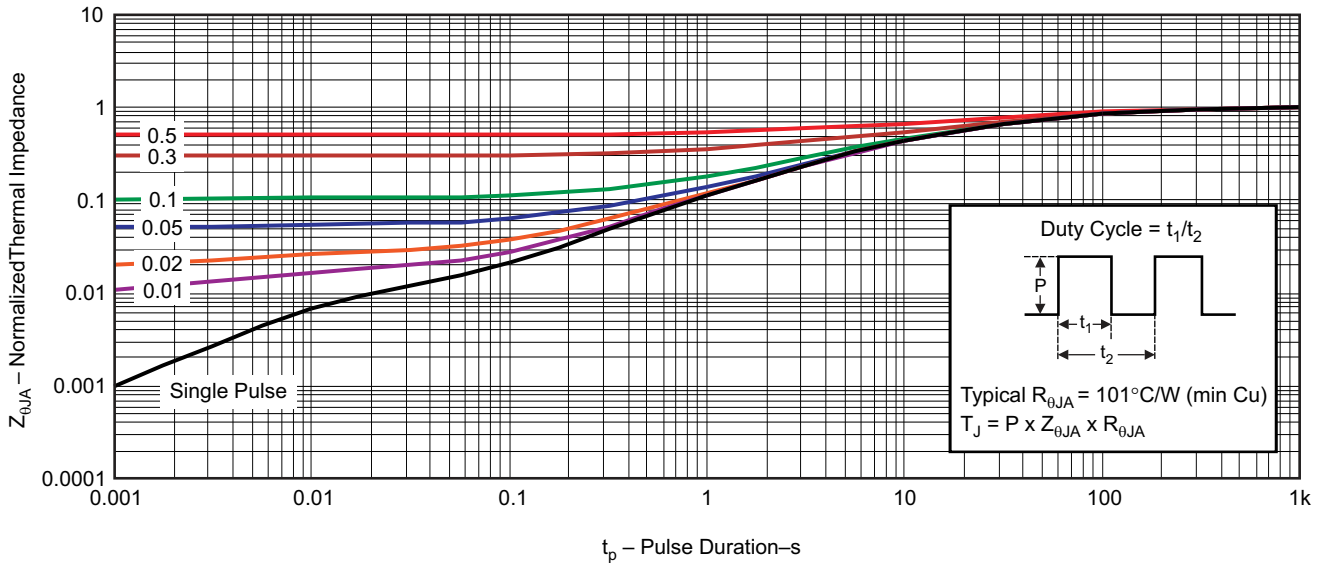


M0137-02

Max $R_{\theta JA} = 126^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

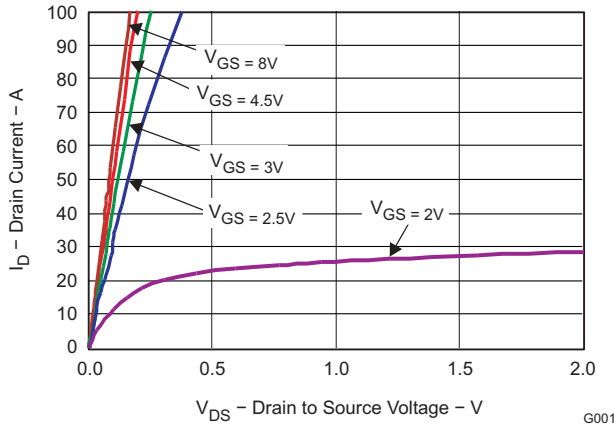


Figure 2. Saturation Characteristics

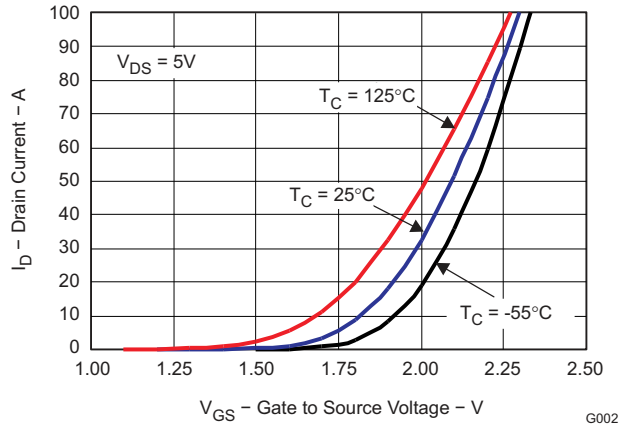


Figure 3. Transfer Characteristics

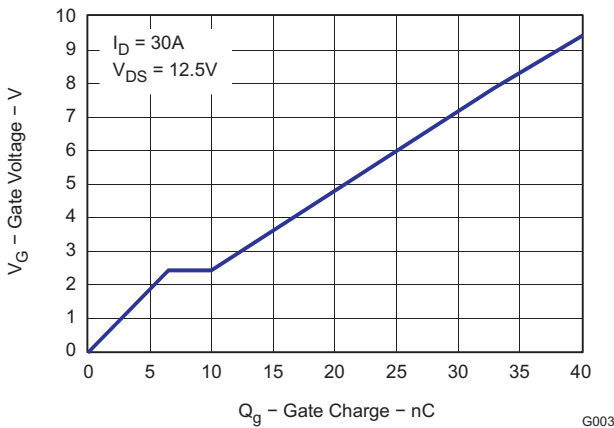


Figure 4. Gate Charge

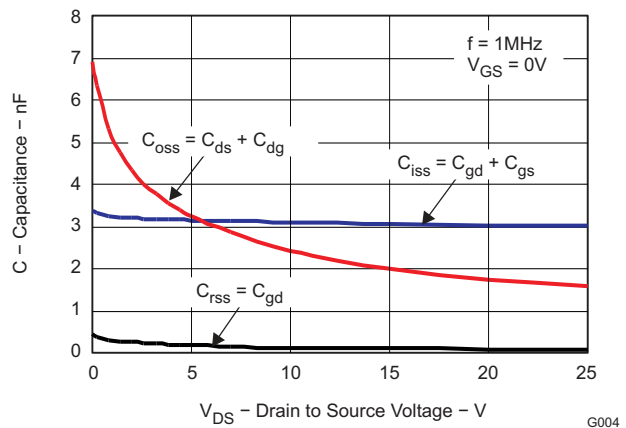


Figure 5. Capacitance

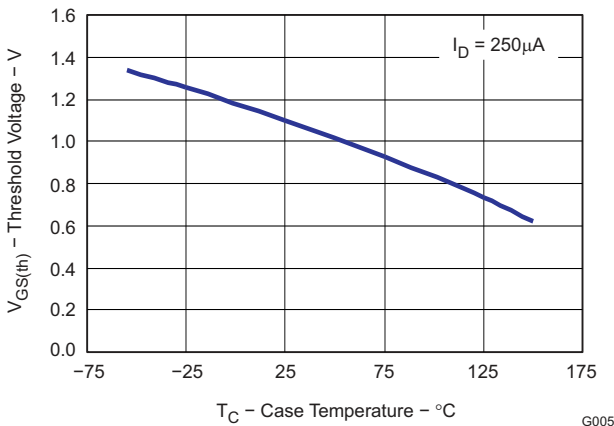


Figure 6. Threshold Voltage vs. Temperature

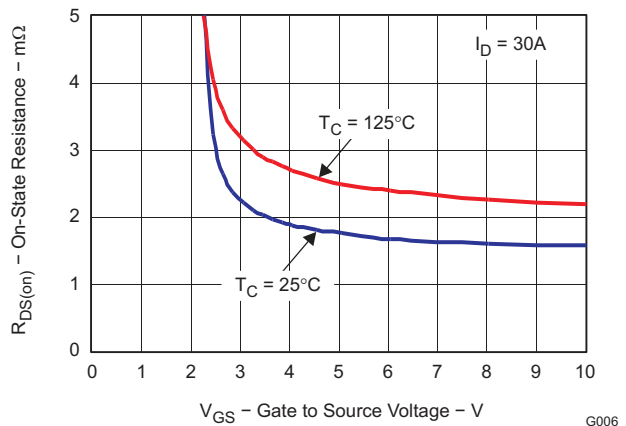


Figure 7. On-State Resistance vs. Gate to Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

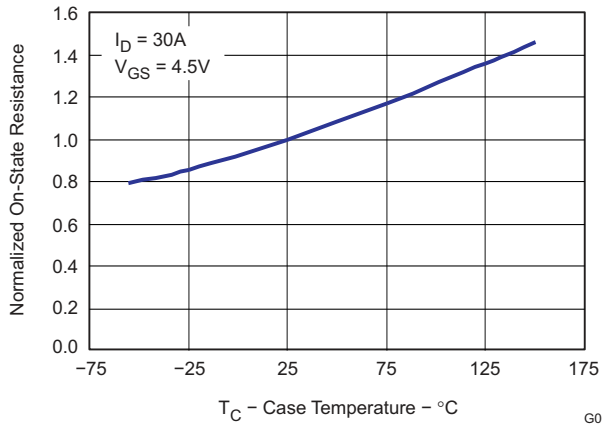


Figure 8. Normalized On-State Resistance vs. Temperature

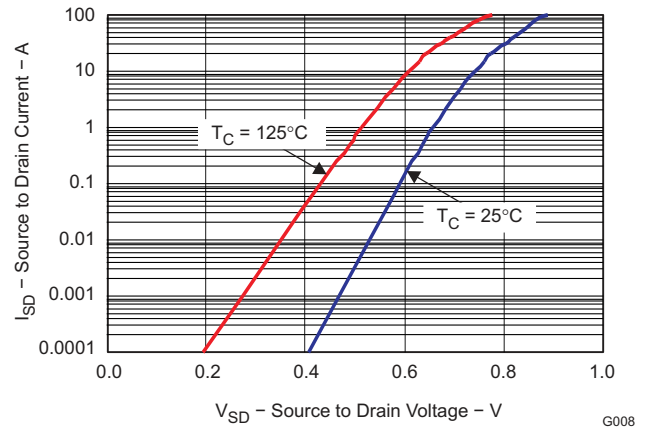


Figure 9. Typical Diode Forward Voltage

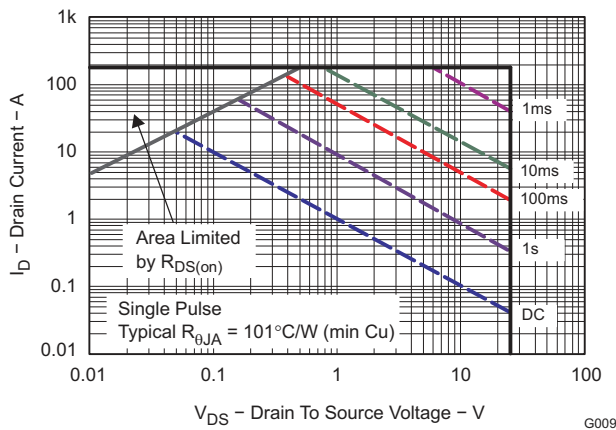


Figure 10. Maximum Safe Operating Area

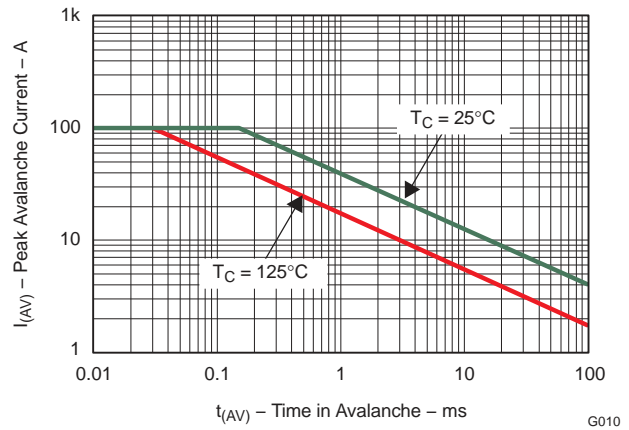


Figure 11. Single Pulse Unclamped Inductive Switching

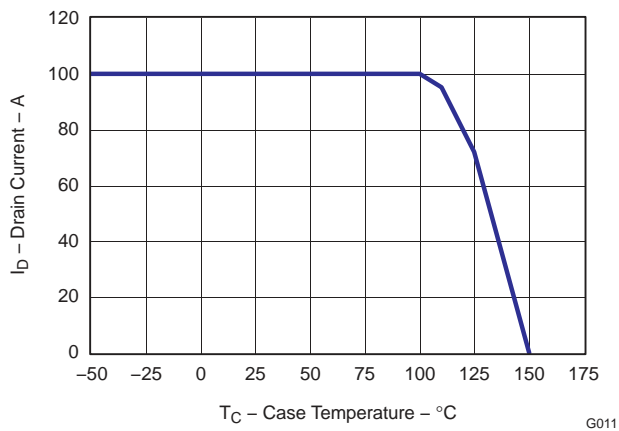
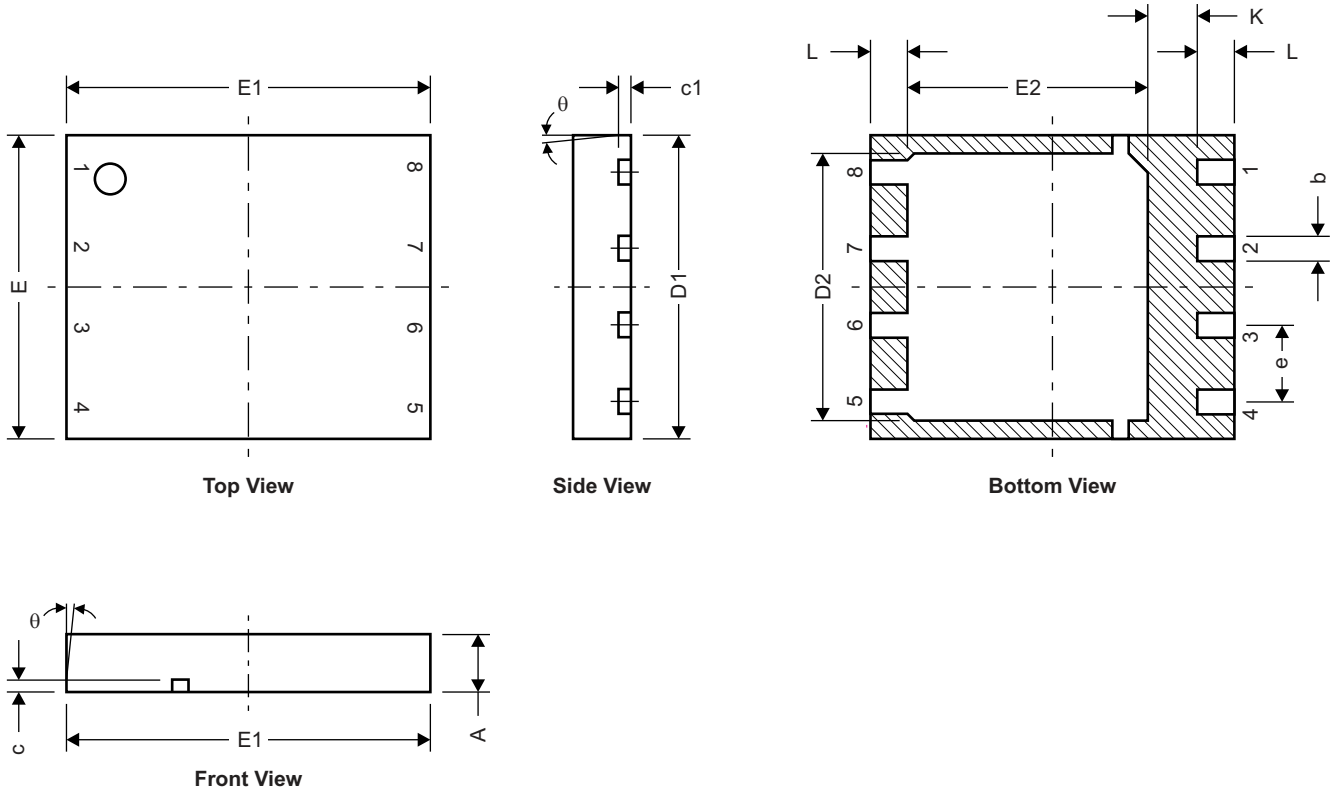


Figure 12. Maximum Drain Current vs. Temperature

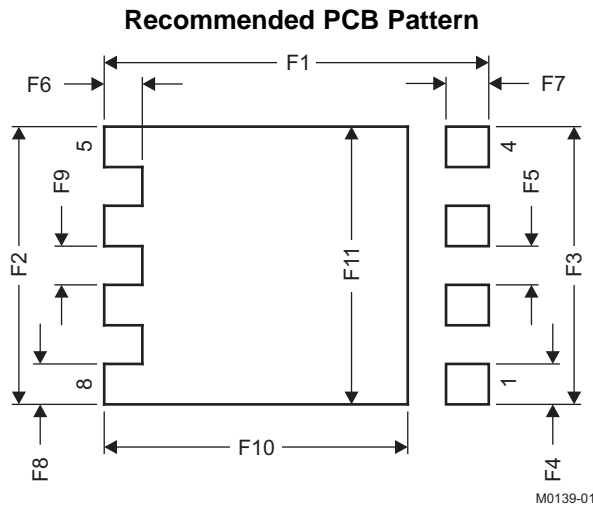
MECHANICAL DATA

Q5 Package Dimensions



M0140-01

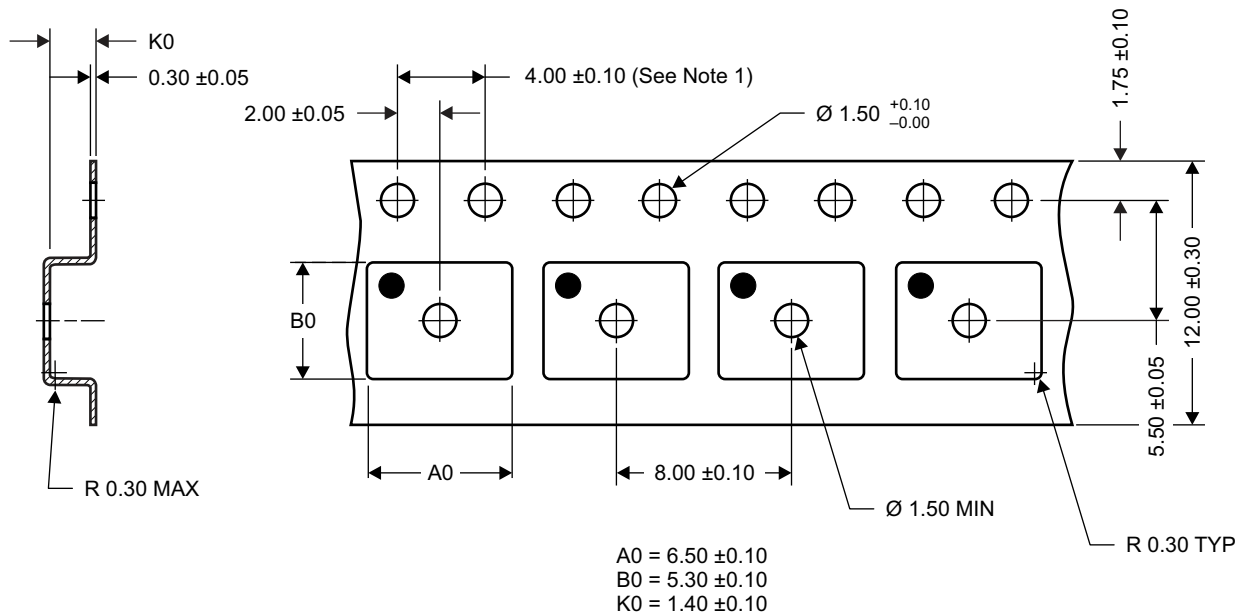
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
L	0.510	0.710	0.020	0.028
θ	0.00			



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5 Tape and Reel Information



Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm, unless otherwise specified.
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- MSL1 260°C (IR and convection) PbF reflow compatible

REVISION HISTORY

Changes from Original (August 2009) to Revision A Page

- Changed Q_{rr} Reverse Recovery Charge typical value From: 102nC To: 63nC **2**
-

Changes from Revision A (September 2009) to Revision B Page

- Changed Note 1 of the ABSOLUTE MAXIMUM RATINGS From: $R_{\theta JA} = 38^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 38^{\circ}\text{C/W}$ **1**
 - Changed I_{DM} Pulsed Drain Current in the ABSOLUTE MAXIMUM RATINGS From: 210A To: 200A **1**
 - Changed From: Max $R_{\theta JA} = 48^{\circ}\text{C/W}$ To: Max $R_{\theta JA} = 50^{\circ}\text{C/W}$ **3**
 - Changed From: Max $R_{\theta JA} = 113^{\circ}\text{C/W}$ To: Max $R_{\theta JA} = 126^{\circ}\text{C/W}$ **3**
 - Changed [Figure 1](#) text - From: $R_{\theta JA} = 101^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 101^{\circ}\text{C/W}$ **3**
 - Changed [Figure 10](#) text - From: $R_{\theta JA} = 101^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 101^{\circ}\text{C/W}$ **5**
-

Changes from Revision B (April 2010) to Revision C Page

- Changed $R_{DS(on)}$ - $V_{GS} = 3\text{V}$ in the Electrical Characteristics table From: 2.7 to 2.9 in the max column **2**
 - Deleted the Package Marking Information section **7**
-

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16325Q5	ACTIVE	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16325	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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