Dual Low Voltage Hot Swap Controller

This IC targets dual voltage hot swap applications across the +2.5V to +3.3V bias supply voltage range with a second lower voltage rail down to less than 1V. It features a charge pump for driving external N-Channel MOSFETs, regulated current protection and duration, output undervoltage monitoring and reporting, optional latch-off or retry response, and adjustable soft-start.

The current regulation level (CR) for each rail is set by two external resistors and each CR duration is set by an external capacitor on the TIM pin. After the CR duration has expired the IC then quickly pulls down the associated GATE(s) output turning off its external FET(s). The ISL6172 offers a latched output or indefinite auto retry mode of operation.

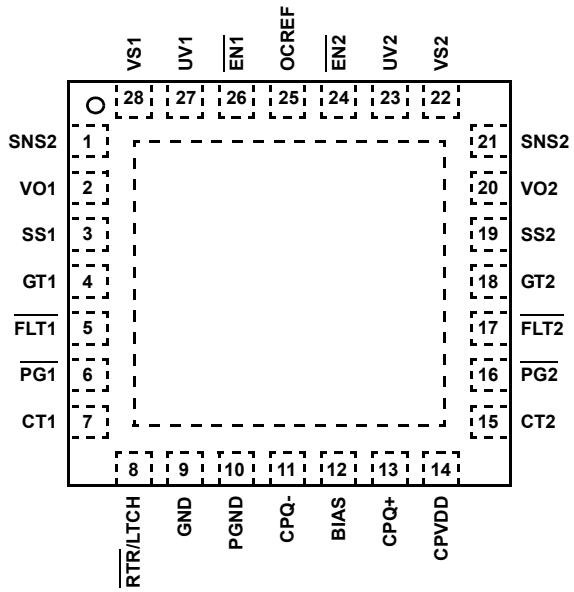
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6172DRZA*	0 to +85	28 Ld 5x5 QFN (Pb-free)	L28.5x5
ISL6172DRZA-T*	0 to +85	28 Ld 5x5 QFN (Pb-free)	L28.5x5
ISL6172EVAL3	Evaluation Platform		

* Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Pinout

28 LEAD QFN
TOP VIEW



Features

- Dual Supply Hot Swap Power Distribution Control to <1V
- Less than 1µs Response Time to Dead Short
- Overcurrent Circuit Breaker Fault Isolation and Programmable Current Regulation Level Protection Functions
- Programmable Current Regulation Duration
- Charge Pump Allows the use of N-Channel MOSFETs
- Rail Independent Control, Monitoring and Reporting I/O
- Adjustable Ramp up for Inrush Protection During Turn On
- Two Levels of Overcurrent Detection Provide Fast Response to Varying Fault Conditions
- Latch-off or Auto Reset Response to Fault Functions
- Adjustable Current Regulation Threshold as low as 20mV
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-free

Applications

- Power Supply Sequencing, Distribution and Control
- Hot Swap/Electronic Breaker Circuits
- Network Hubs, Routers, Switches
- Hot Swap Bays, Cards and Modules

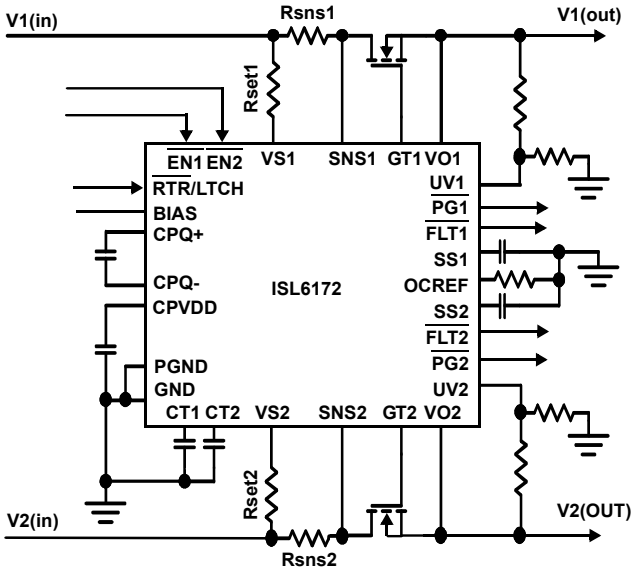


FIGURE 1. TYPICAL APPLICATION

Block Diagram

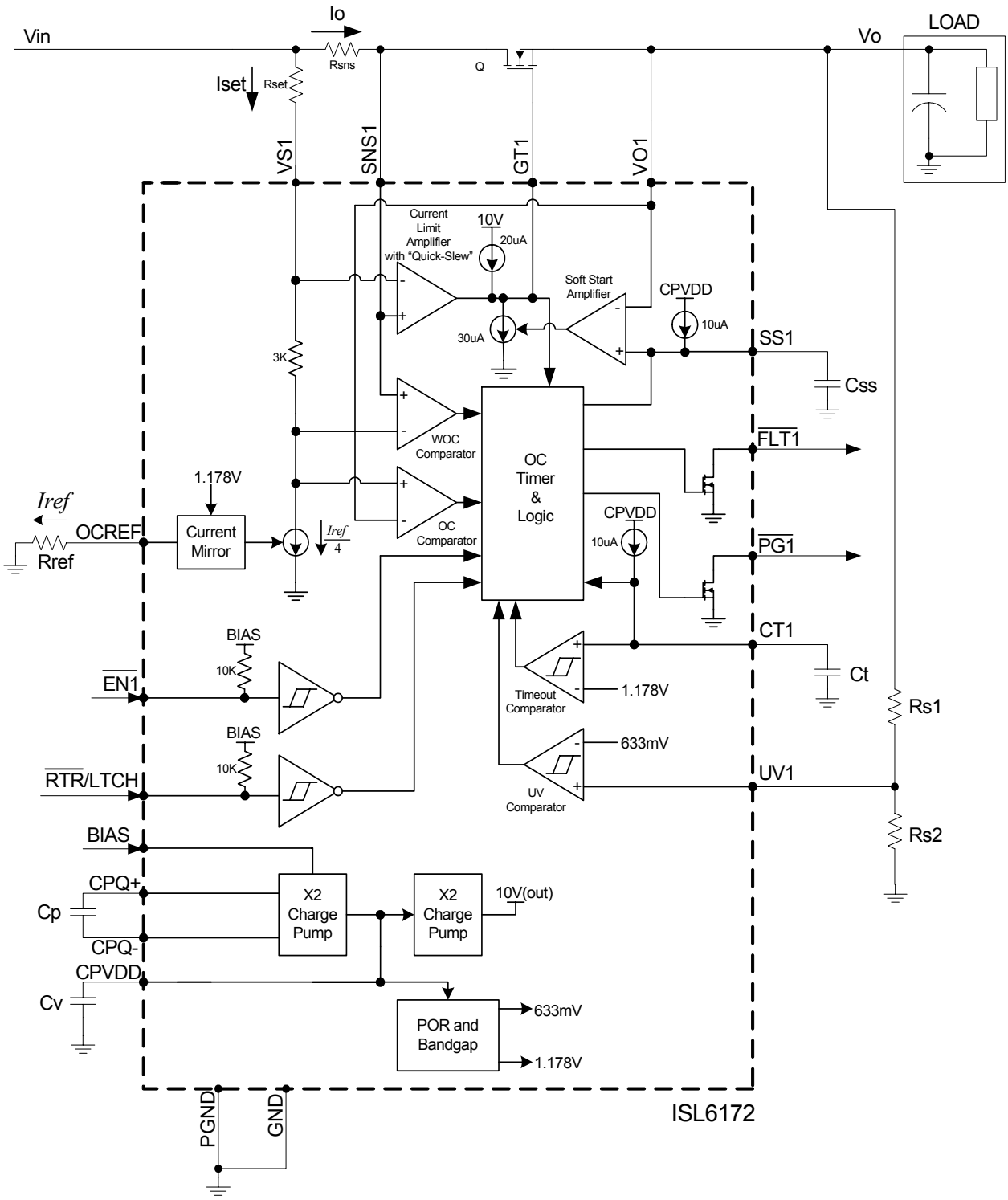
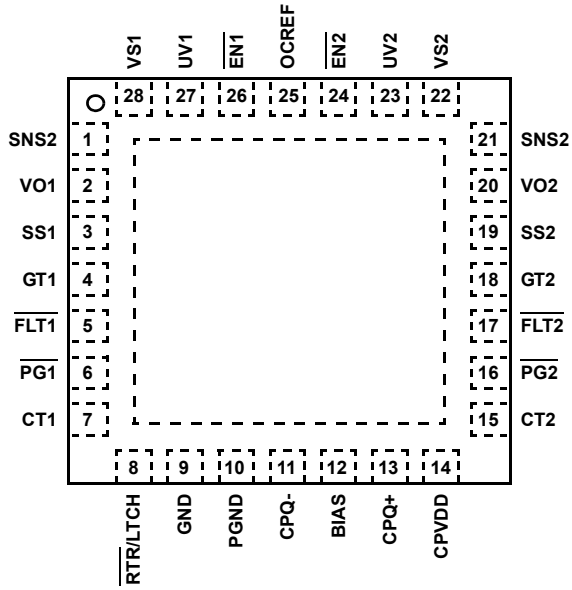


FIGURE 2. ISL6172 - INTERNAL BLOCK-DIAGRAM OF ONE CHANNEL

Pinout

28 LEAD QFN
TOP VIEW



Pin Descriptions

PIN	NAME	FUNCTION	DESCRIPTION
1	SNS1	Current Sense Input	This pin is connected to the current sense resistor and control MOSFET Drain node. It provides current sense signal to the internal comparator and amplifier in conjunction with VS1 pin.
2	VO1	Output Voltage 1	This pin is connected to the control MOSFET switch source, which connects to a load. Internally, this voltage is used for OC comparator input and for SS control.
3	SS1	Soft-Start Duration Set Input	A capacitor from this pin to ground sets the output soft-start ramp slope. This capacitor is charged by the internal 10µA current source setting the soft-start ramp. The output voltage ramp tracks the SS ramp by controlled enhancement of FET gate. Once ramp-up is completed, the capacitor is discharged. If common capacitor is used (by tying SS1, SS2 together and the capacitor to GND from the connection) then both the outputs track each other as they ramp up.
4	GT1	Gate Drive Output	Direct connection to the gate of the external N-Channel MOSFET. At turn-on the Gate will charge to VIN1+5.3V with a 20µA source.
5	$\overline{\text{FLT1}}$	Fault Output	This is an open drain output. It asserts (pulls low) once the current regulation duration (determined by the CTx timeout cap) has expired.
6	$\overline{\text{PG1}}$	Power Good Output	This is an active low, open drain output. When asserted (logic zero), it indicates that the voltage on UV1 pin is more than 643mV (633mV + 10mV hysteresis). This output is valid at VBIAS >1V.
7	CT1	Timer Capacitor	A capacitor from this pin to ground controls the current regulation duration from the onset of current regulation to channel shutdown (current limit time-out). Once the voltage on CTx cap reaches V_{CT_Vth} the GATE outputs are pulled down and the FLT(s) is asserted. The duration of current limit time-out = (C_{TIM}*1.178)/10µA When the OC comparator trips AND the $\overline{\text{RTR}}$/LTCH pin is left floating (or pulled high), the IC's faulty channel remains shut down for 64 cycles (each cycle length is equal to the current limit time-out duration).
8	$\overline{\text{RTR}}$/ LTCH	Retry Or Latch Input	This input dictates the IC behavior (for either channel) under OC condition. If it is pulled high (or left floating), the IC will shut down upon OC detection. If it is pulled low, the IC will go into retry mode after an interval determined by the capacitor on CTx pin. The faulting channel will remain shut down for 64 cycles and will try to come out of it on 65th cycle. Each cycle length is determined by the formula shown in CT pin description.
9	GND	Chip Gnd	This pin is also internally shorted to the metal tab at the bottom of the IC.

Pin Descriptions (Continued)

PIN	NAME	FUNCTION	DESCRIPTION
10	PGND		Charge pump ground. Both GND and PGND must be tied together.
11	CPQ-	Charge Pump Capacitor Low Side	Flying cap lowside
12	BIAS	Chip Bias Voltage	Provides IC Bias. Should be 2V to 4V for IC to function normally. This pin can be powered from a supply voltage that is not being controlled. It is preferable to use 3.3V even if the channels being controlled are 2.5V or lower because more gate drive voltage will be available to the MOSFETs.
13	CPQ+	Charge Pump Capacitor High Side	Flying cap highside. Use of 0.1µF for 2.5V bias and 0.022µF for 3.3V bias is recommended.
14	CPVDD	Charge Pump Output	This is the voltage used for some internal pullups and bias. Use of 0.47µF (minimum) is recommended.
15	CT2	Timer Capacitor	Same function as pin 7
16	$\overline{PG2}$	Power Good Output	Same function as pin 6
17	$\overline{FLT2}$	Fault Output	Same as pin 5
18	GT2	Gate Drive Output	Same as pin 4
19	SS2	Soft-Start Duration Set Input	Same as pin 3
20	VO2	Output Voltage 2	Same as pin 2
21	SNS2	Current Sense Input	Same as pin 1
22	VS2	Current Sense Reference	Voltage input for one of the two voltages. Provides a 20µA current source for the ISET series resistor which sets the voltage to which the sense resistor IR drop is compared.
23	UV2	Undervoltage Monitor Input	This pin is one of the two inputs to the undervoltage comparator. The other input is the 633mV reference. It is meant to sense the output voltage through a resistor divider. If the output voltage drops so that the voltage on the UV pin goes below 633mV, PG2 is deasserted.
24	$\overline{EN2}$	Enable	This is an active low input. When asserted (pulled low), the SS and gate drive are released and the output voltage gets enabled. When deasserted (pulled high or left floating), the reverse happens.
25	OCREF	Ref. Current Adj.	Allows adjustment of the reference current through R_{SET} and the internal current regulation set resistor, thus setting the thresholds for CR, OC and WOC.
26	$\overline{EN1}$	Enable Input	Same as pin 24
27	UV1	Undervoltage Monitor Input	Same as pin 23
28	VS1	Current Sense Reference	Same as pin 22

Absolute Maximum Ratings

VBIAS/VIN1 . . . . . +5.5V
GTx, CPQ+ . . . . . -0.3V to +12V
ENx, RTR/LTCH, SNSx, PGx, FLTx, VSx, CTx, UVx,
SSx, CPQ-, CPVDD. . . . . -0.3V to 5.5VDC
Output Current . . . . . Short Circuit Protected
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 1kV
Machine Model (Per EIAJ ED-4701 Method C-111). 75V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) . . . 1.5kV

Operating Conditions

VBIAS/VIN1 Supply Voltage Range. . . . . +2.25V to +3.63V
Temperature Range (T_A) . . . . . 0°C to 85°C

Thermal Information

Thermal Resistance (Typical, Notes 1, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5x5 QFN Package	42	12.5

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
For recommended soldering conditions, see Tech Brief TB389.
(QFN - Leads Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. All voltages are relative to GND, unless otherwise specified.
3. 1V (min) on the BIAS pin required for $\overline{FLT}$ to be valid.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{DD} = 2.5V to +3.3V, $T_A = T_J$ = 0°C - 85°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT REGULATION CONTROL						
Current Regulation Threshold Voltage	V_{CRVTH_1}	RISET = 1.25K 1%, I_{SET} = 20µA	20	25	30	mV
Current Regulation Accuracy	$V_{CRVTH\_1}R$	RISET = 1.25K 1%, I_{SET} = 20µA	-20		+20	%
Current Regulation Threshold Voltage	V_{CRVTH_2}	RISET = 2.50K 1%, I_{SET} = 20µA	45	50	55	mV
Current Regulation Accuracy	$V_{CRVTH\_2}R$	RISET = 2.50K 1%, I_{SET} = 20µA	-10		+10	%
CT Threshold Voltage	V_{CT_Vth}		1.156	1.178	1.200	V
CT Charging Current	I_{CT}			10		µA
GATE DRIVE						
GATE Response Time from WOC (Open)	pd_woc_open	GATE open 100mV of overdrive on the WOC comparator		3		ns
GATE Response Time from WOC (Loaded)	pd_woc_load	GATE = 1nF		80		ns
GATE Response Time in Current Regulation mode (Loaded)	pd_cr_load	GATE = 1nF 120% Load Current		4		ms
GATE Response Time in "Quick-Slew" pull-down Mode (Loaded)	pd_oc_load	GATE = 1nF 22mV of overdrive on Amplifier Input		50		µs
GATE Turn-On Current	IGATE	GATE = 2V VV_S = 2V V_{SNS} = 2.1V	14	18.5	22	µA
Current Limit Amplifier Transconductance	Gm	$VV_S - V_{SNS}1$ = -25mV		0.35		ms
GATE Pull Down Resistor (WOC, fault or off conditions)	Ig_woc	T_J = 25°C Gate = 2V	18	25	42	Ω
GATE Pull Down Resistor ("Quick-Slew" mode)	Ig_qs	T_J = 25°C Gate = 2V	9	11	13	kΩ

Electrical Specifications V_{DD} = 2.5V to +3.3V, $T_A = T_J$ = 0°C - 85°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE Voltage	V_{GATE}	Bias = 2.5V (see graph on page 7)	8.8	9.3	9.7	V
		2.1 < Bias < 2.5 (see graph on page 7)		8		V
BIAS						
Supply Current	I_{BIAS}	V_{BIAS} = 3.3V		5	10	mA
POR Rising Threshold	VIN_POR_L2H				2.1	V
POR Falling Threshold	VIN_POR_H2L				2.0	V
POR Threshold Hysteresis	VIN_POR_HYS		10			mV
I/O						
Undervoltage Comparator Falling Threshold	V_{UV_VTHF}		620	635	650	mV
Undervoltage Comparator Hysteresis	V_{UV_HYST}		11	16	21	mV
$\overline{EN}$ Rising Threshold	PWR_Vth_R	V_{BIAS} = 2.5V	1.60	1.95	2.25	V
$\overline{EN}$ Falling Threshold	PWR_Vth_F	V_{BIAS} = 2.5V	0.97	1.10	1.30	V
$\overline{EN}$ Hysteresis	PWR_HYST	V_{BIAS} = 2.5V	600	850	1100	mV
$\overline{PG}$ Pull-Down Voltage	VOL_PG	I_{PG} = 8mA	0.047		0.4	V
$\overline{FLT}$ Pull-Down Voltage (Note 3)	VOL_FLT	I_{FLT} = 8mA	0.047		0.4	V
Soft-Start Charging Current	IQ_SS	VSS = 1V		10		µA
CHARGE PUMP						
CPVDD	V_CPVDD	V_{BIAS} = 2.0V	3.6	3.8	4.0	V
CPVDD	V_CPVDD	V_{BIAS} = 3.3V	4.9	5.2	5.5	V
CPVDD	V_CPVDD	V_{BIAS} = 3.3V T = 25°C External User Load = 6mA		5.0		V

Typical Performance Curves (at 25°C unless otherwise specified)

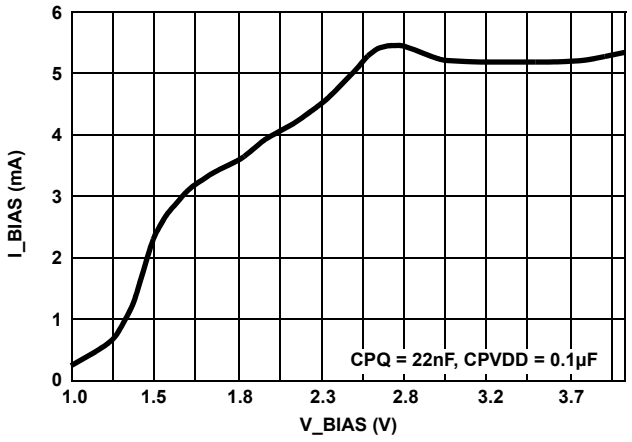


FIGURE 3. I_BIAS vs V_BIAS

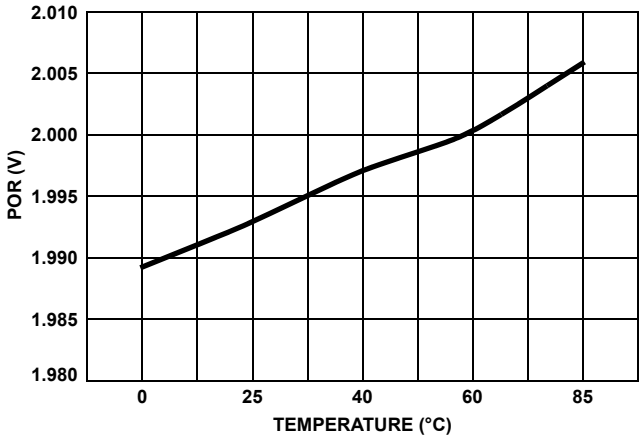


FIGURE 4. POR RISING THRESHOLD vs TEMPERATURE

Typical Performance Curves (at 25°C unless otherwise specified) (Continued)

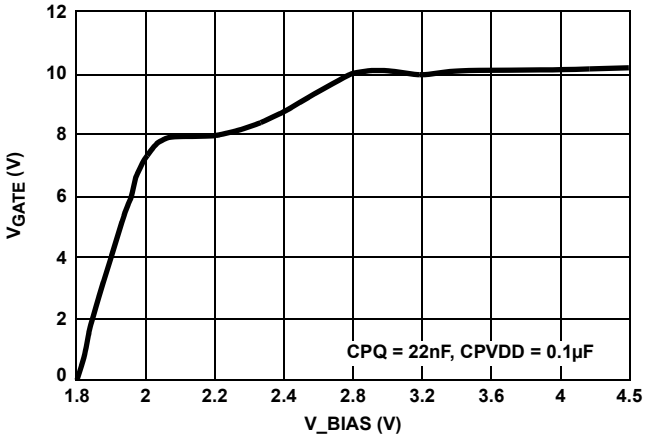


FIGURE 5. V_{GATE} vs V_BIAS

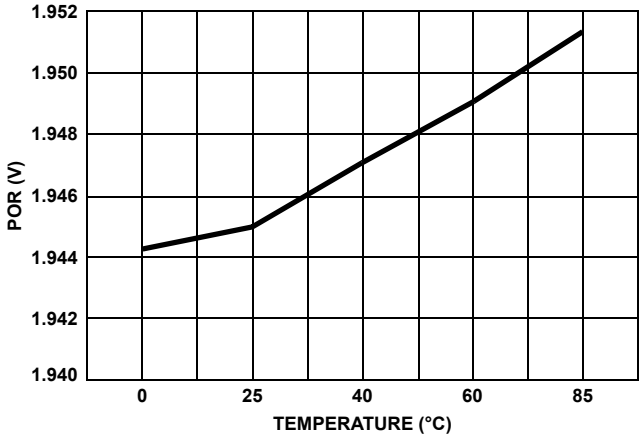


FIGURE 6. POR FALLING THRESHOLD vs TEMPERATURE

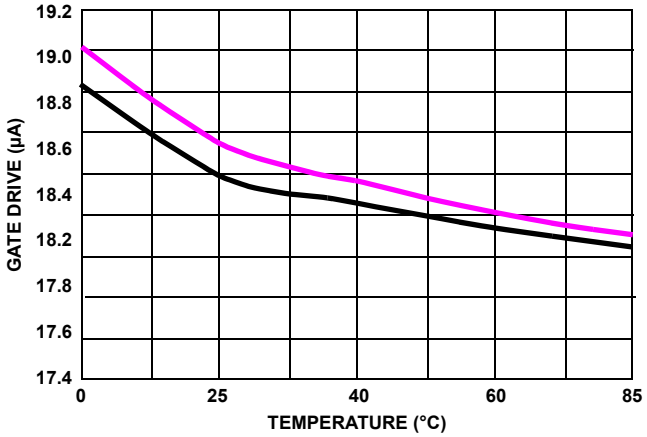


FIGURE 7. GATE DRIVE vs TEMPERATURE

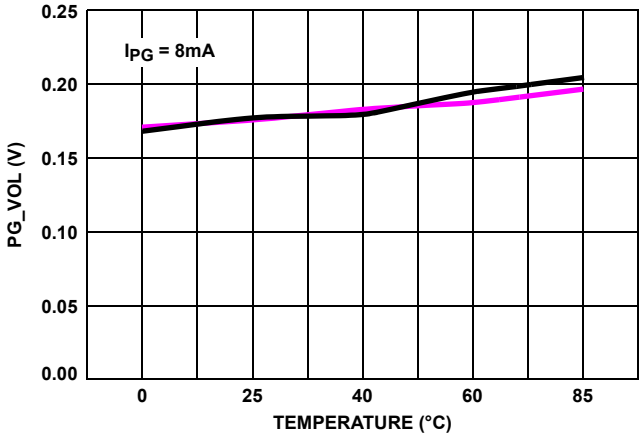


FIGURE 8. PG_VOL vs TEMPERATURE

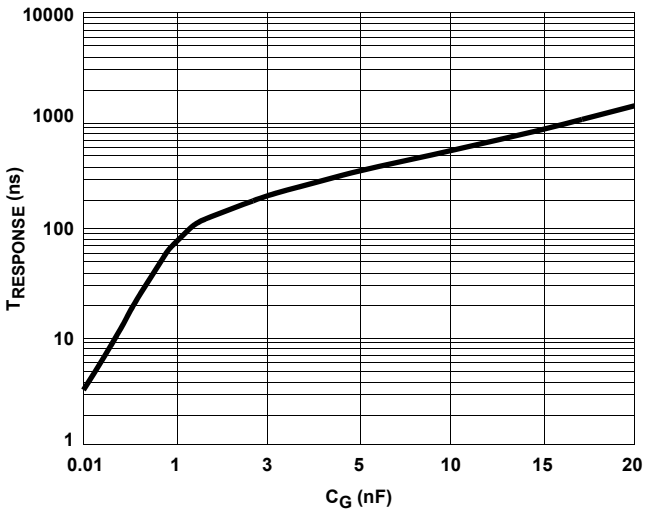


FIGURE 9. WOC RESPONSE vs LOAD CAPACITANCE

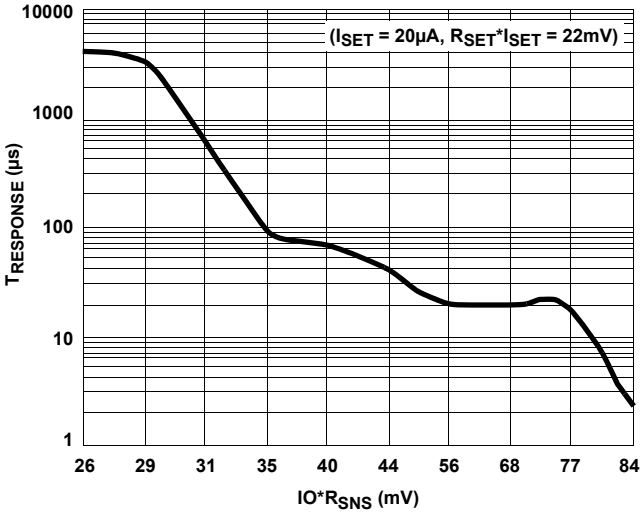


FIGURE 10. RESPONSE TIME vs I_O*R_{SNS}

Typical Performance Curves (at 25°C unless otherwise specified) (Continued)

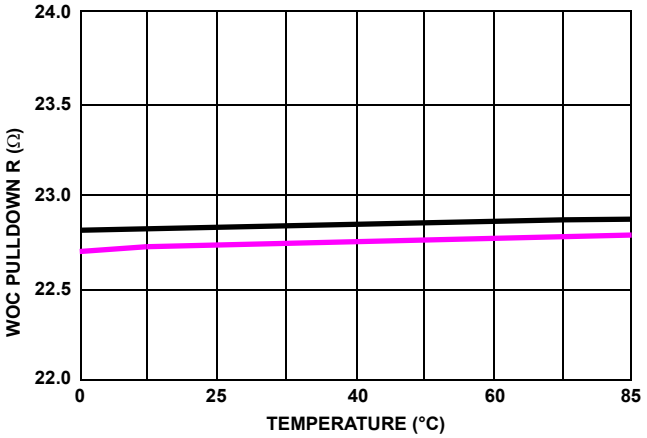


FIGURE 11. WOC PULLDOWN vs TEMPERATURE

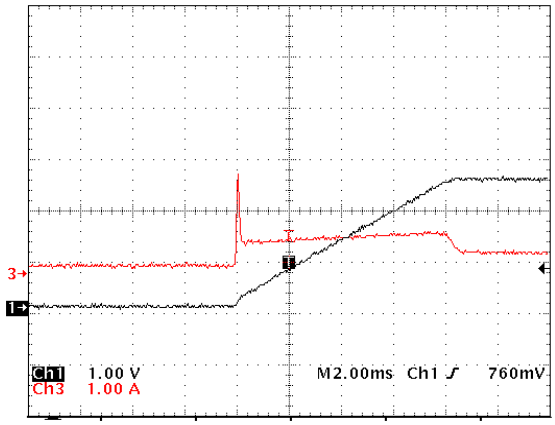
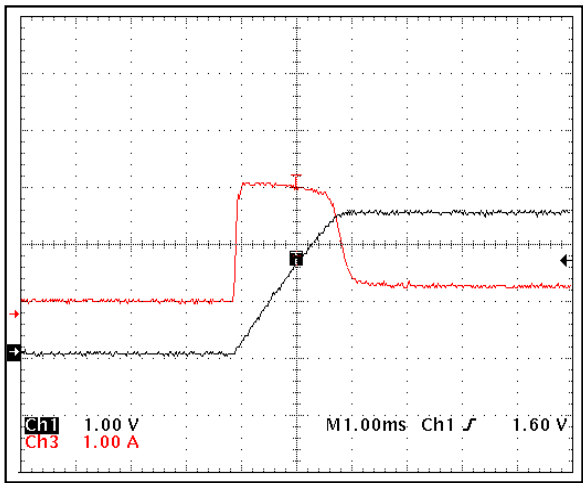


FIGURE 12. SS LIMITED START-UP - SS CAP 0.033µF IN PLACE



CH1: V_O2, CH3: I_{IN}

FIGURE 13. CURRENT LIMITED START-UP: SS CAP REMOVED, I_{CR} SET TO 2.2A. NOTE MAX INRUSH CURRENT REMAINS AT I_{CR} SET LEVEL (2.2A).

Figures 12 and 13 are actual scope shots under different circuit configurations that are possible with this IC. Figure 13 shows that the part is capable of limiting the inrush current to the value set by the current regulation amplifier in absence of or very small sized SS caps. Figure 13 is for the normal circuit shown on the front page.

Detailed Description of Operation

ISL6172 targets dual voltage hot-swap applications with a bias of 2.1V to 3.6VDC and the voltages being controlled down to 0.7VDC. The IC's main function is to limit and regulate the inrush current into the loads. This is achieved by enhancing an external MOSFET in a controlled manner. In order to fully enhance the MOSFET, the IC must provide adequate gate to source voltage, which is typically 5V or greater. Hence, the final steady-state voltage on Gate (GT) pin must be 5V above the load voltage. Two internal charge-pumps allow this to happen.

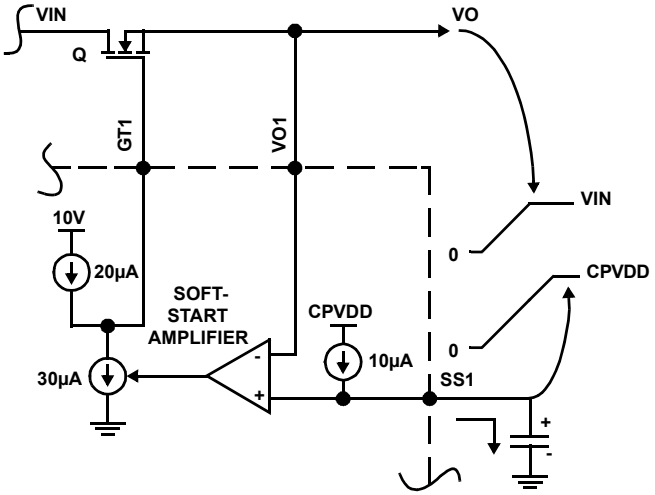


FIGURE 14. SOFT-START OPERATION

Controlled Soft-Start

The output voltages are monitored through the Vo pins and slew up at a rate determined by the capacitors on the Soft-start (SS) pin, as illustrated in Figure 14. 20µA of gate charge current is available. The soft-start amplifier controls the output voltage by robbing some of the gate charge current thus slowing down the MOSFET enhancement. When the load voltage reaches its set level, as sensed by its respective UV pin through an external resistor divider, the Power Good ($\overline{PG}$) output goes active, signaling that the output voltage has reached its set limit.

Current Monitoring and Protection

The IC monitors the load current (Io) by sensing the voltage-drop across the low value current sense resistor (R_{SNS}), which is connected in series with the MOSFET mentioned earlier and shown in the diagram on page 2, through Sense (SNS) and voltage set (VS) pins. The latter is through a resistor, R_{SET}, as shown. Three levels of overcurrent detection are available to protect against all possible fault scenarios. These levels are:

1. Current Limit or Current Regulation (CR)
2. "Quick Slew" Mode
3. Way Overcurrent (WOC)

Each of these modes is described in detail as follows:

1. Current Limit or Current Regulation (CR) Mode: When the load current reaches the current regulation threshold, the current amplifier loop closes and the circuit behaves like a current source. The current regulation threshold is set by setting a reference current, I_{SET}, through R_{SET} by selecting an appropriate resistor between OCREF and GND, which sets I_{REF}. The relationship between I_{REF} and I_{SET} is I_{REF} = 4*I_{SET}, where I_{REF} = Vocref/Rocref = 1.178/Rocref. I_{REF} would typically be set at 80µA.

Selecting appropriate values for R_{SET} and R_{SNS} such that when $I_O = I_{CR}$,

$$Io*R_{SNS} = I_{SET}*R_{SET} \quad \text{(EQ. 1)}$$

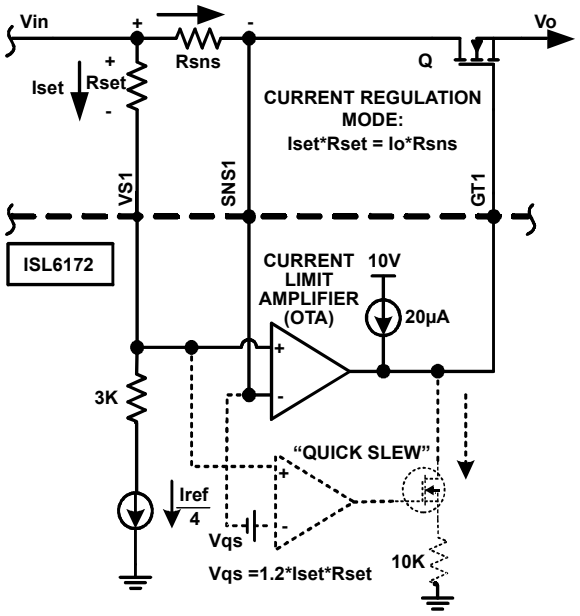


FIGURE 15. CURRENT REGULATION AND QUICK-SLEW OPERATION

The operating mode is shown in Figure 15 (please ignore the portion shown in dotted line for now). When the circuit enters this mode, increased voltage drop across the MOSFET is sensed by the OC comparator, which sets off the timer. CT begins to charge from an internal 10µA current source. The amount of time it takes for this cap to charge to 1.178V sets up the current regulation duration and upon expiration of which the MOSFET gate is pulled down by 80mA current sink unless the load current level drops back to a level below the current regulation threshold level prior to that. In that case, the current regulation mode is no longer active, the MOSFET is allowed to fully enhance and the IC discharges the C_T Cap. If $\overline{RTR}$/LTCH pin is left open or pulled to BIAS, the output remains latched off after the expiration of the time-out period determined by C_T. If $\overline{RTR}$/LTCH pin is pulled to GND, the IC automatically retries to turn on the MOSFET after a wait period, during which C_T is charged and discharged 64 times and the retry attempt takes place on the 65th time. This wait period allows the MOSFET junction to cool down.

2. "Quick Slew" Mode: This mode comes into effect when the di/dt of the load is too fast for the current regulation to see and is 20% or more above the current regulation limit. It shares the same circuit block as the current regulation amplifier in the block diagram. The purpose of having this mode is to ensure the current does not go too high for too long. While in this mode, the gate of the MOSFET is allowed to be pulled down passively with an internal resistor of approximately 10K. Once the current level reaches the current regulation set level, the current regulation amplifier takes over.

3. Way Overcurrent (WOC) Mode: This mode is designed to handle hard shorts on the load side, which can result in very high di/dt. Typically, the current limit set for this mode is 300% of the current regulation limit. This mode uses a very fast comparator, which directly looks at the voltage drop across R_{SNS} and pulls the gate very quickly to GND (as shown in Figure 16) and immediately releases it. If the WOC is still present, the IC enters current regulation mode and the rest of the current regulation behavior follows as described earlier under current regulation mode.

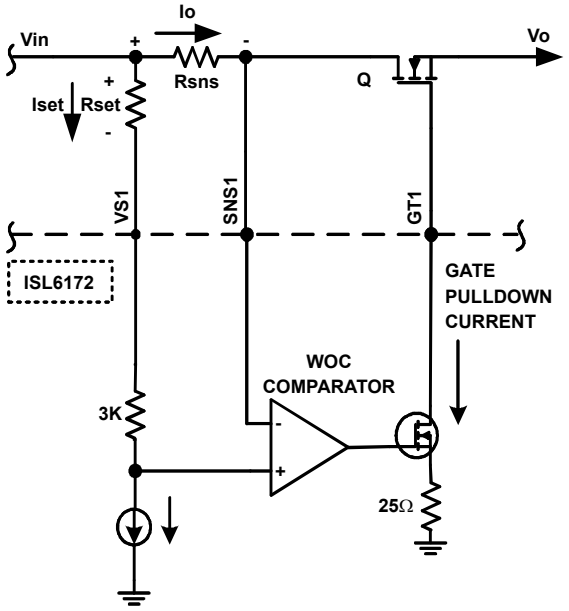


FIGURE 16. WOC OPERATION

Additionally, as shown in the block diagram, there is also an "OC comparator", which looks at the combined MOSFET and Rsense voltage drop. When the MOSFET drop exceeds the R_{SNS} drop by 60mV, timeout circuit starts ticking and CTx is allowed to charge. If the 60mV drop remains in effect until after the time-out period expires (CTx voltage exceeding 1.178V), the gate of the MOSFET is pulled down, SSx capacitor is discharged, FLT is asserted and a new SS sequence is allowed to begin after $\overline{ENx}$ recycle or by keeping the $\overline{RTR}$/LTCH pin pulled low.

The voltage on OCREF pin is the same as the internal band-gap reference voltage, which is 1.178V (nominal). A resistor to GND from this pin sets the reference current (and hence reference voltage) for the current limit amplifier and OC/WOC comparators. The current regulation (CR) duration is set by the capacitor on CT pin to GND. Once the voltage on this pin reaches 1.178V, the CR duration expires. Fault ($\overline{FLT}$) pin goes active (pulls low), signaling the load of a fault condition and the gate (GT) pin gets pulled low.

Retry vs Latched Fault Operational Modes:

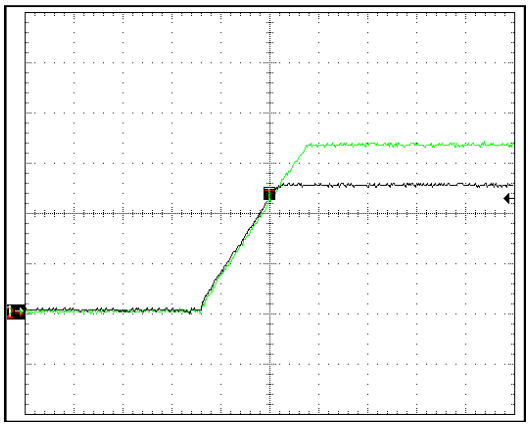
$\overline{RTR}$/LTCH pin dictates the IC behavior after the gate (GT) pin pulls down following a current regulation or OC or WOC condition. If the $\overline{RTR}$/LTCH pin is left floating, the gate pin will remain latched off. It can only be released by de-asserting and reasserting the enable ($\overline{EN}$) input. If $\overline{RTR}$/LTCH pin is pulled to GND, then the Retry mode will be activated. In this mode the IC will automatically attempt to turn-on the MOSFET after a delay, determined by the capacitor on CT pin. In the Retry mode, the internal logic charges and discharges the CT cap 64 times during "wait" period. On the 65th time, retry takes place. If the fault is cleared, the normal power up will continue and fault will clear. If not, the IC will continue to retry indefinitely.

Bias and Charge Pump Voltages:

The BIAS pin feeds the chip bias voltage directly to the first of the two internal charge pumps, which are cascaded. The output of the first charge pump, in addition to feeding the second charge pump, is accessible on CPVDD pin. The voltage on CPVDD pin is approximately 5V. It also provides power to the POR and band-gap circuitry as shown in the block diagram. A capacitor connected externally across CPQ+ and CPQ- pins of the IC is the "flying" cap for the charge-pump.

The second charge-pump is used exclusively to drive the gates of the MOSFETs through the 20µA current sources, one for each channel. The output of this charge pump is approximately 10V as shown in the block diagram.

Tracking



CH1: V_O1, CH2: V_O2, T = 2ms/DIV, C_{SS} = 0.066µF

FIGURE 17. TRACKING MODE WAVEFORMS

The two channels can be forced to track each other by simply tying their SS pins together and using a common SS capacitor. In addition, their $\overline{EN}$ pins also must be tied together. Typical Start-up waveforms in this mode are shown in Figure 17 above. If one channel goes down for any reason, the other one will too. One important thing to note here is that only the overcurrent latch-off mode will work. Autoretry feature WILL NOT work. Retry must be controlled manually through $\overline{EN}$.

TYPICAL HOT-PLUG POWER UP SEQUENCE

1. When power is applied to the IC on BIAS pin, the first charge pump immediately powers up.
2. If the BIAS voltage is 2.1V or higher the IC comes out of POR. Both SS and CT caps remain discharged and the gate (GT) voltage remains low.
3. $\overline{ENx}$ pin, when pulled low (below it's specified threshold), enables the respective channel.
4. SSx cap begins to charge up through the internal 10µA current source, the gate (GT) voltage begins to rise and the corresponding output voltage begins to rise at the same rate as the SS cap voltage. This is tightly controlled by the Soft-start amplifier shown in the block diagram.
5. CTx cap begins to charge at the same time as the corresponding SS cap.
6. Fault ($\overline{FLT}$) remains deasserted (stays high) and the output voltage continues to rise
7. If the output voltage reaches its full value before the corresponding CTx cap voltage reaches 1.178V, the latter gets discharged and the $\overline{FLT}$ remains deasserted. Else, the channel shuts down and $\overline{FLT}$ is asserted.
8. If the voltage on UV pin exceeds 633mV threshold as a result of rising Vo, Power Good ($\overline{PG}$) output goes active.
9. At the end of the SS interval, the SS cap voltage reaches CPVDD and remains charged as long as $\overline{EN}$ remains asserted or CT timer is not timed out. The latter indicates expiration of current regulation duration.

State Diagram

This is shown in Figure 18. It provides a quick overview of the IC operation and can also be used as a troubleshooting road map.

IC Operation State Diagram

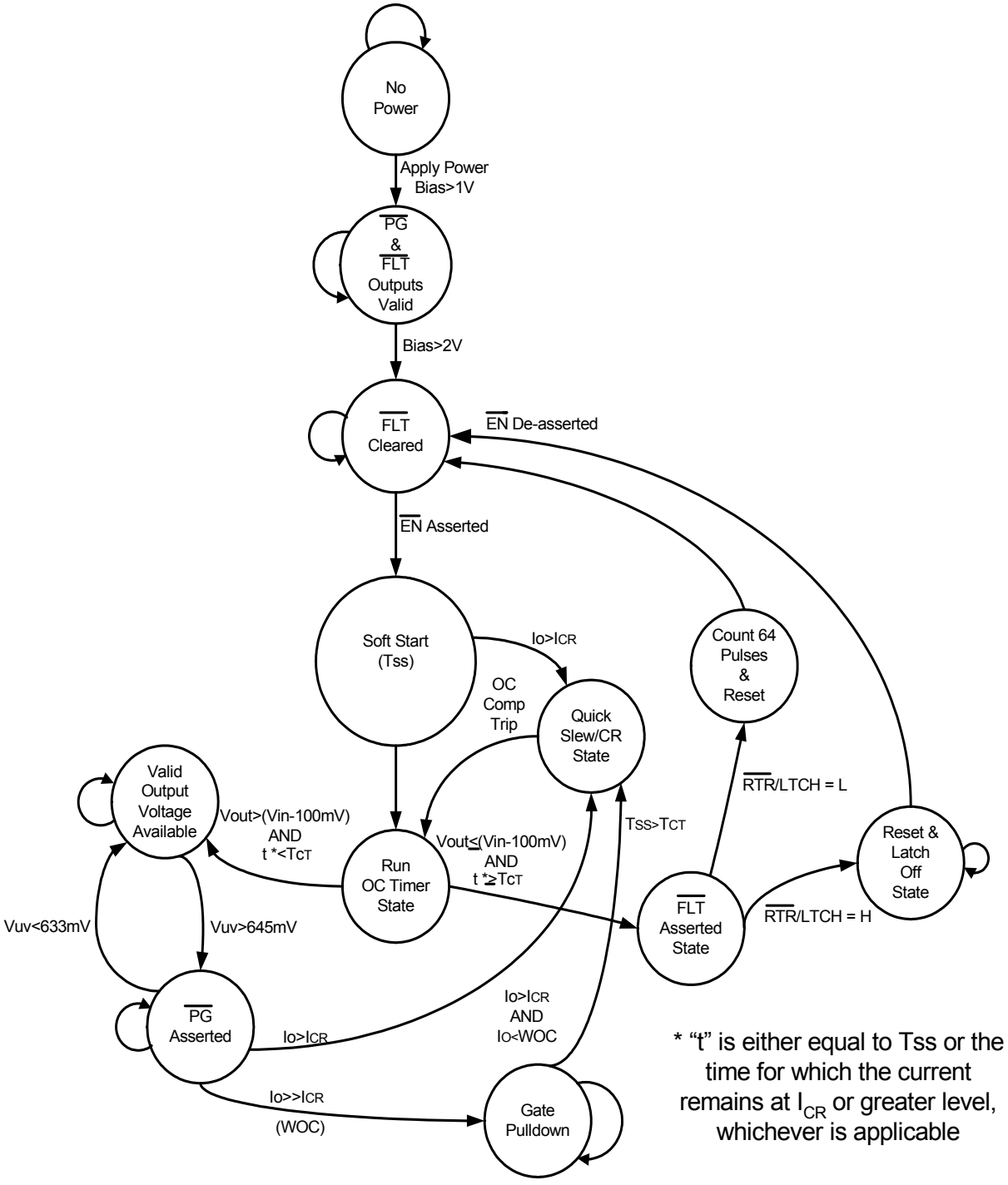


FIGURE 18.

Applications Information

Selection of External Components

Typical application circuit of Figure 2 has been used for this section, which provides guidelines to select the external component values.

MOSFET (Q1)

This component should be selected on the basis of its $r_{DS(ON)}$ specification at the expected Vgs (gate to source voltage). One needs to ensure that the combined voltage drop across the Rsense and $r_{DS(ON)}$ at the desired maximum current (including transients) will still keep the output voltage above the minimum required level. Power dissipation in the device under short circuit condition should also be an important consideration especially in auto-retry mode ($\overline{RTR}$/LTCH pin pulled low). Using ISL6172 in latched off mode results in lower power dissipation in the MOSFET.

Current Sense Resistor (R_{SNS})

The voltage drop across this resistor, which represents the load current (Io), is compared against the set threshold of the current regulation amplifier. The value of this resistor is determined by how much combined voltage drop is tolerable between the source and the load. It is recommended that at least 20mV drop be allowed across this resistor at max load current. This resistor is expected to carry maximum full load current indefinitely. Hence, the power rating of this resistor must be greater than $I_{O(MAX)}{}^2*R_{SNS}$.

Current Set Resistor (R_{SET})

This resistor directly sets the threshold for the current regulation amplifier and indirectly sets the same for the OC and WOC comparators in conjunction with R_{SNS}. Once R_{SNS} has been selected, use Equation 1 to calculate R_{SET}. Use 20µA for I_{SET} in a typical application.

Reference Current Set Resistor (R_{REF})

This resistor sets up the current in the internal current source, $I_{REF}/4$, shown in Figure 2 for the comparators. The voltage at the OCREF pin is the same as the internal bandgap reference. The current (I_{REF}) flowing through this resistor is simply:

$$I_{REF} = 1.178/R_{REF}$$

This current, I_{REF}, should be set at 80µA to force 20µA in the internal current source as shown in Figure 2, because of the 4:1 current mirror.

Selection of Rs1 and Rs2

These resistors should be selected based on where the user wants to set the UV detect point. The UV comparator detects the undervoltage condition when it sees the voltage at UV pin drop below 0.633V. The resistor divider values should be selected accordingly.

Charge Pump Capacitor Selection (C_P and C_V)

C_P is the “flying cap” and C_V is the smoothing cap of the charge pump, which operates at 450kHz set internally. The output resistance of the charge pump, which affects the regulation, is dependent on C_P value and its ESR, Charge-pump switch resistance, frequency and ESR of the smoothing cap, C_V. The output resistance can be approximately calculated using the following equation:

$$R_{OUT} = R_{INT} + 4*ESR_{C_P}+ESR_{C_V}+ [1/(f*C_P)]$$

Where,

R_{OUT} = Output Resistance

R_{INT} = Combined Internal Resistance (25Ω)

ESR_{C_P} = ESR of C_P

ESR_{C_V} = ESR of C_V

f = 450kHz

It is recommended that C_P be kept within 0.022µF (minimum) to 0.1µF (maximum) range. Only ceramic cap is recommended. Use 0.1µF cap if CPVDD output is expected to power an external circuit, in which case the current draw from CPVDD must be kept below 10mA.

C_V should at least be 0.47µF (ceramic only). Higher values may be used if low ripple performance is desired.

Time-out Capacitor Selection (C_T)

This capacitor controls the time-out period. As shown in Figure 2, when the voltage across this capacitor exceeds 1.178V, the time-out comparator detects it and pulls down the gate voltage thus shutting down the channel. An internal 10µA current source charges this capacitor. Hence, the value of this capacitor is determined by the following equation:

$$C_T = (10µA * T_{OUT})/1.178$$

Where,

T_{OUT} = Desired time-out period.

IMPORTANT NOTE: Selection of C_T and C_{SS} should be such that the soft-start period is always shorter than the time-out period. Otherwise the output will remain shut down.

Soft-Start Capacitor Selection (C_{SS})

The rate of change of voltage (dv/dt) on this cap, which is determined by the internal 10µA current source, is the same as that on the output cap. Hence, the value of this capacitor directly controls the inrush current amplitude during hot swap operation.

$$C_{SS} = C_O*(10µA/I_{INRUSH})$$

Where,

C_O = Load Capacitance

I_{INRUSH} = Desired Inrush Current

I_{INRUSH} is the sum of the dc steady-state load current and the load capacitance charging current. If the dc steady-state load remains disabled until after the soft-start period expires ($\overline{PG}$x could be used as a load enable signal, for example), then only the capacitor charging current should be used as I_{INRUSH}.

ISL6172 Evaluation Platform

The **ISL6172EVAL3** is the primary evaluation board for this family. The board is a standalone evaluation platform and it only needs input bias and test voltages.

The evaluation board has been designed with a typical application and accessibility to all the features in mind to enable a user to understand and verify these features of the IC. The circuit is designed for 2A for each input rail but it can easily be scaled up or down by adjusting some component values. LED indicators are provided to indicate Fault and/or Power Good status. The switches are there to perform Enable function for each channel and to select autoretry or latchoff mode.

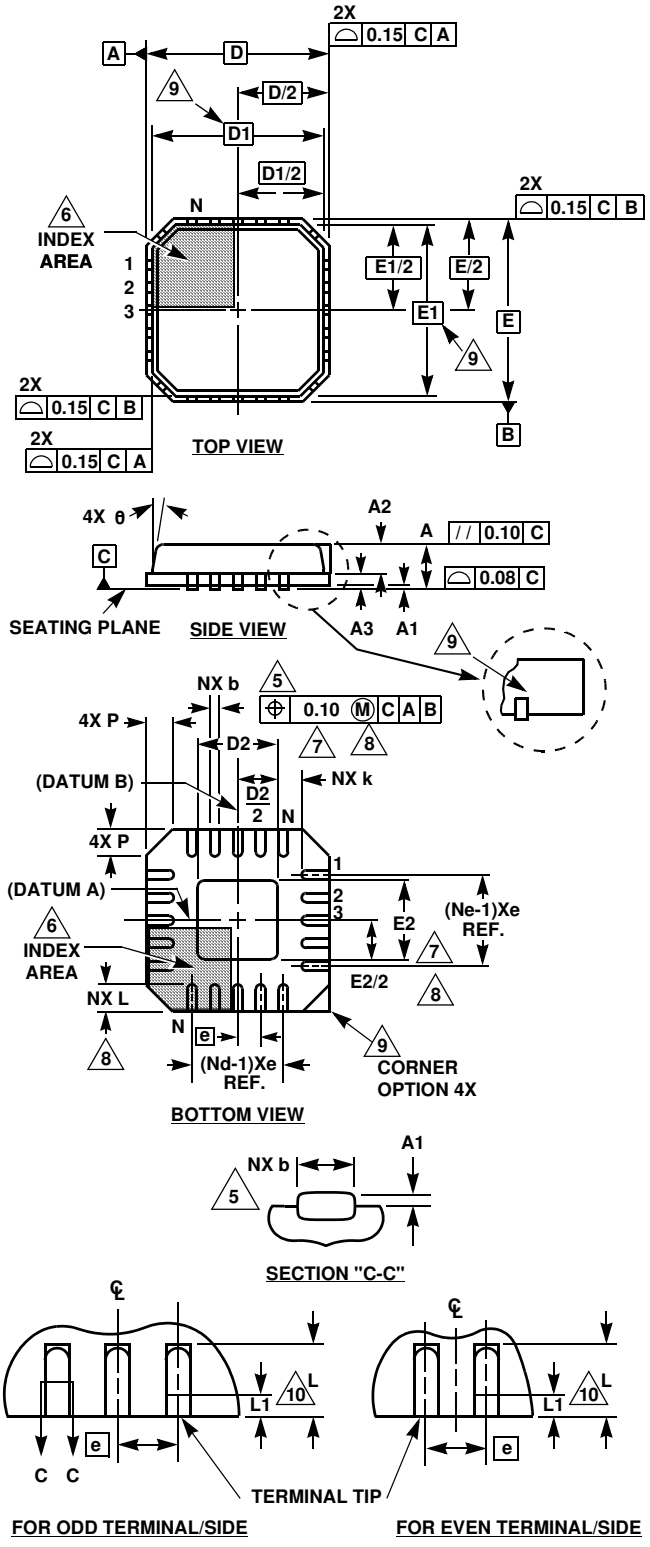
There are two input voltages, one for each channel plus there is optional “+5V” input. The latter is to test the pull-up capability of $\overline{FLT}$ and $\overline{PG}$ outputs to +5V. The loop jumpers are there to facilitate current measurement using an oscilloscope current probe.

Pins SS1 and SS2 of the IC are available on header J2 as test points so that they can be tied together to achieve tracking between Vo1 and Vo2.

Each channel is preloaded with capacitive and resistive loads. Extra load can be externally applied if necessary.

The outputs are brought out to banana sockets to allow external loading if desired.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L28.5x5

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		28		2
Nd		7		3
Ne	8	7		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 0 02/03

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.