Texas Instruments

TLV320AIC10/11 EVM

User's Guide

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AAP Data Converters

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Preface

Read This First

About This Manual

This document describes of the TLV320AIC10/11 EVM.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 – Introduction
- ❏ Chapter 2 – Physical Description
- ❏ Chapter 3 – Operation Modes
- ❏ Chapter 4 – Analog and Digital Interface
- ❏ Chapter 5 – Software Driver
- ❏ Chapter 6 – PC Board and Bill of Materials
- ❏ Appendix A – Schematics

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Chapter 1

Introduction

This chapter gives a general overview of the TLV320AIC10/11 evaluation module (EVM) and briefly describes the four functional sections on the EVM board.

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1.1 Features

The TLV320AIC10/11 evaluation module (EVM) is a daughterboard that plugs directly into the peripheral connector of TI's TMS320C5402 DSK (DSP starter kit) board. The board is populated with two TLV320AIC10/11 chips and has footprints for six more. The EVM provides a platform for evaluating the various operating modes and applications of AIC10/11 devices.

TLV320AIC10/11 devices are analog interface circuits (AIC), also called modem CODECs. They have 16-bit resolution and up to 22 kilosamples per second (KSPS) speed. The device is designed for use with TI's TMS320C5402 digital signal processors (DSP), or any other DSP or microprocessor that features the multichannel buffered serial port (McBSP) or synchronized serial peripheral interface (SPI).

For detailed specifications and applications of the TLV320AIC10/11, refer to TI's *General-Purpose 3-V to 5.5-V 16-bit, 22-KSPS DSP CODEC Data Manual* (SLWS093) and *General-Purpose Low-Voltage 1.1-V to 3.6-V I/O, 16-bit, 22-KSPS DSP CODEC Data Manua*l SLWS100).

For more information about TI's TMS320C5402 DSK, visit TI's web site at:

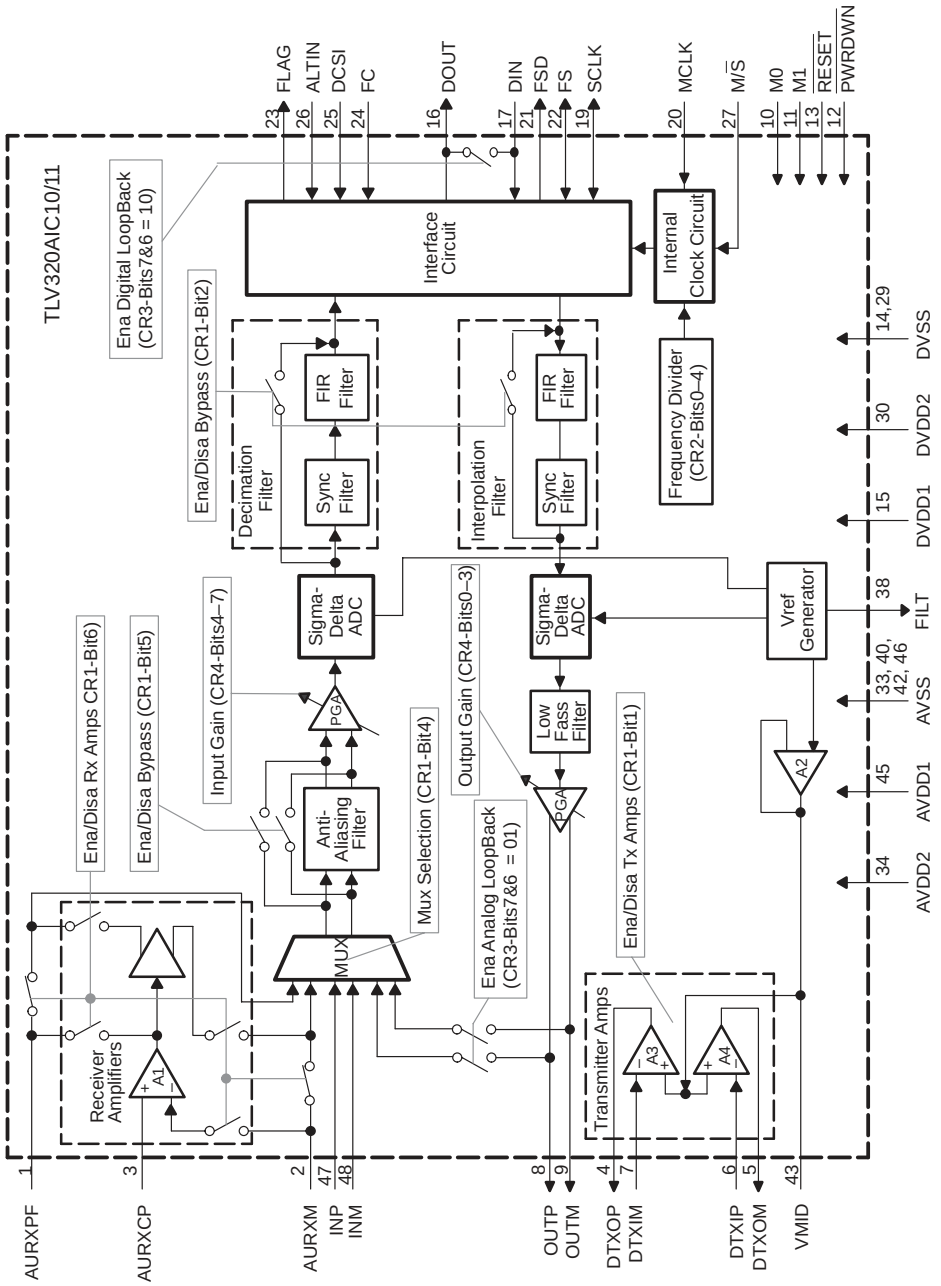
http://www.ti.com/sc/docs/tools/dsp/tmdx320005402.htm

1.2 TLV320AIC10/11 Device Block Diagram

The TLV320AIC10/11 device contains both analog-to-digital converter (ADC) and digital-to-analog converter (DAC) data paths. The ADC data path includes operational amplifiers for input signal conditioning, an input multiplexer, an antialiasing filter, a programmable gain amplifier, a Sigma-Delta ADC, and a decimation filter. The DAC data path comprises an interpolation filter, a Sigma-Delta DAC, a low-pass reconstruction filter, a programmable gain amplifier, and output transmit operational amplifiers. DSP interface circuitry, band-gap voltage reference, and clock generator/control circuits are also present in the AIC10/11 devices.

Figure 1–1 shows the block diagram of the TLV320AIC10/11 device, and includes the signal pinouts for the AIC10/11. The signals along the left side of the illustration are analog and interface to the application. Signals shown along the right side are digital and interface with the DSP and the other AIC10/11 devices and circuitry. There are four control registers (CR) in each AIC10/11 device. Each register requires configuration for proper operation.

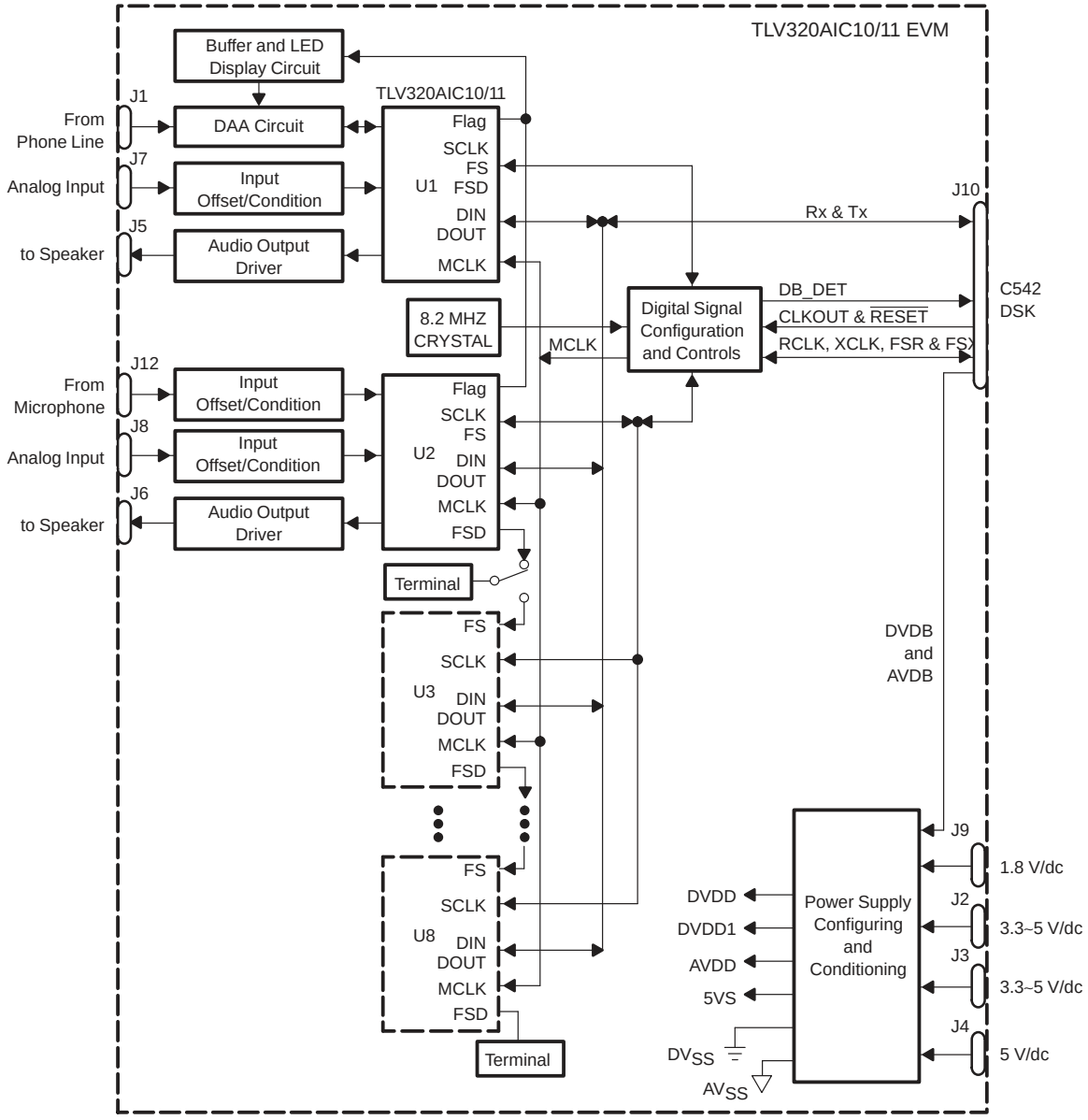
Figure 1–1. TLV320AIC10/11 Device Block Diagram



1.3 EVM Block Diagram

The TLV320AIC10/11 EVM system block diagram is illustrated in Figure 1–2. The EVM system not only provides an evaluation tool for the AIC device, it also gives an indication of the features and functions available for the hardware system configuration.

Figure 1–2. TLV320AIC10/11 EVM Block Diagram



As shown in Figure 1–2, there are four functional sections on the EVM board:

1) AIC10/11 devices and support circuits.The EVM is populated with two AIC10/11 devices and has footprints for six more. The unpopulated devices are illustrated with dashed lines. Also on the board are setup, configuration, and reset circuits that interface with all AIC10/11 devices.

2) Analog interface and support circuits. Two analog input conditioning and scaling circuits and one analog output driving circuit are onboard for each of the two populated AIC10/11 devices.

3) Digital interface and support circuit. The 80-pin connector from the EVM board to the TMS320C5402 DSK motherboard is the major digital interface circuit.

4) Power supply circuits. Power to the EVM board can be supplied from the motherboard or from external sources by configuring the onboard jumpers.

Chapter 2

Physical Description

This chapter describes the physical characteristics of the TLV320AIC10/11 EVM and lists the components used on the module.

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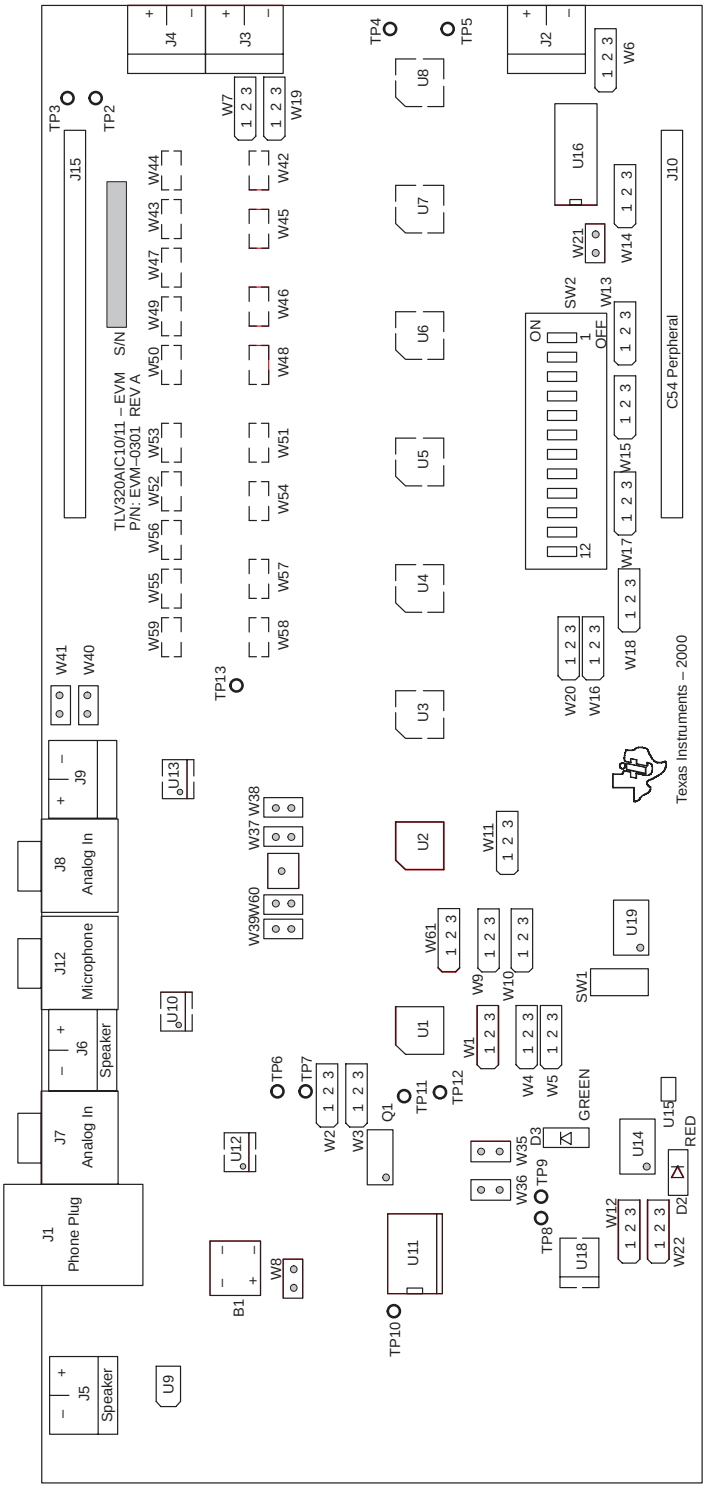
2.1 EVM Board Layout

Figure 2–1 shows the top view of the TLV320AIC10/11 EVM board and the locations of components that can be configured by the user. Configurable items include connectors, jumpers, switches, and buttons. The locations of major semiconductor chips and LEDs also are illustrated in Figure 2–1.

Figure 2–1. EVM Board Layout



2.2 EVM Connector Description

Table 2–1 lists all connectors on the EVM board. Table 2–2 gives the pin definition for power connectors J2, J3, J4 and J9. Table 2–3 specifies the two output connectors, J5 and J6. Table 2–4 describes J10, the 80-pin connector to the EVM system motherboard, TMS320C5402 DSK.

Table 2–1. EVM Connectors

Connectors	Number of Pins	Description
J1	–	Telephone plug for input to DAA circuit (to U1)
J2	2	Wire pair for 3.3-V to 5-V digital power supply (AIC10 only)
J3	2	Wire pair for 3.3-V to 5-V analog power supply
J4	2	Wire pair for 5-V analog power supply (5VS)
J5	2	Wire pair for speaker audio output (from U1)
J6	2	Wire pair for speaker audio output (from U2)
J7	–	Plug for analog input to U1
J8	–	Plug for analog input to U2
J9	2	Wire pair for 1.1-V to 3.6-V digital power supply (AIC11 only)
J10	80	Connector from/to DSP (TMS320C5402 DSK)
J12	–	Plug for microphone audio input (U2)
J15	80	(for board support only)

Table 2–2. EVM Connectors to Power Supplies

Connectors	Pin Position	Pin Definition
J2 (AIC10 only)	1 (upper)	To the positive of 3.3-V to 5-V power supply
	2 (lower)	To the negative of 3.3-V to 5-V power supply (digital ground)
J3	1 (upper)	To the positive of 3.3-V to 5-V power supply
	2 (lower)	To the negative of 3.3-V to 5-V power supply (analog ground)
J4	1 (upper)	To the positive of 5-V power supply
	2 (lower)	To the negative of 5-V power supply (analog ground)
J9 (AIC11 only)	1 (left)	To the positive of 1.1-V to 3.6-V power supply
	2 (right)	To the negative of 1.1-V to 3.6-V power supply (digital ground)

Table 2–3. EVM Connectors to Outputs

Connectors	Pin Position	Pin Definition
J5	2 (right)	To the positive (red) of speaker IN
	1 (left)	To the negative (black) of speaker IN
J6	2 (right)	To the positive (red) of speaker IN
	1 (left)	To the negative (black) of speaker IN

Table 2–4. EVM Connector to Motherboard

Connector	Pin No.	Pin Definition
J10	1	12 V
	2	–12 V
	3 and 4	Digital ground
	5	5 V, Digital
	6	5 V, Analog
	7 & 8	Digital ground
	9	5 V, Digital
	10 to18	Not used
	19	3.3 V, Digital
	20	3.3 V, Analog
	21	X_CLKX0, McBSP0 Tx clock
	22	Not used
	23	X_FSX0, McBSP0 Tx frame sync
	24	X_DX0, McBSP0 Tx data
	25 and 26	Digital ground
	27	X_CLKR0, McBSP0 Rx clock
	28	Not used
	29	X_FSR0, McBSP0 Rx frame sync
	30	X_DR0, McBSP0 Rx data
	31 and 32	Digital ground
	33	X_CLKX1, McBSP1 Tx clock
	34	Not used
	35	X_FSX1, McBSP1 Tx frame sync
	36	X_DX1, McBSP1 Tx data
	37 and 38	Digital ground
	39	X_CLKR1, McBSP1 Rx clock
	40	Not used
	41	X_FSR1, McBSP1 Rx frame sync
	42	X_DR1, McBSP1 Rx data

Table 2–4. EVM Connector to Motherboard (Continued)

Connectors	Pin No.	Pin Definition
J10	43 and 44	Digital ground
	45 to 50	Not used
	51 and 52	Digital ground
	53 to 58	Not used
	59	X_/RESET, Reset signal from motherboard
	60	Not used
	61 and 62	Digital ground
	63 to 74	Not used
	75	DB_DET, Daughterboard detector
	76 and 77	Digital ground
	78	X_CLKOUT, DSP CLKOUT Pin output signal = ½ CPU Freq
	79 and 80	Digital ground

2.3 EVM Jumper Description

The EVM has 28 user-configured jumpers on the board to allow maximum flexibility in design and applications for TLV320IC10/11 EVM owners. Table 2–5 describes the 28 jumpers and lists the manufacturer's default position for each jumper. Also, there are footprints on the board for an additional 18 jumpers associated with the 6 unpopulated AIC10/11 devices, U3 to U8. Refer to Figure 2–1, or the top layer printed-circuit board in Chapter 6, *PC Board and Bill of Materials*, for the location of all jumpers.

Table 2–5. EVM Jumper Description and Position

Jumper	Description	Position		
		1–2	2–3	Default
W1	AIC10/11 #1 Master/slave setting	Master	Slave	Master
W2	AIC10/11 #1 OUTP connection to DAA or audio driver	Audio Driver	DAA	Audio Driver
W3	AIC10/11 #1 OUTM connection to DAA or audio driver	Audio Driver	DAA	Audio Driver
W4	Communication sync mode (M0 and M1) configuration†	1	0	0 (Pulse Mode)
W5		1	0	
W6	DVDD1 from external (J2) or from motherboard (DVDB)	J2	DVDB	J2
W7	AVDD from external (J3) or from motherboard (AVDB)	J3	AVDB	J3
W8	DAA CPC5604 pin RXS to GND cap enable	Cap Enable		Disabled
W11	AIC10/11 #2 Master/slave setting	Master	Slave	Slave
W12	AIC10/11 #2 Pin FLAG output to /CID or NOT	/CID	NOT	/CID
W13	AIC10/11 #2 FS from DSP McBSP1 or AIC10/11 #1 FSD	McBSP1	FSD	1-2-3‡
W14	MS_CLOCK from DSP CLKOUT or onboard XTAL	CLKOUT	XTAL	XTAL
W15	AIC10/11 #2 SCLK from DSP McBSP1 or McBSP0	McBSP1	McBSP0	1-2-3‡

Table 2–5. EVM Jumper Description and Position (Continued)

Jumper	Description	Position		
		1–2	2–3	Default
W16	AIC10/11 #2 DIN from DSP McBSP1 or McDSP0	McBSP1	McBSP0	McBSP0
W17	AIC10/11 #2 DOUT from DSP McBSP1 or McDSP0	McBSP1	McBSP0	McBSP0
W18	DVDB from motherboard 5 V or 3.3 V	5 V	3.3 V	None
W19	AVDB from motherboard 5 V or 3.3 V	5 V	3.3 V	None
W20	DCSI from DSP McBSP1 to AIC10/11 #1, or both (#1&2)	AIC10/11 #1	AIC10/11 #1 and 2	1-2-3§
W21	Motherboard (C5402DSK) detecting AIC10/11EVM enable	Enabled		Enabled
W22	Hardware powerdown (PD) for AIC10/11s	PD Ena	PD Disa	PD Disa
W35	AIC10/11 #1 INP from DAA RX+ being connected or not	Conn		Conn
W36	AIC10/11 #1 INM from DAA RX– being connected or not	Conn		Conn
W37	AIC10/11 #2 INM from J8 being connected or not	Conn		Conn
W38	AIC10/11 #2 INP from J8 being connected or not	Conn		Conn
W39	AIC10/11 #2 OUTM connected to audio driver or not	Audio Driver		Audio Driver
W40	FC is disabled (GND) or not	Disabled		Disabled
W60	AIC10/11 #2 OUTP connected to audio driver or not	Audio Driver		Audio Driver
W61	DVDD1 from J9 (AIC11)) or J2 (AIC10)	J9	J2	J2 for AIC10 or J9 for AIC11
W62	FSD tied high	Enabled		Enabled

† Refer to TLV320AIC10/11 Data Manual, Table 2–1 for serial interface modes.
‡ Short all 3 positions for using DCSI with DSP C54xx's SW driver.
§ Short all 3 positions for using DX of McBSP1 to send data to DCSI of both U1 and U2.

2.4 EVM Switch Description

Switch array SW2 connects the six unpopulated AIC10/11 devices (U3 to U8) to all digital data, control and configuration signals when switched to ON.

2.5 EVM Reset Button

Pressing pushbutton SW1 manually resets all onboard AIC10/11 devices.

2.6 EVM LED Description

FLAG pins of U1 and U2 control LEDs D2 and D3, respectively. The FLAG is a digital output of the AIC10/11 device, and can be programmed by the software driver to flash an LED on, thus indicating good communication between the AIC10/11 and the DSP. Table 2–6 shows the relationship between AIC10/11 device and LED.

Table 2–6. EVM LED Description

LED	LED Color	FLAG From
D2	Red	AIC10/11 U2
D3	Green	AIC10/11 U1

2.7 EVM Board Power Supply

The AIC10/11 EVM board requires three separate dc power sources. These power sources can be from the TMS320C5402 DSK motherboard or from external power supplies.

Two analog power sources are required. The 5 V supplied to connector J4 is used for the onboard DAA circuits and speaker output drivers. The supplied 3.3 V to 5 V to connector J3 is used for all other EVM analog circuits.

One dc power source is required for the EVM digital circuits. The EVM can be configured for using AIC10 or AIC11 devices by setting a jumper. Select position 2–3 of W61 for AIC10 devices, or position 1–2 for AIC11 devices. TLV320AIC10 devices require digital I/O power of 3.3 V to 5 V (connected to J9), and the TLV320AIC11 devices require digital I/O power of 1.1 V to 3.6 V (typically 1.8 V) connected to J2.

Chapter 3

Operation Modes

This chapter describes the master and slave operation modes of the TLV320AIC10/11 EVM.

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3.1 EVM Operation Modes

TLV320AIC10/11 devices have two operation modes, master or slave. The device is a master device if it generates the shift clock (SCLK) and frame sync signal (FS) and sends them to slave devices. A slave device uses external SCLK and FS signals.

The TLV320AIC10/11 EVM board is populated with two TLV320AIC10/11 devices and has footprints and basic circuits for six more such devices. The two populated AIC10/11s (U1 and U2) can be configured as two separate masters or slaves to interface with the McBSP0 and McBSP1 on TMS320C5402 DSK. The separate master/slave operation modes are shown in Table 3–1. The devices can also be cascaded to connect to McBSP0, as is shown in Table 3–2.

Table 3–1. Separate Operation Modes

McBSP0	McBSP1	AIC10/11 U1	AIC10/11 U2
Master	—	Slave	—
Slave	—	Master	—
—	Master	—	Slave
—	Slave	—	Master

Table 3–2. Cascaded Operation Modes

McBSP0	AIC10/11 U1	AIC10/11 U2	AIC10/11 U3 to U8 (not populated)
Master	Slave	Slave	Slave(s)
Slave	Master	Slave	Slave(s)

By EVM design, AIC10/11 device U1 interfaces with McBSP0 only, and can be configured as a master or slave of McBSP0. Device U2 interfaces with both McBSP0 and McBSP1. U2 can be configured as a master or slave of McBSP1, or as a slave of U1 interfacing with McBSP0. Setup of the onboard jumpers is required for proper operation.

3.1.1 AIC10/11 Master Mode

A TLV320AIC10/11 device is configured as a master if the M/S pin of the device is pulled high. The master device generates the SCLK and FS.

If the number of cascaded AIC10/11 = 1 to 4: Frequency of SCLK = MCLK/N

If the number of cascaded AIC10/11 devices = 5 to 8:
Frequency of SCLK = 2*MCLK/N

Where frequency divider N = 1, 2, …. 32.

The frequency divider is programmable and is defined in AIC10/11 control register CR2. The powerup default value is 32.

AIC10/11 onboard device U1 works as a master to McBSP0 (and/or to other AIC10/11 devices) when the M/S pin is set to high. Device U2 works as a master to McBSP1, not only when the M/S pin is set to high, but also when jumpers W13, W15, W16, and W17 are configured to position 1–2.

3.1.2 AIC10/11 Slave Mode

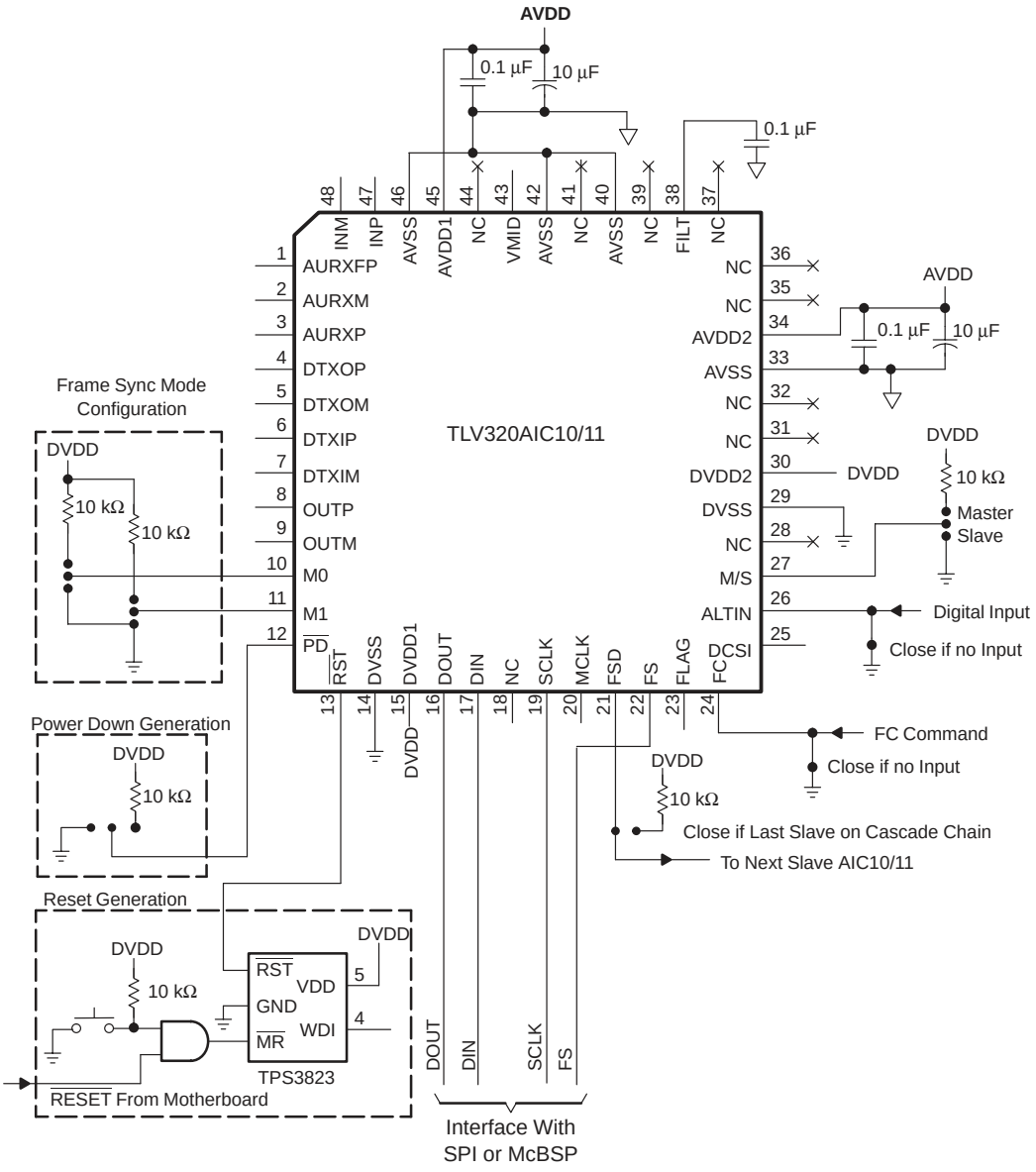
A TLV320AIC10/11 is configured as a slave device if the M/S pin is pulled low. In the slave mode, the device receives both the shift clock (SCLK) and the frame sync (FS) as input signals. It receives SCLK from the master device and FS from either the master device or another slave device that is upstream in the cascade.

The onboard AIC10/11 device U1 works as a slave (to McBSP0) when the M/S pin is set to low. Device U2 works as a slave when the M/S pin is set to low and jumpers W13, W15, W16 and W17 are configured to position 1–2 (slave to McBSP1, and separate mode), or when the jumpers are configured to position 2–3 (slave to U1, and cascade mode).

3.2 Other Basic Configurations

Figure 3–1 shows other important basic configuration circuits that support the proper operation of an AIC10/11 device. If there is more than one AIC10/11 device working in cascade, only one *frame sync mode configuration (M0/M1)* circuit, one *powerdown generation ($\overline{PD}$)* circuit, and one *reset generation ($\overline{RESET}$)* circuit are needed for the system.

Figure 3–1. Basic Configuration Circuits



Chapter 4

Analog and Digital Interface

This chapter describes the analog and digital interface circuits of the EVM.

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4.1 Analog Interface Circuits

Two analog inputs and one analog output can be connected to the AIC10/11 device. The TLV320AIC10/11 EVM system has 4 input and 2 output connectors that interface to external analog circuits via the two populated (U1 and U2) AIC10/11 devices. Refer to Figure 1–2 for these connections. For the detail circuit design refer to Appendix A, *EVM System Schematics.*

4.1.1 Input Offset Converter Circuits

The EVM board has two input offset or bias converter circuits. External analog input to the offset bias circuits is via connectors J7 and J8. These circuits provide analog input to the AURXFP/AURXM pins of the AIC10/11 U1 and to the INP/INM input of AIC10/11 U2. Analog inputs to the bias circuits are single-ended signals. The inputs are converted to a differential signal ranging from 0 V to AVDD (AV_{DD}=3.3 V to 5 V) with the offset centered at VMID. Note that VMID=AV_{DD}/2, and can range from 1.5 V to 2.5 V.

The input offset or bias converter circuits use the TI TLV2462 (U12 and U13). The TLV2462 is a two-channel, low power, rail-to-rail input/output operational amplifier designed for single-supply portable applications.

4.1.2 DAA Interface

By connecting jumpers W2 and W3 to position 2–3, and populating jumpers W35 and W36, the CODEC U1 and U2 can be applied to interface with U11, the data access arrangement (DAA) chip, for communication with a PSTN via the standard RJ–11 modular jack J1. Refer to Table 2–5 for jumper descriptions, and to Figure 2–3 for jumper locations,

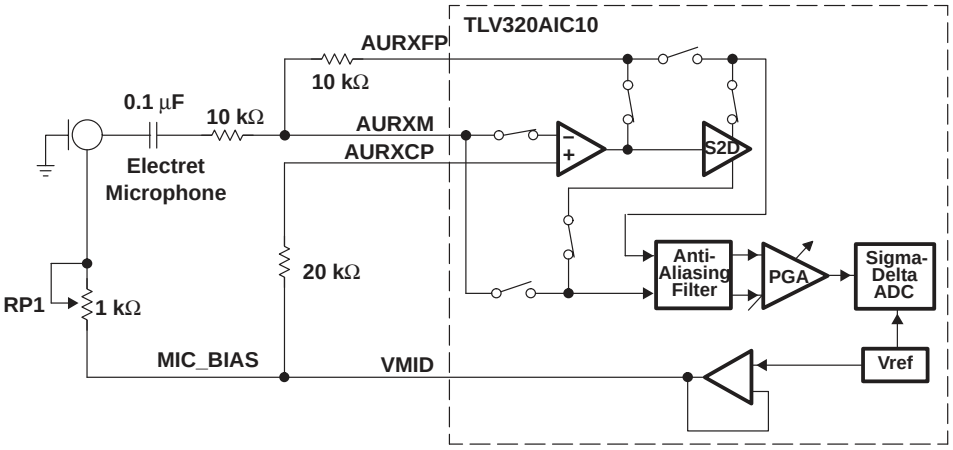
Telephone line input is via J1. The INP/INM and OUTP/OUTM of the AIC10/11 CODEC device U1 are connected to RX+/RX– and TX+ and TX–, respectively, of DAA U11. Device U1 also controls the off-hook (OH) signal of the DAA by programming the FLAG pin, and detects the DAA ring-detection signal (RING) through the ALTIN pin. CODEC device U2 controls the DAA Calling-ID (CID) signal by programming the pin FLAG. The operational amplifier (U18), as a logic buffer, provides the logic level to be used by the $\overline{OH}$ and $\overline{CID}$ pins of the DAA device.

4.1.3 Microphone Interface

The built-in receiver operational amplifier circuit of AIC10/11 device U2 can be programmed by the user to interface the device with the microphone input J12 (see Figure 1–1). The common mode of this on-chip circuit is referenced by VMID to bias or offset the microphone input signal. Figure 4–1 shows the recommended electret microphone interface to a TLV320AIC10/11 device.

It is important to note that the maximum current that can be drawn from the VMID output pin is $\leq$ 5 mA. While the circuit in Figure 4–1 illustrates an electret microphone, other types or models can be used without much trouble. However, a different value for RP1 will be required.

Figure 4–1. Microphone Interface With TLV320AIC10/11



Microphone Interface

4.1.4 Speaker Interface

The DAC signals of AIC10/11 U1 and U2 can be output to the two speaker drivers on the EVM board. A speaker driver circuit contains a TI TPA4861 audio power amplifier capable of delivering 1 W continuous average power into an 8 Ω load, typically a speaker. By setting jumpers W2 and W3 to position 1–2, the analog output of U1 is routed to the speaker driver. Similarly, by populating jumpers W39 and W60, the device analog output of U2 is routed to its onboard speaker driver. Connect external speakers to J5 (from U1) and J6 (from U2).

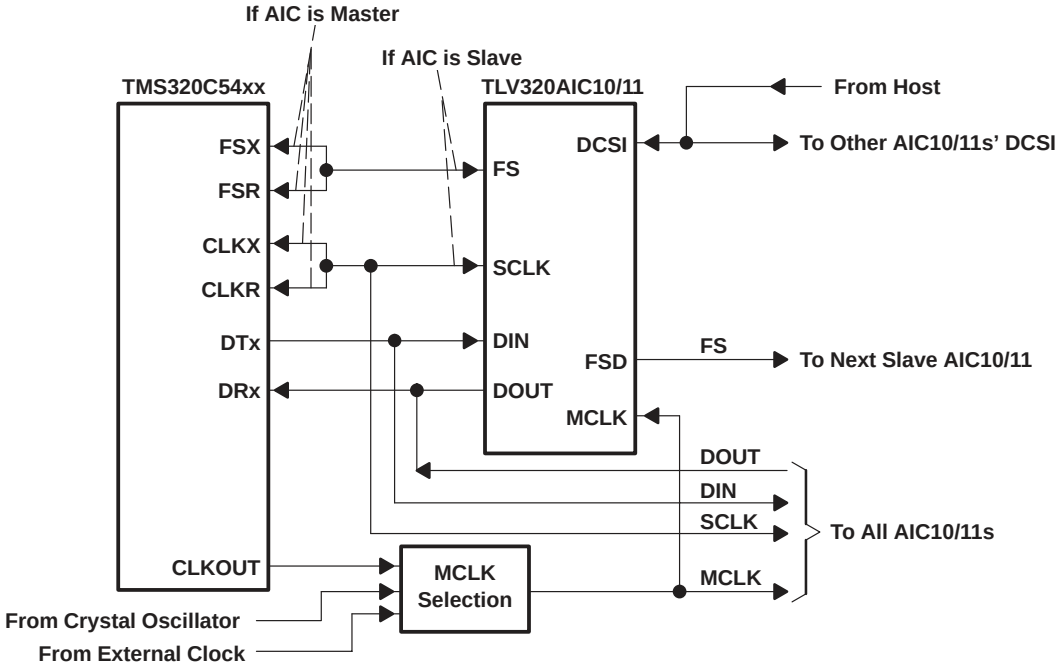
4.2 Digital Interface Circuits

This section describes the digital interface circuits of the EVM. Additional information for digital configuration and setup circuits is given in Chapter 3.

4.2.1 C5402 DSK McBSP Interface

Figure 4–2 illustrates the connection and data flow direction for C54xx DSP McBSP and TLV320AIC10/11 interface. The AIC10/11 devices U1 and U2 on the EVM board are designed to connect to the McBSP ports of the C5402 DSP via connector J10 (80 pin). Table 2–4 lists the interface connections for the EVM connector to the C5402 DSK motherboard.

Figure 4–2. C540x DSP McBSP and AIC10/11 Interface



4.2.2 Host Interface

The host interface on the AIC10/11 EVM is primarily designed for the AIC device direct configuration. When direct configuration of the AIC control registers via the DCSI pin is used, jumper W20 selects the serial data input source from either the motherboard DSK McBSP1 or from an external source.

4.2.3 MCLK Selection

The AIC10/11 EVM contains an onboard crystal oscillator that generates an 8.2 MHz clock. Installing jumper W14 to position 2–3 selects the onboard oscillator as the master clock source (MCLK) for onboard CODEC devices. Also, the DSP system clock (CLKOUT, at the ½ CPU frequency) is brought onboard the EVM from the motherboard through J10. Installing W14 to position 1–2 selects CLKOUT as MCLK source. An external clock source can be used as MCLK by removing jumper W14 and connecting the external clock to pin 2 (center pin) of W14.

4.2.4 AIC10/11 Device Digital Configuration

Operation and mode of the two TLV320AIC10/11 devices (U1 and U2) can be configured through the *digital signal configuration and controls* circuits. Refer to Figure 1–2 EVM Block Diagram in Chapter 1.

The *digital signal configuration and control*s circuits contain the jumper configurations that determine master/slave and separate/cascade operation mode. Other basic setup and configuration circuits, including the frame sync mode configuration circuit, reset generation circuit, and power-down generation circuit, are also used. These mode and circuit configurations are discussed in Chapter 3, *Operation Modes*.

Chapter 5

Software Driver

This chapter describes the software driver and application examples for the TLV320AIC10/11 EVM. There are three software versions available for downloading from the TLV320AIC10/11 development tool web site:

https://www_a.ti.com/apps/dc_plugins/aic10/11_register.asp)

The three software drivers are:

- ❏ AIC10 EVM Test Software
- ❏ TLV320AIC10/11 Plug-In for Code Composer Studio
- ❏ AIC10/11 EVM Software Driver and Application Examples

Topic **Page**

5.1 AIC10 EVM Test Software

Software drivers *aic10sw_m* and *aic10sw_ms* contain code for a single master codec and a master/slave cascade, respectively. The following C54xx software subroutines are included. They have been tested with the TI code composer, and they demonstrate how to program the C54xx DSK to control a cascade of master U1 and slave U2 on the AIC10/11–EVM.

- AIC10_DTMF.C
  This C-code serves as the main program and generates DTMF for phone numbers (customer supplied number; example: area code and seven digits) based on a sampling rate of 16 KSPS. It also contains two ISRs (interrupt service routines) for McBSP0 and McBSP1. McBSP0 services the master/slave cascading of the two TLV320AIC10/11s on the board, and McBSP1 programs the FLAG pin of both U1 and U2 using DCSI via jumper W20 to make LEDs D1 and D2 flash.

- C5402VEC.ASM
  This code defines the vector table for C54xx software.

- DCSI_COMM.ASM
  This code controls McBSP1 data transfer for TLV320AIC10/11's direct configuration (DCSI).

- INIT5402.ASM
  This code initializes the C5402 registers.

- MCBSP.ASM
  This code initializes the C5402's McBSP registers.

- INITAIC10.ASM
  This code detects master and slave codecs and initializes their four control registers to:

  - Set sampling rate at 16 KSPS.
  - Turn on OFF-HOOK for DAA interface with the master codec.
  - Enable the MIC preamp to receive input from the microphone.

- MS_COMM.ASM
  This code controls McBSP0 data transfer to/from the master TLV320AIC10/11 codec.

- SL_COMM.ASM
  This code controls McBSP0 data transfer to/from the slave TLV320AIC10/11 codec.

5.2 TLV320AIC10/11 Plug-In for Code Composer Studio

There are two examples for the AIC10/11 in this zip-file:

- Dial tone
- Sample

Dial tone demonstrates the write-block function of the AIC10/11 driver. It generates a sequence of dial tones based on a telephone number and puts it out on the master output.

Sample demonstrates the read-block function of the AIC10/11 driver. It reads a block of samples from the master and slave AIC10/11 and stores it in the DSP memory.

Unzip the file to the original folders and load the project file (AIC10/11_CCS.mak for both examples).

Dial Tone:

- Hook up a speaker to the master speaker port.
- Load the program to the DSP DSK and start it with F5.

Sample:

- Set a breakpoint at the dc_rblock function (line 38), load the program to the DSK and start the program with F5.
- After each cycle (F5), the data contains the samples from the AIC10/11 chain.
- Open a graph window to see the samples as a wave-form.

Note:
These subroutines have been tested using the C54xx C/ASM compiler Ver 3.1. If a different compiler version is used, the user may have to adjust the pipeline delay (that is, NOP) associated with McBSP code to meet the McBSP timing requirement.

The DSK is bundled with a special version of *Code Composer Studio*, allowing new designers to experiment with code composer features like real-time analysis and data visualization. *Code Composer Studio*'s unrivaled feature set makes DSP development easy. The DSK's special 32-K object code generation tool set allows users to experiment with sample code, test algorithms, and write their own application. Users have the flexibility of writing their application in C, making getting started easier than ever before.

For more information about the C5402 DSK, go to *http://www.ti.com/sc/docs/tools/dsp/tmdx320005402.htm*

New *Code Composer Studio* free evaluation tools (FETs) from TI are a full-featured, full-function, 30-day time-limited version of the C5000 DSPs software development tools and are now available for download at *http://www.ti.com/sc/docs/tools/dsp/5ccsfreetool.htm*

5.3 AIC10/11 EVM Software Driver and Application Examples

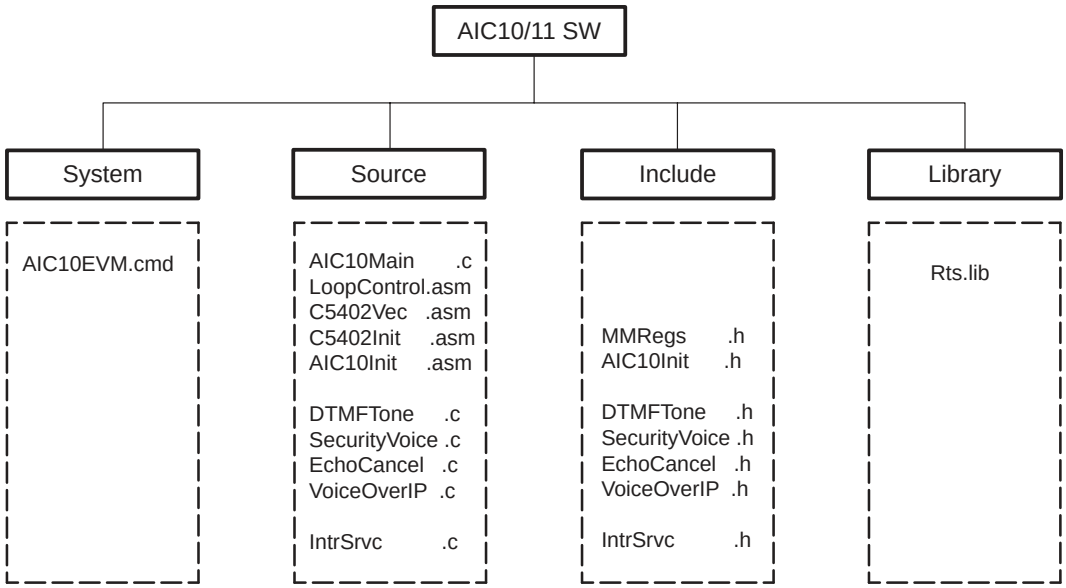
The newly developed software driver consists of the basic DSP McBSP and AIC10/11 software initialization or configuration programs. Also a *plug-and-play* algorithm is applied to perform the AIC10/11 hardware configuration auto-identification and configuration of the AIC10/11 control registers. The system driver programs are written in TMS320C54x assembly language.

Additionally, some application examples have been developed to help users in evaluating, testing, and applying the devices. These application examples are arranged into a main loop that repeats at a programmable rate, such as 16 KHz. Two interrupt service routines are developed. One interrupt service interfaces with McBSP0, and another routine interfaces with McBSP1. All application examples are in C code.

5.3.1 Software Structure

There are four groups of AIC10/11 software code: *system, source, include*, and *library*. Figure 5–1 illustrates the basic structure of the software code. The programs in the *system* group are mainly the DSP memory mapping and program linking commands. Those in the *source* group are the major programs. The head files in the *include* group define all variables or parameters for the corresponding source code. The *library* group contains the C54xx assembly library and other frequently used routines or macros.

Figure 5–1. Basic Structure of Software Code



5.3.2 System Management Source Programs

There are several source programs functioning as the EVM system management. These can be the same or very similar for different applications, and therefore can be reusable. They are:

- AIC10Main.c: Calls the system management and all application programs.
- LoopControl.asm: Main loop control to ensure the loop is running properly. Checks and displays the DSP status.
- C5402Vec.asm: Sets up C5402 interrupt vector table.
- C5402Init.asm: Initializes C5402 memory mapping registers (MMRs) and sets up the DSP for user applications.
- AIC10Init.asm: Reads from AIC10/11 devices to recognize the hardware configuration. Writes to CRs in all onboard AIC10/11 devices to control and initialize communications.

5.3.3 User Application Programs

There are several examples of application programs included with the EVM system, or supplied on the TI website. These application programs, as well as customer developed application programs, may be used. Example application programs are:

- DTMFTone.c: DTMF tone generation program
- SecurityVoice.c: Changes the microphone input to secure voice. The identity of voice over the speaker cannot be identified.
- EchoCancel.c: Echo cancellation program
- VoiceOverIP.c: VoIP program (under construction)

Chapter 6

PC Board and Bill of Materials

This chapter illustrates the PC board silkscreen and layers for Revision C of the AIC10/11 EVM and provides a bill of materials for the EVM, Rev. C.

Topic **Page**

6.1 Printed-Circuit Board (Rev. C)

This section illustrates the printed-circuit board for the TLV230AIC10/11 EVM.

Figure 6–1. Printed-Circuit Board (Rev. C, Top)

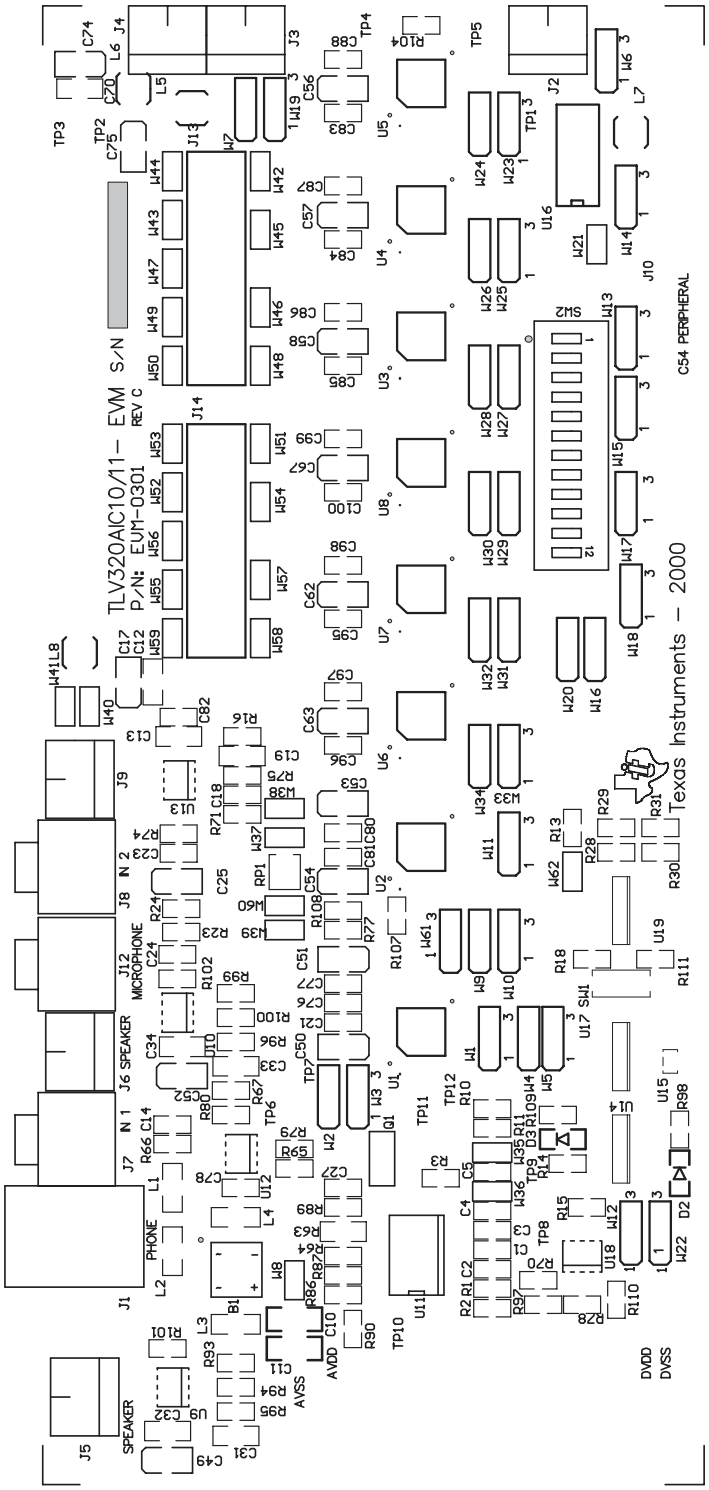


Figure 6–2. Printed-Circuit Board (Rev. C, Bottom)

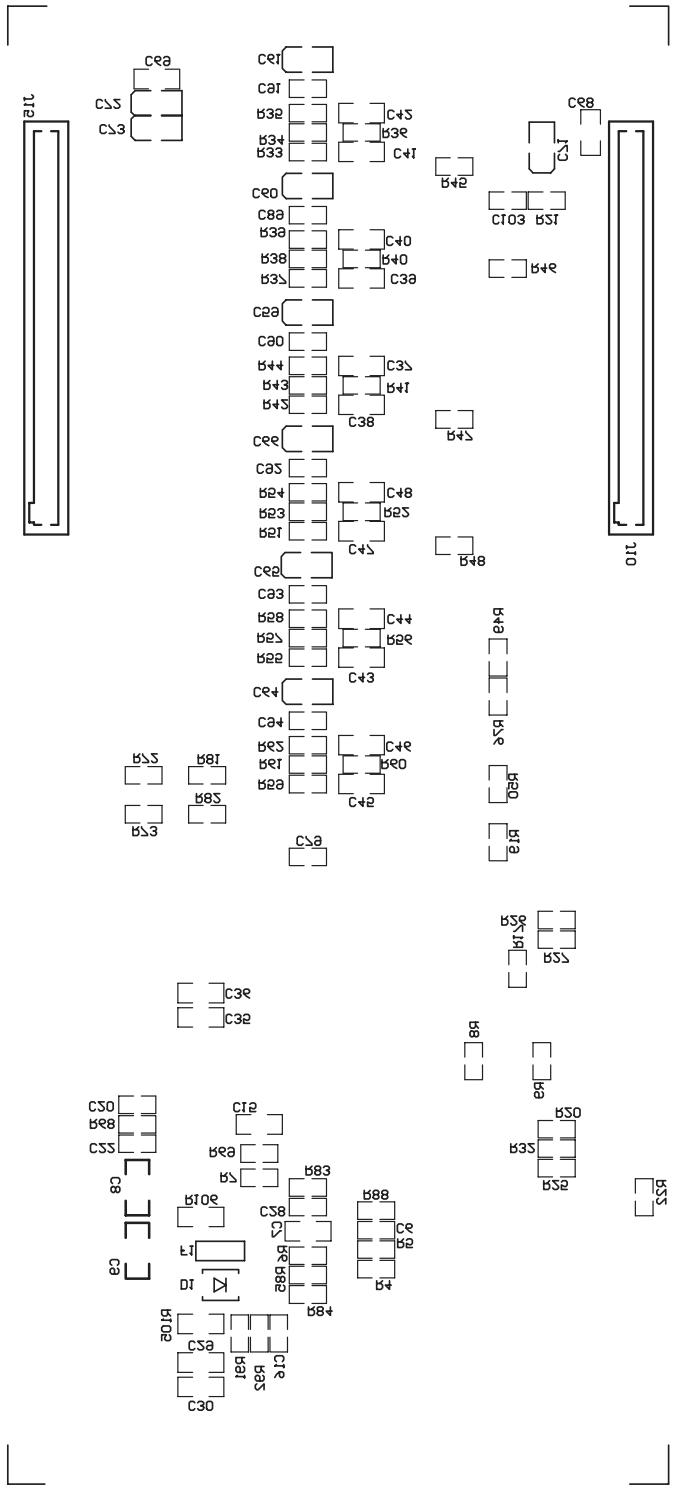


Figure 6–3. Printed-Circuit Board Layer 1 (Rev. C)

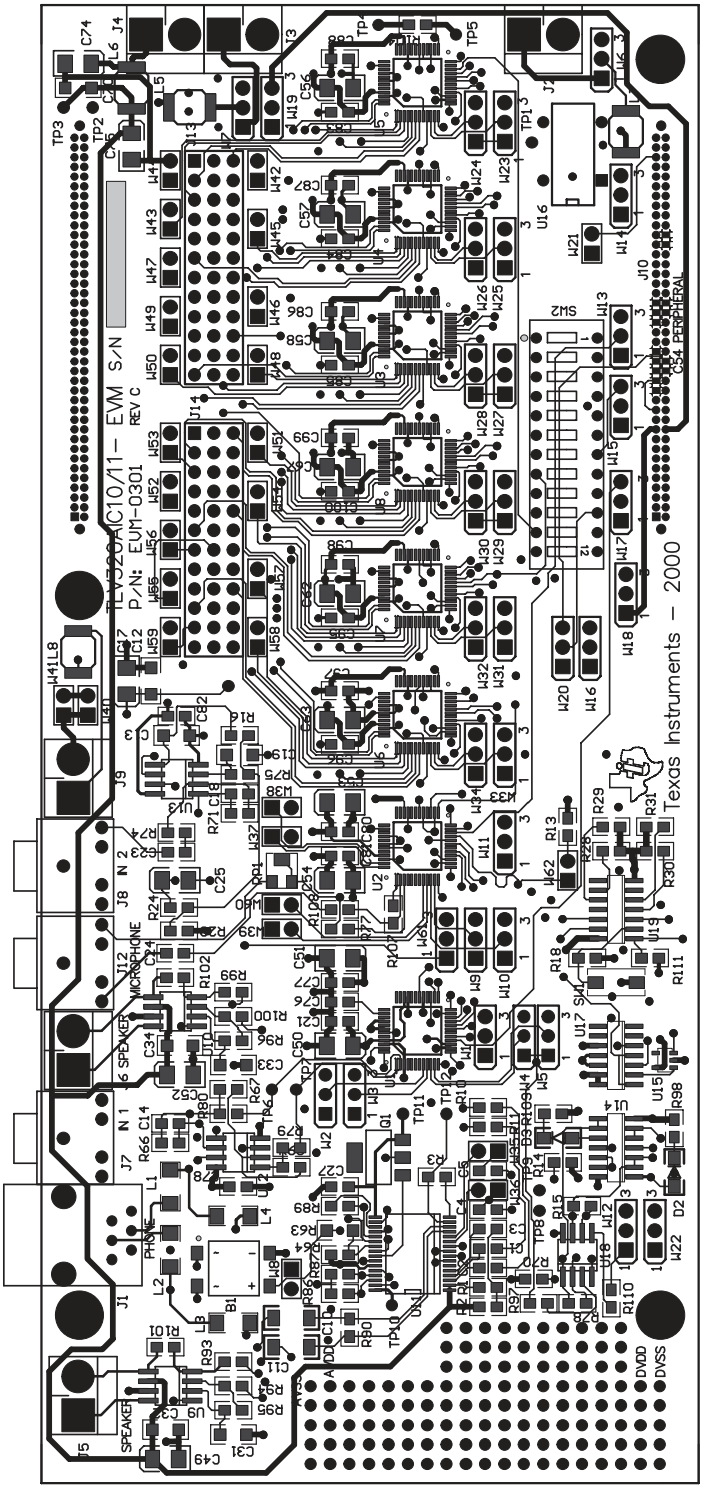


Figure 6–4. Printed-Circuit Board Layer 2 (Rev. C)

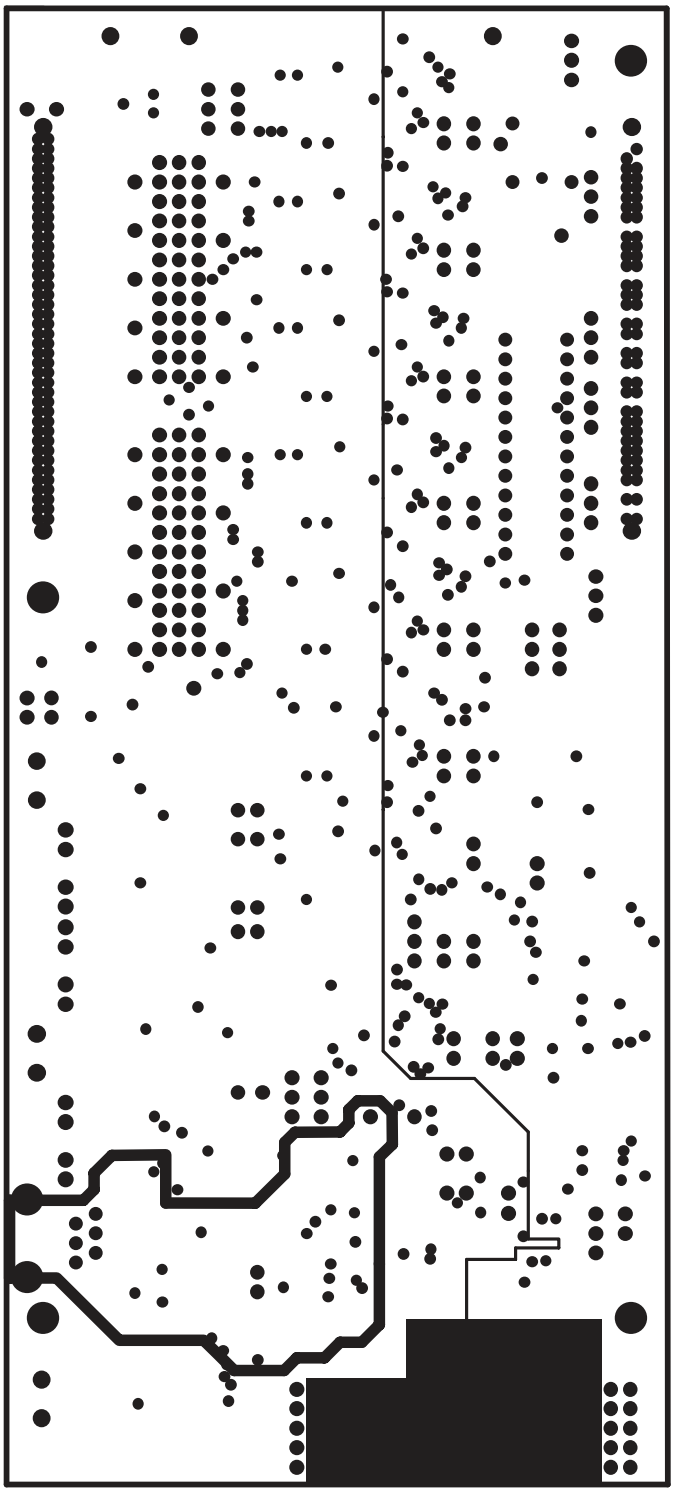


Figure 6–5. Printed-Circuit Board Layer 3 (Rev. C)

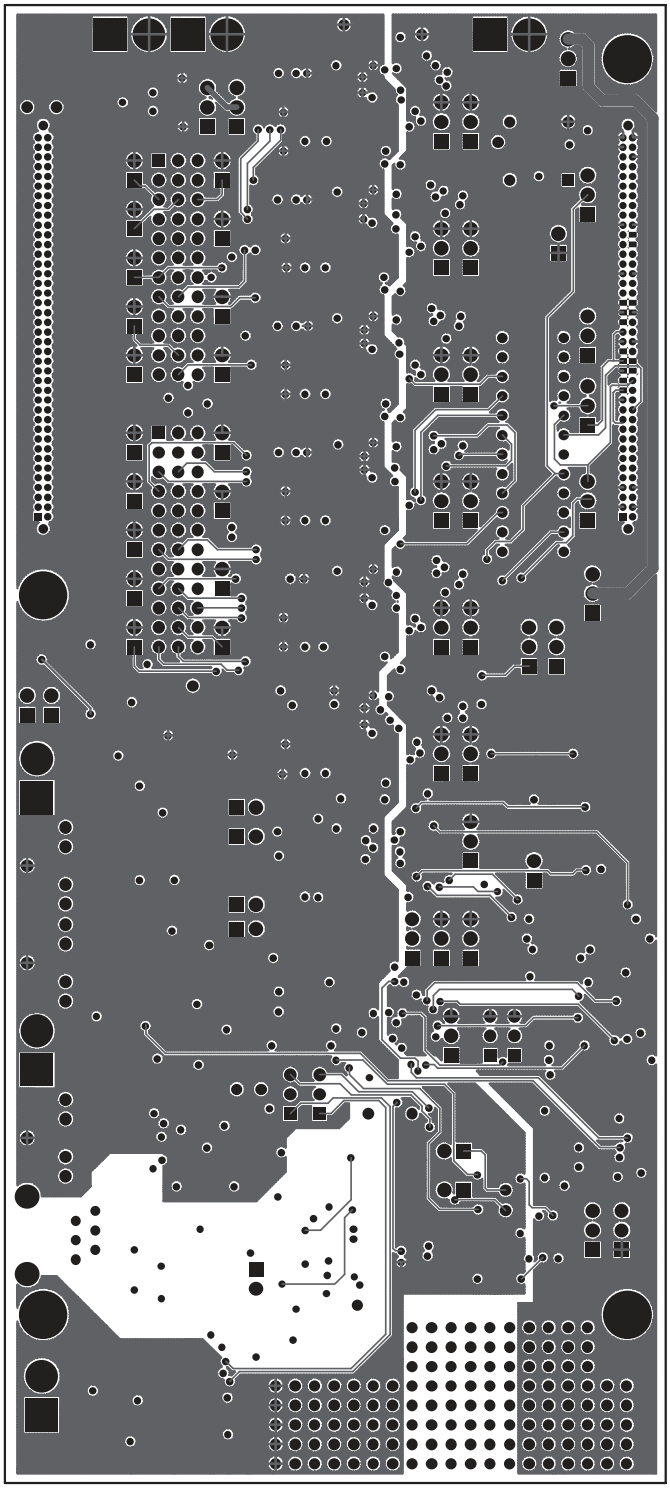


Figure 6–6. Printed-Circuit Board Layer 4 (Rev. C)

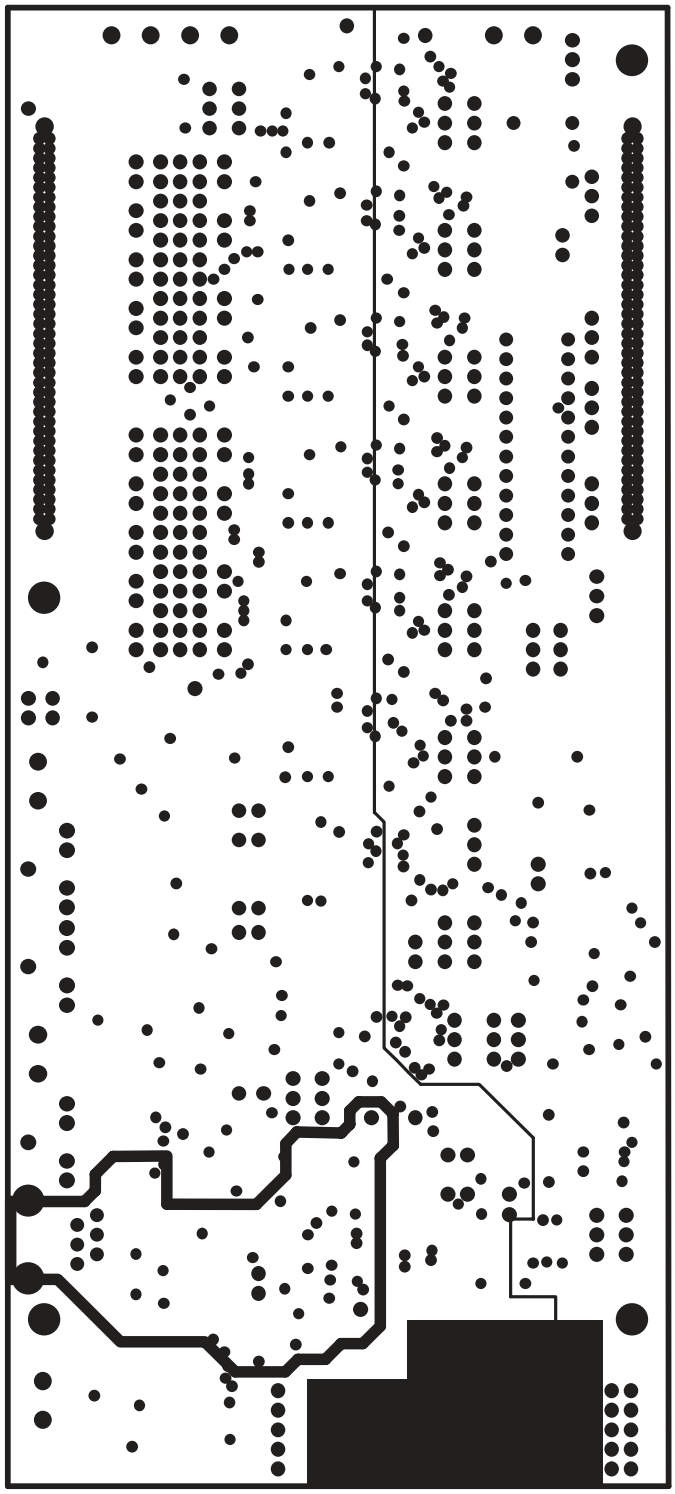


Figure 6–7. Printed-Circuit Board Layer 5 (Rev. C)

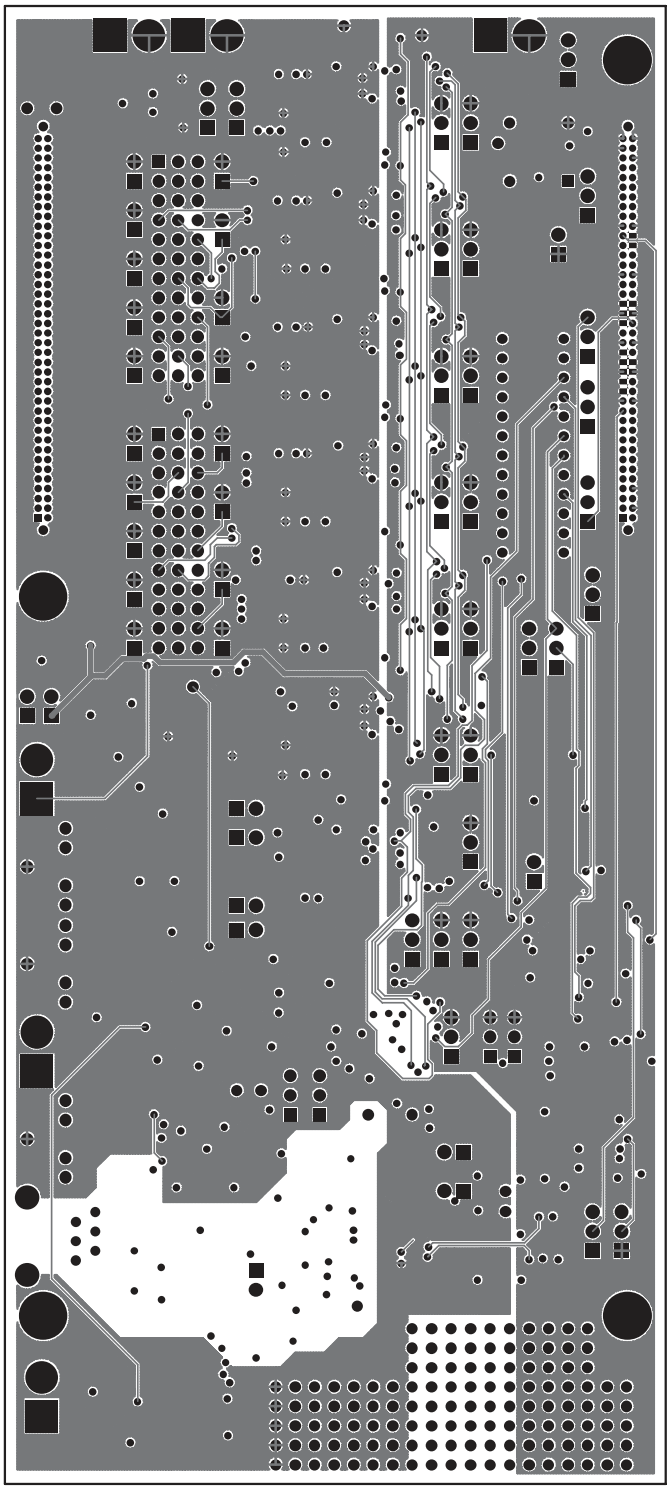
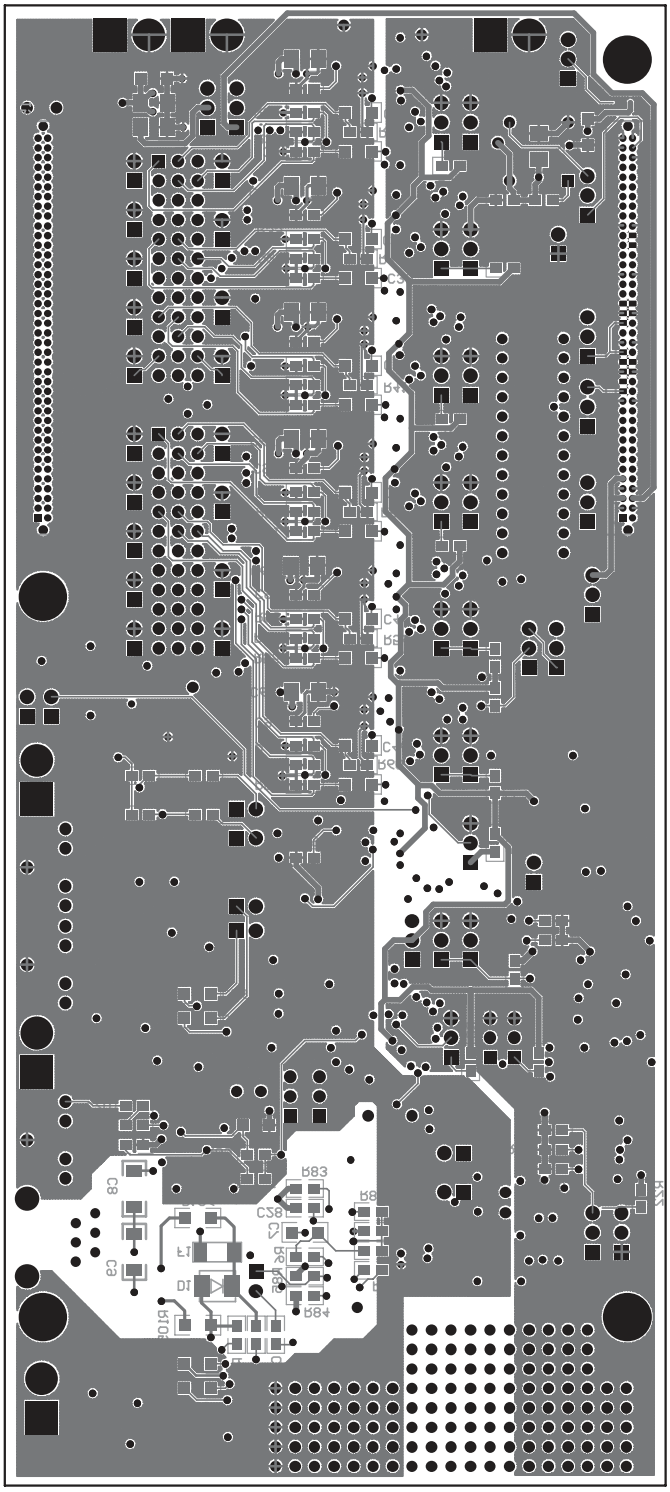


Figure 6–8. Printed-Circuit Board Layer 6 (Rev. C)



6.2 Bill of Materials (Rev. C)

Ref Des	Used	Part Type	Footprint	Description	Population Status
B1	1	SMT_BRIDGE	SAI_F27_1N	SHINDENGEN S1NB60 or Digikey DF06SGICT-ND	
C1 C100 C103 C104 C2 C20 C21 C23 C24 C3 C4 C5 C6 C76 C77 C78 C79 C80 C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99	36	0.1 µF	0805	Ceramic multilayer capacitor	
C10 C11 C8 C9	4	220 pF 2KV	1808	NOVACAP SP1808B221M202N	
C12 C13 C15 C19 C22 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C68 C69 C70	28	1 µF	1260	Ceramic multilayer capacitor	
C14 C18	2	560 pF	0805	Ceramic multilayer capacitor	
C16	1	4.7 nF	0805	Ceramic multilayer capacitor	
C17 C25 C49 C50 C51 C52 C53 C54 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 C71 C72 C73 C74 C75	25	10 µF	3528		
C27	1	0.01 µF	0805	Ceramic multilayer capacitor	
C28	1	0.47 µF	0805	Ceramic multilayer capacitor	
C7	1	0.001 µF 500 V	1206	NOVACAP 1206B102K501N	
D1	1	P3100SB	DO-214	TECCOR (Mouser 5191–P3100SA)	
D2	1	LED red	1206	Digikey L62201CT-ND	
D3	1	LED green	1206	Digikey L62205CT-ND	
F1	1	FUSE	3216-CHIP (1206)	WICKMANN 4431100000 1A 63 V Digikey WK4661CT-ND	
J1	1	RJ12	154–UL6663	Mouser RJ12 phone jack –PN 154-UL6663	
J10 J15	1	TFM-140	TFM-140	TFM-140-31-S-D	J15 TFM used for mechanical support
J12 J7 J8	3	PHONO_JACK	161-3504	PCB mount phone jack Mouser 161-3504	
J13 J14	2	12X3X.1	12X3X.1	36 pin header for PCB interconnect	DO NOT POPULATE
J2 J3 J4 J5 J6 J9	6	CON_2TERM_ SCREW	2term_screw_con	2-terminal screw connector	

Ref Des	Used	Part Type	Footprint	Description	Population Status
L1 L2 L3 L4	4	BEAD	1806	Taiyo Yuden FBMJ4516HM111N	
L5 L6 L7 L8	4	4.7 µH	DO1608C	DO1608C–Series – Coil Craft	
Q1	1	CPC5602C	4-SOT223	N-Channel FET, 4 pin SOT-223	
R1	1	200KΩ	805	RES, SMD, 0805	
R10 R107 R108 R11 R111 R13 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R6 R60 R61 R62 R8 R9	55	10KΩ	805	RES, SMD, 0805	
R100 R101 R102 R74 R77 R93 R94 R95 R96 R99	10	20KΩ	805	RES, SMD, 0805	
R104	1	0Ω	805	RES, SMD, 0805	
R105 R106	2	10Ω	1206	RES, SMD, 1206	
R16 R69 R7 R75	4	44KΩ	805	RES, SMD, 0805	
R2	1	604KΩ 1%	805	RES, SMD, 0805	
R3 R4	2	150KΩ	805	RES, SMD, 0805	
R5	1	10MΩ	805	RES, SMD, 0805	
R63	1	10MΩ, 1/4W	1206	RES, SMD, 1206	
R97 R110	2	11KΩ	805	RES, SMD, 0805	
R64	1	1.2MΩ	805	RES, SMD, 0805	
R14 R15 R65 R66 R67 R68 R70 R71 R72 R73 R74 R78	12	22KΩ	805	RES, SMD, 0805	
R76 R98 R109	3	1KΩ	805	RES, SMD, 0805	
RP1	1	1KΩ	TRIM POT	3214W-1-102E	
R79 R80 R81 R82	4	470Ω	805	RES, SMD, 0805	
R83	1	8.2Ω	805	RES, SMD, 0805	
R84	1	300Ω	805	RES, SMD, 0805	
R85	1	604Ω 1%	805	RES, SMD, 0805	
R86 R87	2	806KΩ 1%	805	RES, SMD, 0805	
R88	1	402Ω 1%	805	RES, SMD, 0805	
R89	1	100Ω	805	RES, SMD, 0805	
R90	1	1MΩ	0805	RES, SMD, 0805	
R91 R92	2	1.5MΩ	0805	RES, SMD, 0805	
SW1	1	SW-PB	EVQ–PJ	Panasonic EVQ–PJS05K	
SW2	1	SW 12 POS	X-435640-X	Dip switch, AMP 7100 series, 12 pos	
TP1 TP2 TP10 TP11 TP12 TP13 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9	13	TP_0.025	test_point2	SAMTEC TWS-101-07-L-S 0.025" pin	

Ref Des	Used	Part Type	Footprint	Description	Population Status
U1 U2 U3 U4 U5 U6 U7 U8	8	TLV320AIC10	48-TQFP (PFB)	TLV320AIC10	DO NOT POPULATE U3–U8
U10 U9	2	TPA4861	8-SOP (D)	TPA4861	
U11	1	CPC5604	32_SOIC	CPC5604	
U12 U13 U18	3	TLV2462A	8-SOP(D)	TLV2462A	
U14	1	SN74HC02	14-SOP (D)	Quad 2 input pos OR	
U15	1	TPS3823	5-SOT (DBV)	TPS3823	
U16	1	EPSON 8.200 MHz	4PIN_XTL_DC	EPSON SG-8002DC-SCC-8.200 MHZ	
U17	1	SN74HC74	14-SOP (D)	Dual D PET FF RS CR	
U19	1	SN74HC08	14-SOP (D)	Quad NAND gate	
W1 W10 W11 W12 W13 W14 W15 W16 W17 W18 W19 W2 W20 W22 W23 W24 W25 W26 W27 W28 W29 W3 W30 W31 W32 W33 W34 W4 W5 W6 W61 W62 W7 W9	34	3POS_JUMPER	3 pos_jump	SAMTEC TSW-103-07-L–S 0.1” spacing	DO NOT POPULATE W23–W28 W29–W34
W21 W35 W36 W37 W38 W39 W40 W41 W42 W43 W44 W45 W46 W47 W48 W49 W50 W51 W52 W53 W54 W55 W56 W57 W58 W59 W60 W8 W62	29	2POS_JUMPER	2 pos_jump	SAMTEC TSW-102-07-L–S 0.1” spacing	DO NOT POPULATE W42–W50 W51–W59
Jumper Hook Up Table TLV320AIC10					
W3 1–2		W2 1–2	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W11 2–3		W10 2–3	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W22 2–3		W7 1–2	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W36 SHORT		W21 SHORT	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W9 2–3		W1 1–2	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W6 1–2		W14 2–3	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W37 SHORT		W38 SHORT	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W20 1–2–3		W15 1–2–3	3 pos short	S.V.Tronics 70-0000-3	
W13 1–2–3			3 pos short	S.V.Tronics 70-0000-3	
W5 1–2		W4 1–2	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W17 2–3		W16 2–3	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W39 SHORT		W60 SHORT	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W41 SHORT		W35 SHORT	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
W61 2–3		W40 SHORT	2 pos short	SAMTEC SNT-100-BK–T or equivalent	
Jumper Hook Up Table TLV320AIC11					
W61 1–2			2 pos short	SAMTEC SNT-100-BK–T or equivalent	

Appendix A

Schematics

This Appendix contains the TLV320AIC10/11 EVM, Rev. C schematics.

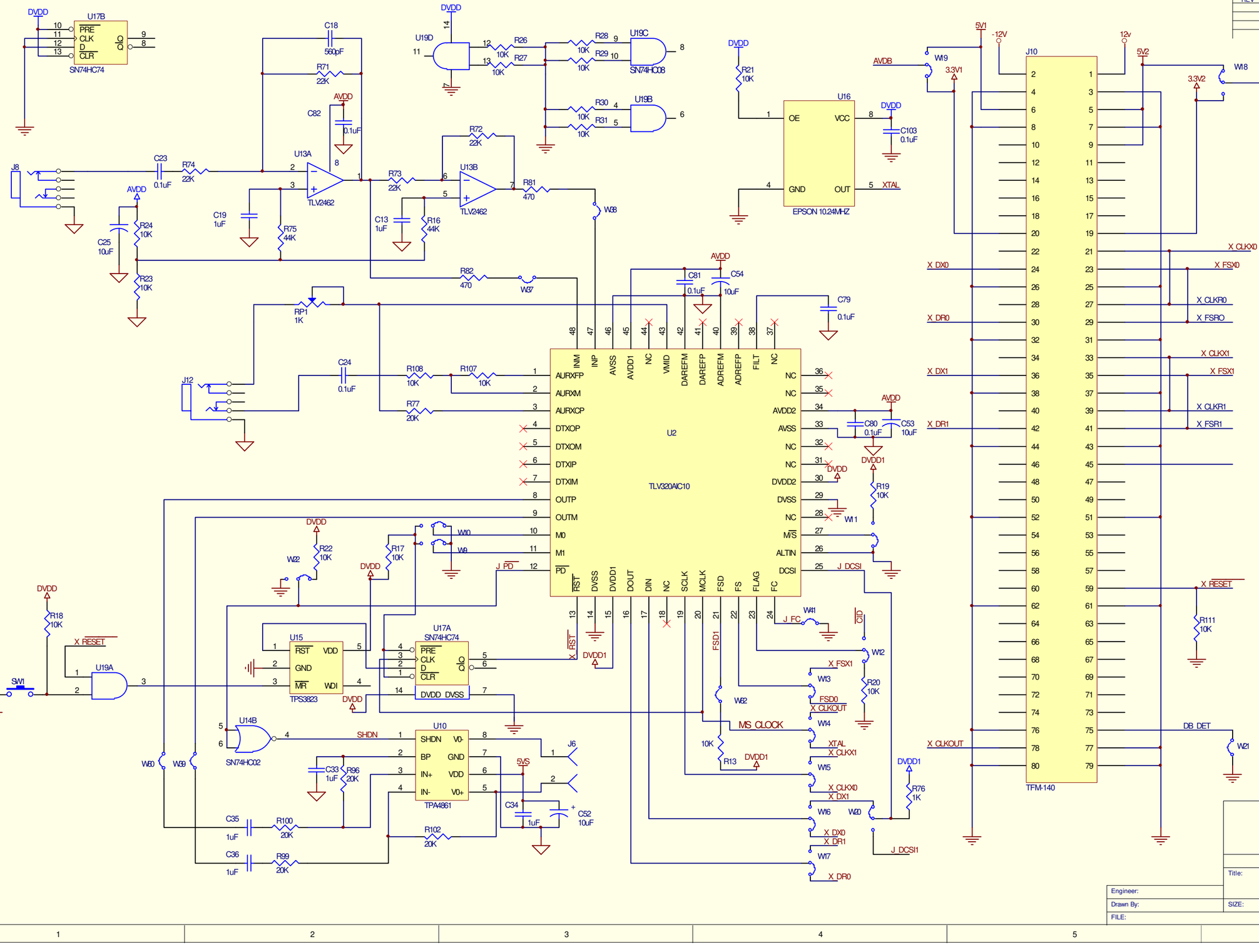
Revision History		
REV	ECN Number	Approved

U18B TLV2462 · U18A TLV2462 · U12A TLV2462 · U12B TLV2462 · U11 CPC5604 · U1 TLV320AIC10 · U9 TPA4861 · U14A · U14C · U14D

Q1 CPC5602C · B1 · D1 P3100SB · F1 FUSE · D2 Red · D3 Green · J1 RJ12 · J2 3.3V - 5.0V · J3 3.3V - 5.0V · J4 5V · J5 · J7 · J9 1.8V

Engineer:	12500 TI Boulevard. Dallas, Texas 75243
Drawn By:	Title: TLV320AIC10/11 EVM Schematic
FILE:	SIZE: · DATE: 18-Dec-2000 · REV: · SHEET: · OF:

Revision History		
REV	ECN Number	Approved



12500 TI Boulevard. Dallas, Texas 75243			
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Engineer:			
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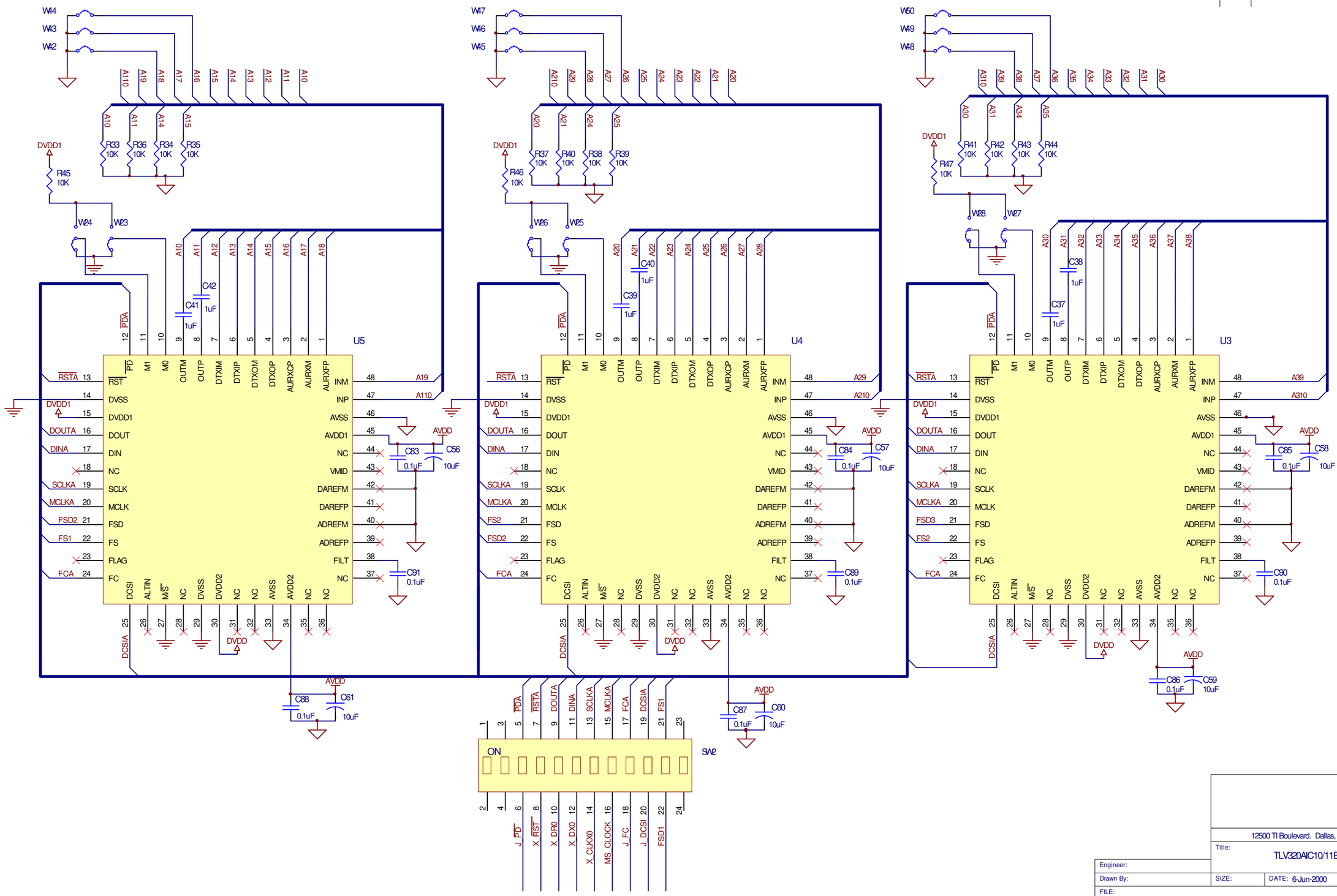
FILE:			SHEET: OF:

Revision History		
REV	ECN Number	Approved



12500 TI Boulevard. Dallas, Texas 75243			
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Revision History		
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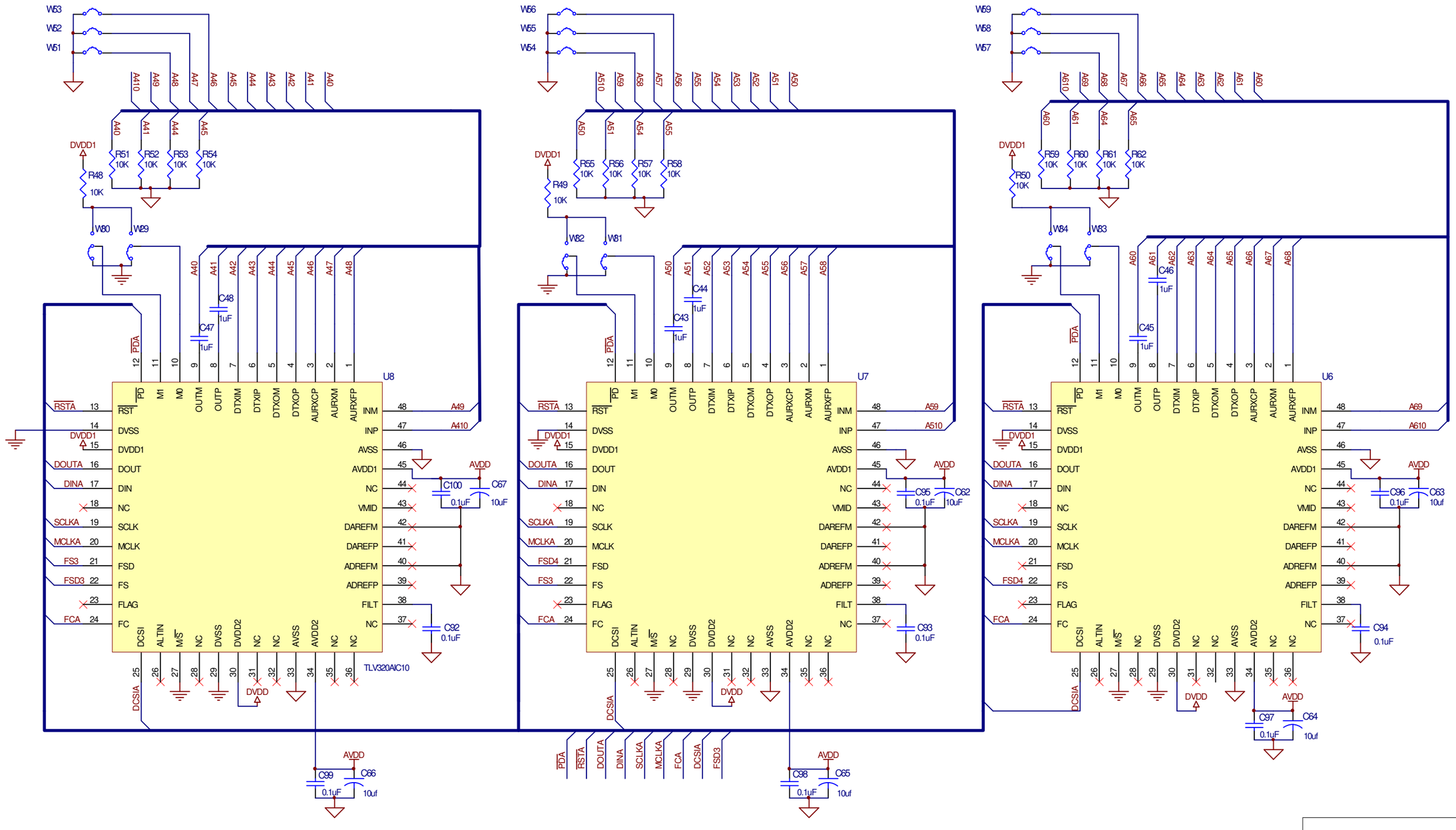

12500 TI Boulevard. Dallas, Texas 75243

Title: TLV320AIC10/11EVM

Engineer:			
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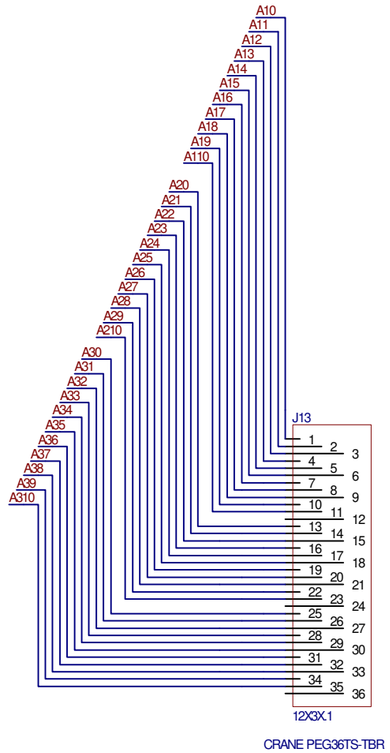
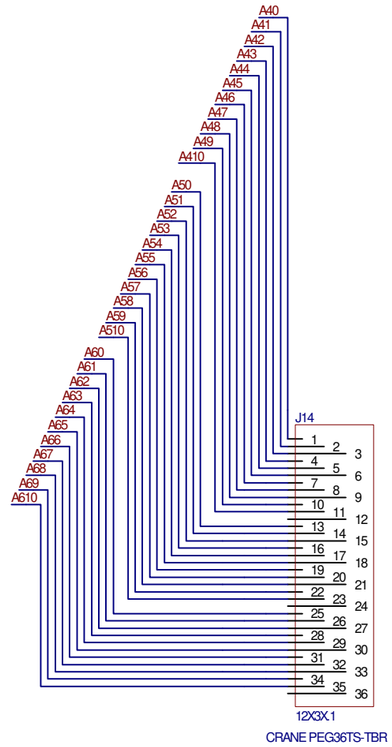
FILE:			SHEET: 4 OF: 5

Revision History		
REV	ECN Number	Approved



CRANE PEG36TS-TBR



CRANE PEG36TS-TBR

12500 TI Boulevard. Dallas, Texas 75243

Title: TLV320AIC10/11EVM

Engineer:			
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FILE:			SHEET: 5 OF: 5