

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## DESCRIPTION/ORDERING INFORMATION

This 1-bit to 4-bit address register/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

This device is ideal for use in applications in which a single address bus is driving four separate memory locations. The SN74ALVCH162832 can be used as a buffer or a register, depending on the logic level of the select ( $\overline{SEL}$ ) input.

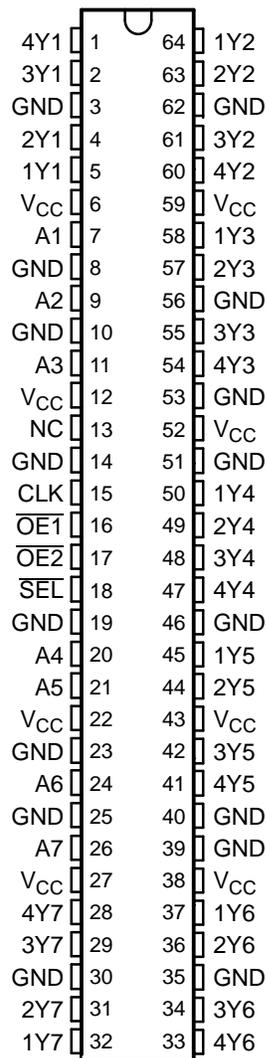
When  $\overline{SEL}$  is a logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable ( $\overline{OE}$ ) inputs. Each  $\overline{OE}$  controls two groups of seven outputs.

When  $\overline{SEL}$  is a logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data at the A inputs is stored in the internal registers.  $\overline{OE}$  controls operate the same as in the buffer mode.

When  $\overline{OE}$  is a logic low, the outputs are in a normal logic state (high or low logic level). When  $\overline{OE}$  is a logic high, the outputs are in the high-impedance state.

Neither  $\overline{SEL}$  nor  $\overline{OE}$  affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

DGG PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP - DGG    Tape and reel	SN74ALVCH162832GR	ALVCH162832

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**SN74ALVCH162832**  
**1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCAS588I–MAY 1997–REVISED SEPTEMBER 2004

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

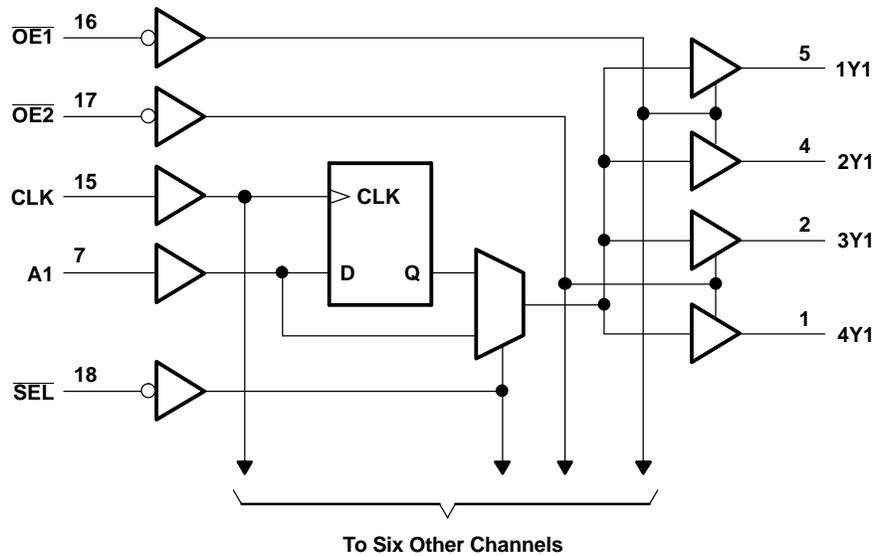
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**FUNCTION TABLE**

INPUTS				OUTPUT Y
$\overline{OE}$	SEL	CLK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through each V <sub>CC</sub> or GND		±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>		55	°C/W
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	-2	mA
		V <sub>CC</sub> = 2.3 V	-6	
		V <sub>CC</sub> = 2.7 V	-8	
		V <sub>CC</sub> = 3 V	-12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	2	mA
		V <sub>CC</sub> = 2.3 V	6	
		V <sub>CC</sub> = 2.7 V	8	
		V <sub>CC</sub> = 3 V	12	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCAS588I–MAY 1997–REVISED SEPTEMBER 2004

**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V
	I <sub>OH</sub> = -2 mA	1.65 V	1.2			
	I <sub>OH</sub> = -4 mA	2.3 V	1.9			
	I <sub>OH</sub> = -6 mA	2.3 V	1.7			
		3 V	2.4			
	I <sub>OH</sub> = -8 mA	2.7 V	2			
I <sub>OH</sub> = -12 mA	3 V	2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V	0.2			V
	I <sub>OL</sub> = 2 mA	1.65 V	0.45			
	I <sub>OL</sub> = 4 mA	2.3 V	0.4			
	I <sub>OL</sub> = 6 mA	2.3 V	0.55			
		3 V	0.55			
	I <sub>OL</sub> = 8 mA	2.7 V	0.6			
I <sub>OL</sub> = 12 mA	3 V	0.8				
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5			μA
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V	25			μA
	V <sub>I</sub> = 1.07 V	1.65 V	-25			
	V <sub>I</sub> = 0.7 V	2.3 V	45			
	V <sub>I</sub> = 1.7 V	2.3 V	-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V	3 V	-75			
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	±10			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	40			μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	750			μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	4.5			pF
	Data inputs		5			
C <sub>o</sub>	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND	7.5			pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

**TIMING REQUIREMENTS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	(1)		150		150		150		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	(1)		3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, A data before CLK↑	(1)		2		2		1.6		ns
t <sub>h</sub>	Hold time, A data after CLK↑	(1)		0.7		0.5		1.1		ns

(1) This information was not available at the time of publication.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			(1)		150		150		150		MHz
$t_{pd}$	A	Y	(1)		1.1	4.7	4.8		1.5	4.3	ns
	CLK		(1)		1	5.3	5.3		1.4	4.7	
	$\overline{\text{SEL}}$		(1)		1.1	6	6.2		1.5	4.8	
$t_{en}$	$\overline{\text{OE}}$	Y	(1)		1	5.9	5.9		1.1	5.1	ns
$t_{dis}$	$\overline{\text{OE}}$	Y	(1)		1.4	6.3	5.4		1.6	5.1	ns

(1) This information was not available at the time of publication.

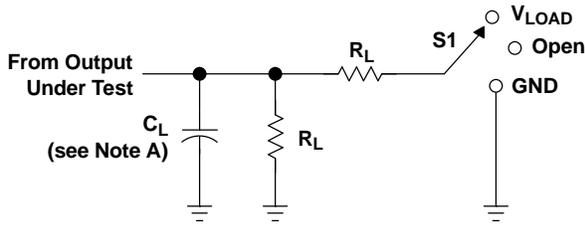
## OPERATING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance per bit (four outputs switching)	All outputs enabled	(1)	119	132	pF
		All outputs disabled	(1)	22	25	

(1) This information was not available at the time of publication.

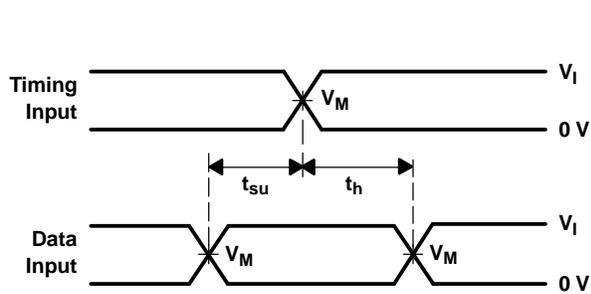
PARAMETER MEASUREMENT INFORMATION



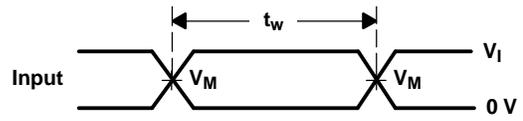
TEST	S1
$t_{pd}$ $t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PZH}$	Open $V_{LOAD}$ GND

LOAD CIRCUIT

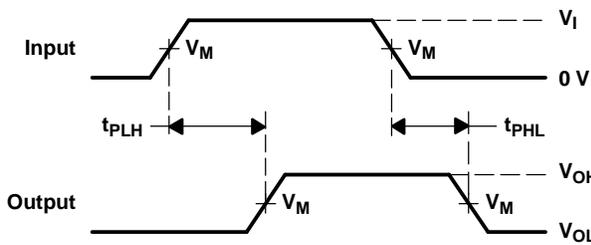
$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
1.8 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 V \pm 0.2 V$	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3 V \pm 0.3 V$	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



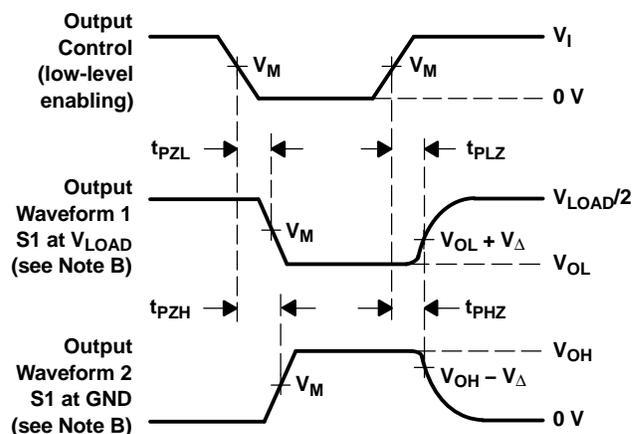
VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES

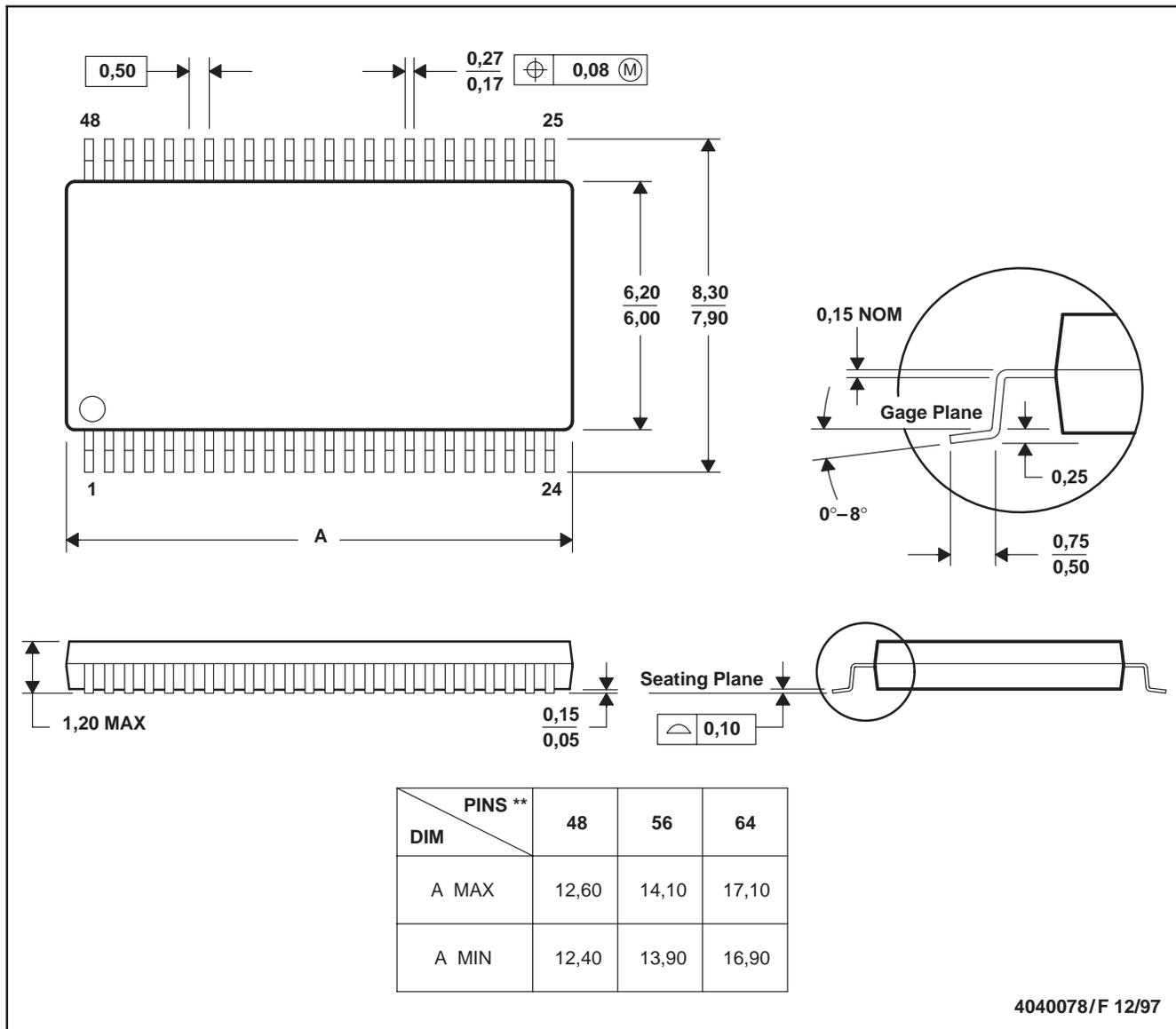
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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