HARRIS SEMICONDUCTOR

HI-524

August 1997

4-Channel Wideband and Video Multiplexer

Features

- Crosstalk (10MHz) . . . . . < -60dB
- Fast Access Time 150ns
- Fast Settling Time 200ns
- TTL Compatible

Applications

- Wideband Switching
- Radar
- TV Video
- ECM

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0524-5	0 to 75	18 Ld CERDIP	F18.3
HI1-0524-2	-55 to 125	18 Ld CERDIP	F18.3
HI4P0524-5	0 to 75	20 Ld PLCC	N20.35
HI3-0524-5	0 to 75	18 Ld PDIP	E18.3
HI1-0524-8	-55 to 125	18 Ld CERDIP	F18.3
HI1-0524/883	-55 to 125	18 Ld CERDIP	F18.3
HI4-0524/883	-55 to 125	20 Ld CLCC	J20.A

Description

The HI-524 is a 4-Channel CMOS analog multiplexer designed to process single-ended signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an enable input to inhibit all channels (chip select).

Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure the Crosstalk is less than -60dB at 10MHz.

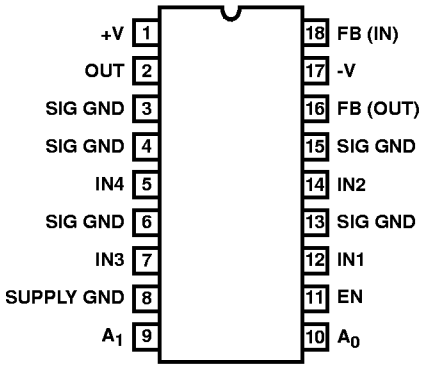
The HI-524 is designed to operate into a wideband buffer amplifier such as the Harris HA-2541. The multiplexer chip includes two "ON" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel r_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

The HI-524 is well suited to the rapid switching of video and other wideband signals in telemetry, instrumentation, radar and video systems.

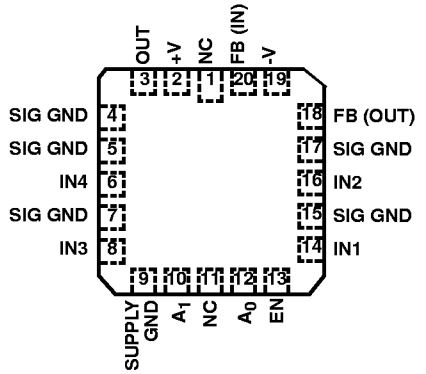
For MIL-STD-883 compliant parts, request the HI-524/883 data sheet.

Pinouts

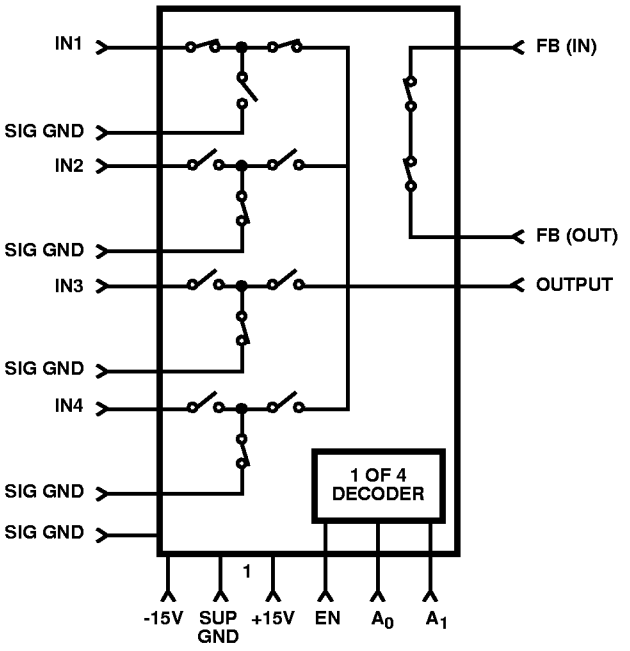
(CERDIP, PDIP)
TOP VIEW



(CLCC, PLCC)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3148.1**

Absolute Maximum Ratings

Voltage Between Supplies 33V
Digital Input Voltage
$+V_A$ . . . . . +6V
$-V_A$ . . . . . -6V
Analog Input Voltage
$+V_{IN}$ . . . . . $+V_{SUPPLY}$ +2.0V
$-V_{IN}$ . . . . . $-V_{SUPPLY}$ -2.0V
Either Supply to Ground 16.5V

Operating Conditions

Temperature Range
HI-524-2, -8. . . . . -55^oC to 125^oC
HI-524-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	70	18
CLCC Package	65	16
PDIP Package	90	N/A
PLCC Package	80	N/A

Maximum Junction Temperature . . . . . 175^oC
CERDIP, CLCC Packages . . . . . 175^oC
PLCC, PDIP Packages . . . . . 150^oC
Maximum Storage Temperature
(CERDIP, CLCC) . . . . . -65^oC to 150^oC
(PLCC). . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC
(PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.5V; V_{EN} = +2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	HI-524-2/-8			HI-524-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, t_A	(Note 5)	25	-	150	300	-	150	300	ns
Break-Before-Make Delay, t_{OPEN}	(Note 5)	25	-	20	-	-	20	-	ns
Enable Delay (ON), $R_L = 500\Omega$, $t_{ON\ (EN)}$		25	-	180	300	-	180	-	ns
Enable Delay (OFF), $R_L = 500\Omega$, $t_{OFF\ (EN)}$		25	-	180	250	-	180	-	ns
Settling Time (0.1%)	(Note 5)	25	-	200	-	-	200	-	ns
(0.01%)		25	-	600	-	-	600	-	ns
Crosstalk	(Note 6)	25	-	-65	-	-	-65	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	4	-	-	4	-	pF
Channel Output Capacitance, $C_{D(OFF)}$		25	-	10	-	-	10	-	pF
Digital Input Capacitance, C_A		25	-	5	-	-	5	-	pF
DIGITAL INPUT SPECIFICATIONS									
Input Low Threshold (TTL), V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold (TTL), V_{AH}		Full	2.4	-	-	2.4	-	-	V
Input Leakage Current (High), I_{AH}		Full	-	0.05	1	-	0.05	1	µA
Current (Low), A_L		Full	-	-	25	-	-	25	µA
ANALOG CHANNEL SPECIFICATIONS									
Analog Signal Range, V_{IN}		Full	-10	-	+10	-10	-	+10	V
On Resistance, r_{ON}	(Note 2)	25	-	700	-	-	700	-	Ω
		Full	-	-	1.5	-	-	1.5	KΩ
Off Input Leakage Current, $I_{S\ (OFF)}$	(Note 3)	25	-	0.2	-	-	0.2	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D\ (OFF)}$	(Note 3)	25	-	0.2	-	-	0.2	-	nA
		Full	-	-	50	-	-	50	nA
On Channel Leakage Current, $I_{D\ (ON)}$	(Note 3)	25	-	0.7	-	-	0.7	-	nA
		Full	-	-	50	-	-	50	nA

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.5V; V_{EN} = +2.4V, Unless Otherwise Specified **(Continued)**

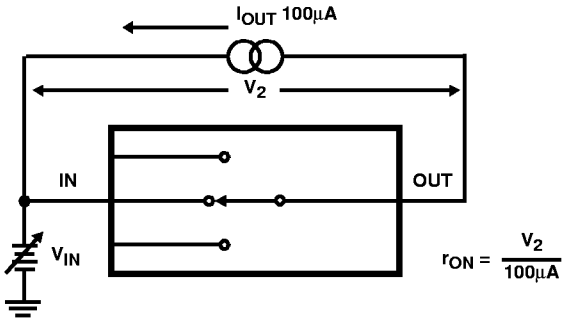
PARAMETER	TEST CONDITIONS	TEMP (^oC)	HI-524-2/-8			HI-524-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
3dB Bandwidth	(Note 4)	25	-	8	-	-	8	-	MHz
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	-	750	-	-	750	mW
Current, I+	(Note 7)	Full	-	-	25	-	-	25	mA
Current, I-	(Note 7)	Full	-	-	25	-	-	25	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{IN} = 0V; I_{OUT} = 100µA (See Test Circuit 1).
3. V_O = ±10V; V_{IN} = ±10V. (See Test Circuits 2, 3, 4.)
4. MUX output is buffered with HA-5033 amplifier.
5. 6V Step, ±3V to ±3V, See Test Circuit 5.
6. V_{IN} = 10MHz, $3V_{P-P}$ on one channel, with any other channel selected. (Worst case is channel 3 selected with input on channel 4.) MUX output is buffered with HA-2541 as shown in Applications section. Terminate all channels with 75Ω.
7. Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

Typical Performance Curves and Test Circuits

T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified



TEST CIRCUIT 1. ON RESISTANCE

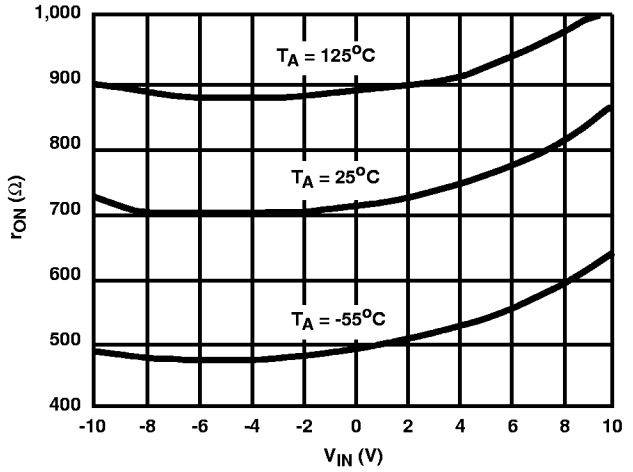


FIGURE 1. ON RESISTANCE vs ANALOG INPUT VOLTAGE

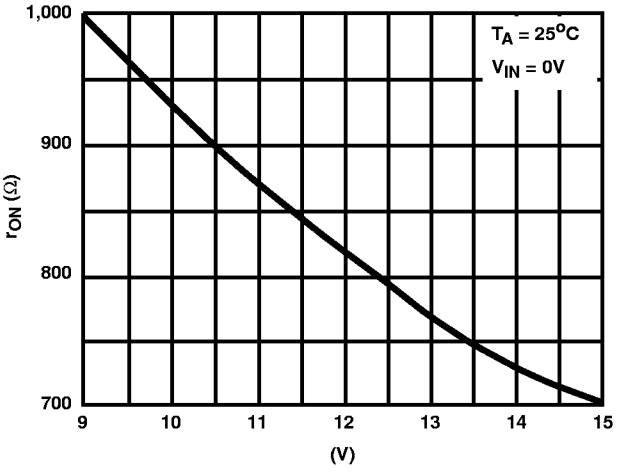


FIGURE 2. ON RESISTANCE vs SUPPLY VOLTAGE

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified **(Continued)**

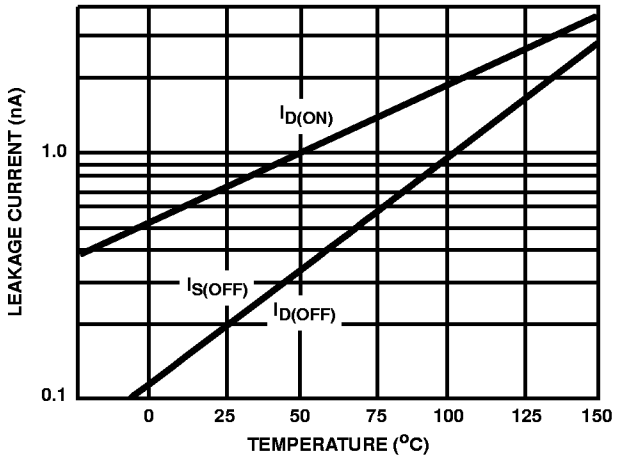
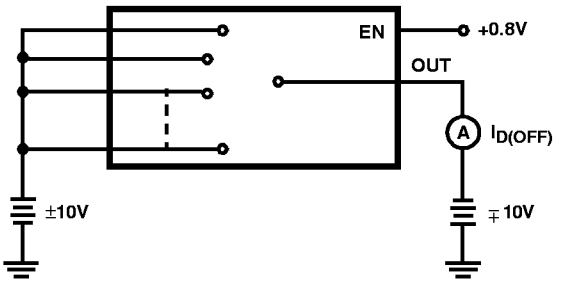
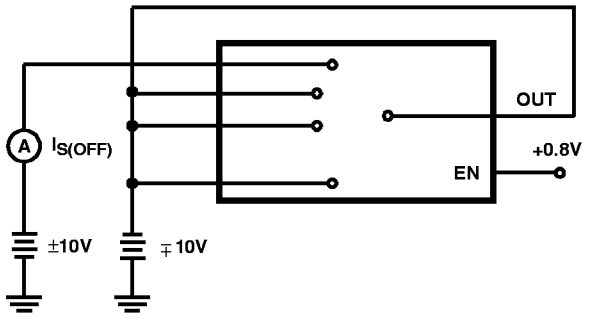


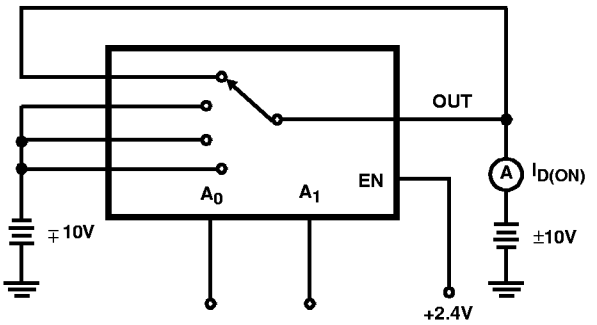
FIGURE 3. LEAKAGE CURRENT vs TEMPERATURE



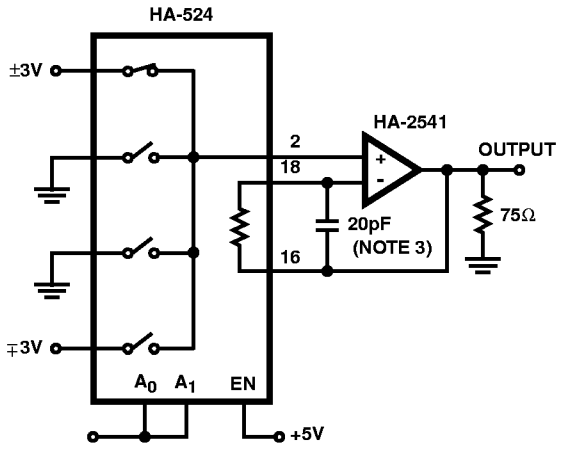
TEST CIRCUIT 2. LEAKAGE CURRENT (NOTE 1)



TEST CIRCUIT 3. LEAKAGE CURRENT (NOTE 1)



TEST CIRCUIT 4. LEAKAGE CURRENT (NOTE 1)



TEST CIRCUIT 5. SETTLING TIME, ACCESS TIME, BREAK-BEFORE-MAKE DELAY (NOTE 2)

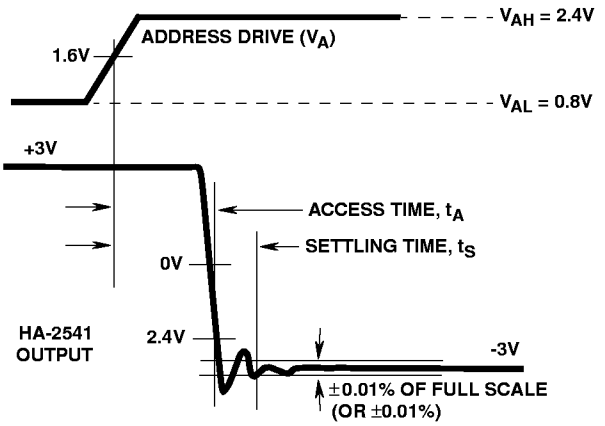


FIGURE 4. POWER SUPPLY CURRENT vs TEMPERATURE

NOTES:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V.)
2. This test requires channel inputs 1 and 4 at the same level.
3. Capacitor value may be selected to optimize AC performance.

Typical Performance Curves and Test Circuits $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified **(Continued)**

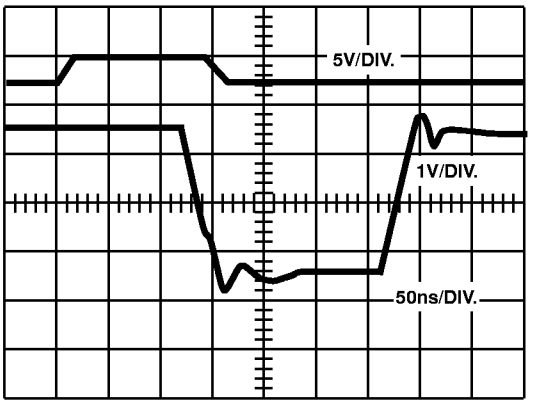


FIGURE 5. ACCESS TIME

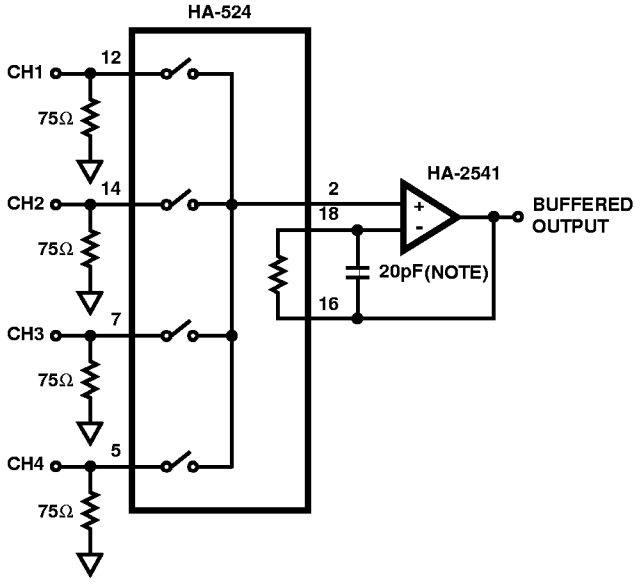
TABLE 1. TRUTH TABLE

A_1	A_0	EN	ON CHANNEL
X	X	L	None
L	L	H	1 (Note)
L	H	H	2
H	L	H	3
H	H	H	4

NOTE: Channel 1 is shown selected in the Functional Diagram.

Typical Applications

Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



NOTE: Capacitor value may be selected to optimize AC performance.

The buffer amplifier should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ±100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel "ON" resistance, to minimize offset voltage due to the buffer's bias currents.

Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These switches open for V_{EN} = Low. This allows two or more HI-524s to operate into one HA-2541, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback, and the amplifier remains stable.

All HI-524 DIP package pins labeled 'SIG GND' (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best crosstalk performance.

Bypass capacitors (0.1µF to 1µF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8 DIP package). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current flow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. The best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

Die Characteristics

DIE DIMENSIONS:

2250µm x 3720µm x 485µm ±25µm

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.58×10^5 A/cm^2

Metallization Mask Layout

HI-524