DAC8871 Evaluation Module

This user's guide describes the characteristics, operation, and the use of the DAC8871 evaluation module (EVM). It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The document includes the physical printed-circuit board layout, schematic diagram, and circuit descriptions.

Related Documentation From Texas Instruments

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Data Sheet	Literature Number
DAC8871	SBAS396
REF102	SBVS022
OPA211	SBOS377
OPA277	SBOS079
OPA4227	SBOS110
INA105	SBOS145

Questions about this or other data converter EVMs?

If you have questions about this or other Texas Instruments data converter evaluation modules, send an e-mail to the Data Converter Application Team at dataconvapps@list.ti.com. Include in the subject heading the product in which you are interested.

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1 EVM Overview

This section gives a general overview of the DAC8871 evaluation module (EVM) and describes some of the factors to be considered when using this module.

1.1 Features

This EVM features the DAC8871 digital-to-analog converter. The DAC8871EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality and performance of the 16-bit, high-resolution, high-voltage output, single-channel, and serial input DAC. This EVM features a high-speed serial interface of up to 50 MHz to communicate with any host microprocessor or DSP-based system.

The DAC8871 is designed to work with bipolar output range or unipolar output range depending on the reference voltage that is applied to the reference input high and low pins ($V_{REF}H$ and $V_{REF}L$) of the device. The voltage reference configuration implemented on this EVM uses the Kelvin connection feature of the DAC8871 device. This connection helps to minimize the internal errors caused by the changing reference current and its associated circuit impedances.

A +10-V precision voltage reference is provided onboard via U3 (REF102) to supply the necessary external reference voltage to set the DAC8871 output range. Though only ±10-V output range is provided on the board, the provision of test points TP1 and TP2 allows users to select their own external reference supply of up to ±18 V maximum.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The DC power supply requirement for this DAC8871EVM (V_{DD}) is selectable between +3.3 V and +5 V via the W9 jumper header. The +3.3 V comes from J3-9, and the +5 V comes from J3-10 terminal, when plugged in via the 5-6K interface board or other interface platform. These power supply voltages are referenced to digital ground through the J3-5 terminal.

The V_{CC} and V_{SS} that range from +19.8 V maximum to -19.8 V minimum connect through the J3-1 and J3-2 terminals, respectively. All the analog power supplies are referenced to analog ground through the J3-6 terminal.

CAUTION

To avoid potential damage to the EVM board, ensure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The DAC8871 requires an external reference source to set the DAC's operating voltage output range. By applying the desired voltage between the range of 0 V to +18 V into the $V_{REF}H$ pin sets the positive range of the DAC8871 output. In like manner, applying the desired voltage between the range of –18 V to ($V_{REF}H$ – 1.25 V) into the $V_{REF}L$ pin sets the negative range of the DAC8871 output. The voltages applied into the $V_{REF}H$ and $V_{REF}L$ pins dictate the mode of operation of the DAC (i.e., either unipolar or bipolar mode).

For optimum performance, the DAC8871 supports a set Kelvin connection to the external reference via $V_{REFH}F$ and $V_{REFH}S$ pins, as well as $V_{REFL}F$ and $V_{REFL}S$ pins. This option for reference configuration minimizes the internal errors caused by the changing reference current and its associated circuit impedances.

A +10-V precision voltage reference is provided for the external reference source of the DAC through REF102, U3. The -10-V reference supply is generated by inverting the +10-V output of the REF102 via the INA105 or an OPA227 and some resistor components. This EVM uses the INA105 as its default component to generate the –10-V reference voltage.

The reference voltages are selectable via jumpers W1 and W3. When shorting pins 1 and 2 of both jumpers, the onboard +10-V reference via REF102 is selected. Shorting pins 2 and 3 of both jumpers selects the reference voltages that are applied via J1 pins 18 and 20, respectively. These voltages normally come from the host platform that is used to interface with the DAC8871EVM.

The test points TP1 and TP2 are also provided to allow the user to connect other external reference sources if the onboard reference circuit is not desired. The external voltage reference should not exceed the applied power supplies V_{CC} and V_{SS} of the DAC under test.

CAUTION

When applying an external voltage reference through TP1 or J1-20 and TP2 or J1-18, ensure that it does not exceed ±18 V. Otherwise, this can permanently damage the DAC8871, U1, device under test.

1.3 EVM Basic Functions

This EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC8871 digital-to-analog converter. Functional evaluation of the installed DAC device can be accomplished with the use of any microprocessor, DSP, or some sort of a signal/waveform generator.

The headers J2 (top side) and P2 (bottom side) are passed through connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8871EVM using a custom-built cable.

An adapter interface board (5-6K adapter interface board) is also available to fit and mate with the TI C5000™ and C6000™ DSP Starter Kit (DSK). This eliminates the need for a user to build a custom cable. In addition, this EVM can connect to and interface with an MSP430-based platform (HPA-MCU) that uses the MSP430FG4618 microprocessor. For more details or information regarding the 5-6K adapter interface board or the HPA-MCU platform, call Texas Instruments or send an e-mail to dataconvapps@list.ti.com.

The DAC output can be monitored through pins 2 and 6 of the J1 header connector.

Figure 1 shows a block diagram of the EVM.

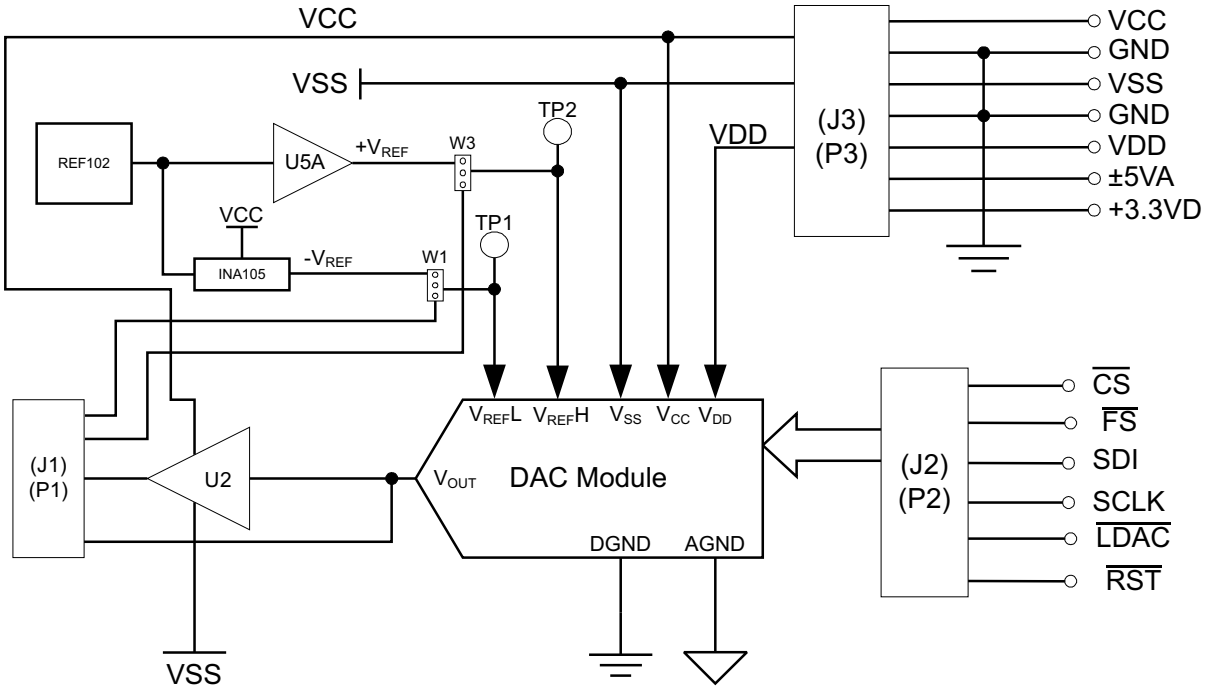

Figure 1. Block Diagram

2 PCB Design and Performance

This section discusses the layout design of the PCB and describes the physical and mechanical characteristics of the EVM, as well as a brief description of the EVM test performance procedure performed. Also included is the list of components used on this evaluation module.

2.1 PCB Layout

The DAC8871EVM is designed to preserve the performance quality of the DAC, the device under test, as specified in the data sheet. The key to a successful design implementation is the careful analysis of the EVM's physical restrictions and the elements that can contribute to the EVM's potential performance degradation. By properly selecting the right components and building the circuit correctly, obvious attributes that can diminish EVM performance can be taken cared of during the schematic design phase. Good circuit design includes adequate bypassing, identifying, and managing the analog and digital signals, along with understanding the components mechanical attributes.

An obscure part of the design process can be the layout. The main concern is primarily with the placement of components and the proper routing of signals. Bypass capacitors should be placed as close as possible to the pins, and analog and digital signals should be properly separated from each other. Because the power and ground plane is important, it should be carefully considered in the layout process. A solid plane is ideal but if this is impractical, a split plane can be used. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections, starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning that the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces, but use the biggest possible trace width that is allowable in the design. These design practices can be seen in Figure 2 through Figure 6.

The DAC8871 EVM board is constructed on a two-layer printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 43,1800 mm (1.7000 inch) × 82,5500 mm (3.2500 inch), and the board thickness is 1,5748 mm (0.062 inch). Figure 2 through Figure 6 show the individual artwork layers.

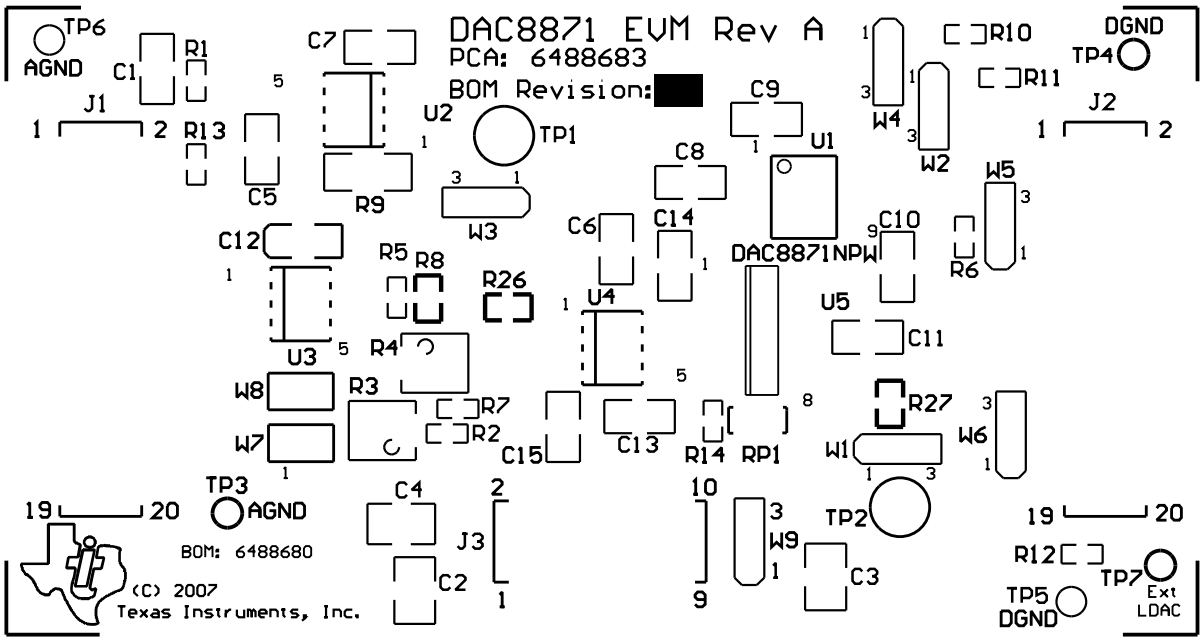

Figure 2. Top Silkscreen

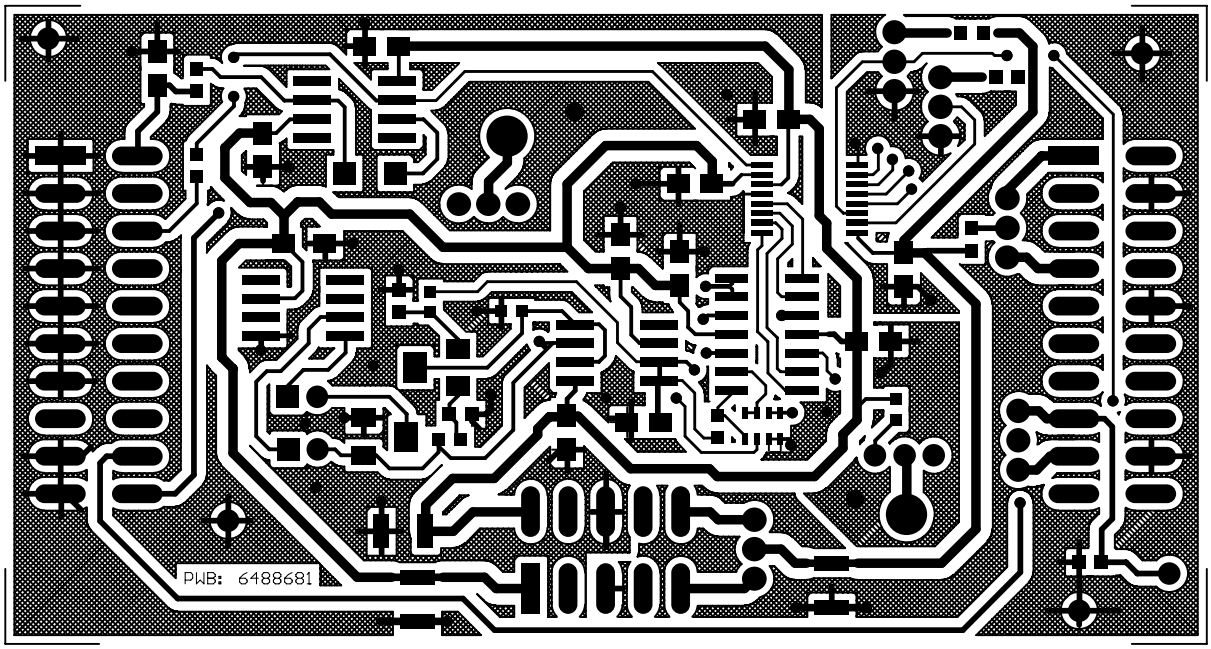

Figure 3. Layer 1, Top Signal Plane

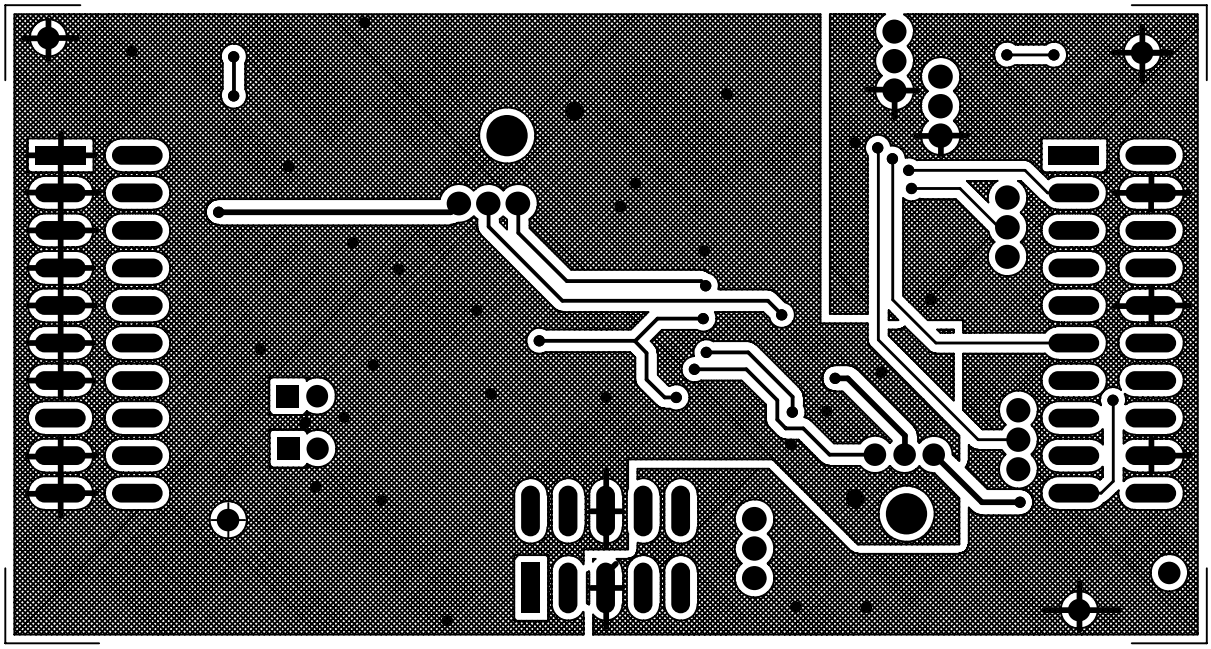

Figure 4. Layer 2, Bottom Signal Plane

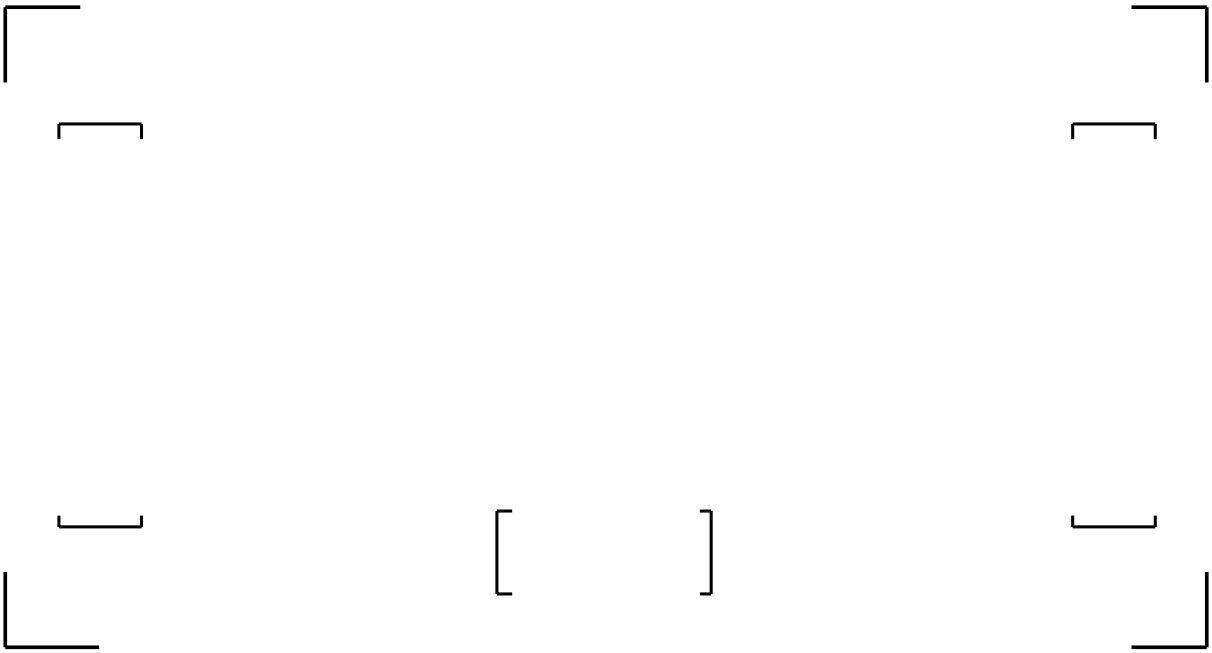

Figure 5. Bottom Silkscreen

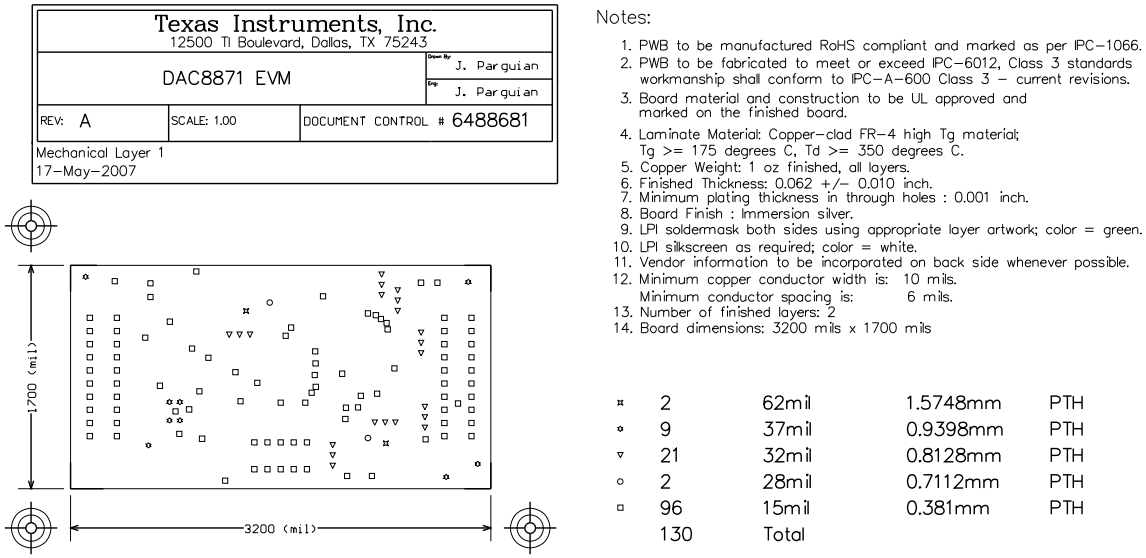

Figure 6. Drill Drawing

2.2 EVM Performance

The EVM performance test is carried out using a high-density DAC bench test board, an Agilent 3458A digital multimeter, and a personal computer running the LabVIEW™ software. The EVM board is tested for all codes of 65535, and the device under test (DUT) is allowed to settle for 1 ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL.

Figure 7 shows the INL and DNL characteristic plots.

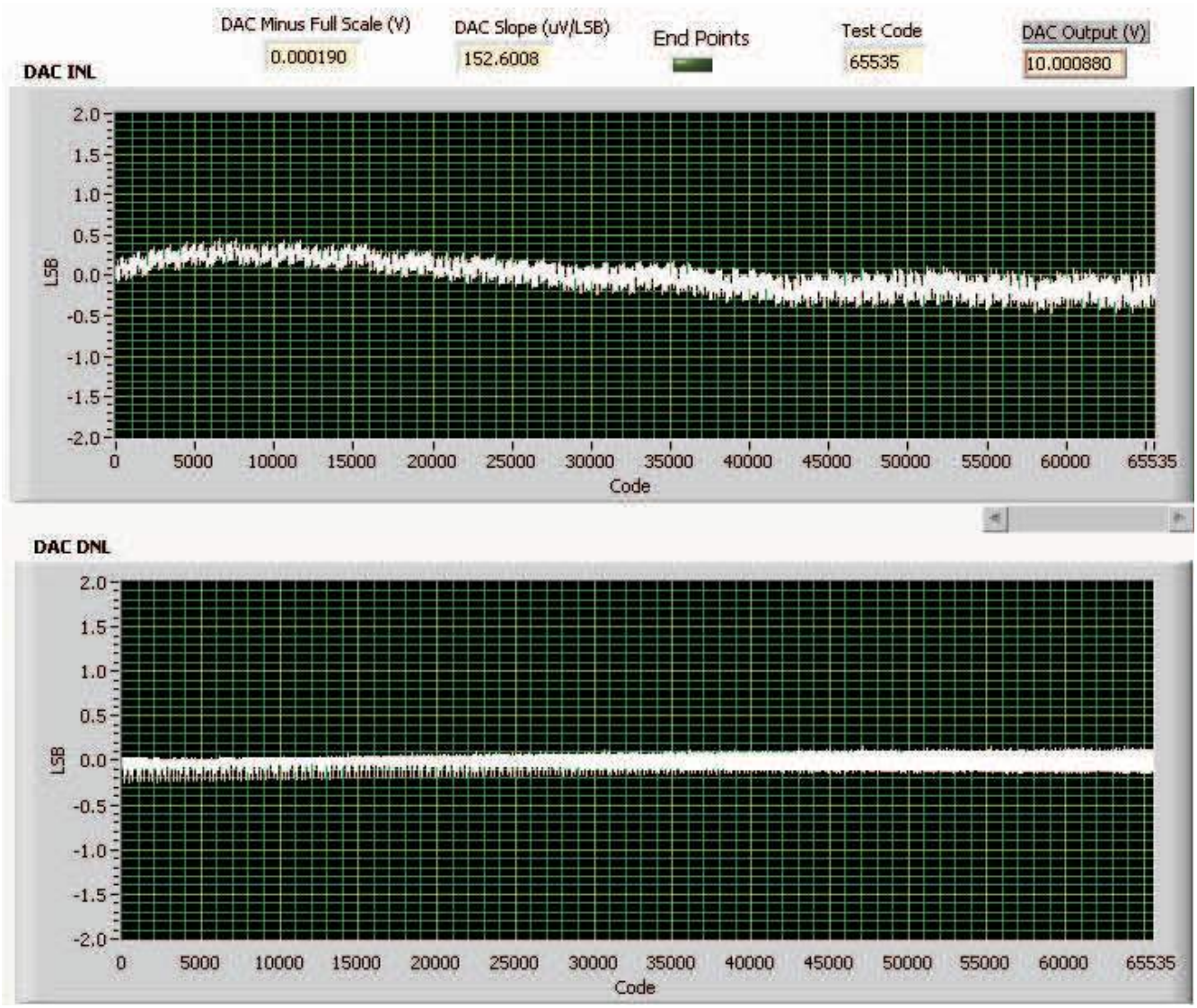

Figure 7. INL and DNL Characteristic Plot

2.3 Bill of Materials

Table 1. Bill of Materials

Qty.	Value	Designators	Description	Vendor	Vendor Part Number
1	N/A	N/A	Printed Wiring Board	Texas Instruments	6488681
0	100pF	C1 (1)	0608, Ceramic, COG, 50V, 5%	TDK	C1608COG1H101J
3	10µF	C2 C3 C4	1210, Ceramic, X7R, 16V	TDK	C3225X7R1C106Z
10	0.1µF	C5–C11 C13–C15 (2)	0805, Ceramic, X7R, 50V, 10%	TDK	C2012X7R1H104K
1	1µF	C12	1206, Ceramic, X7R, 16V, 10%	TDK	C3216X7R1C105K
2	10 × 2 × 0.1 SMT	J1 J2 (Top Side)	10 Pin, Dual Row, TH Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P

(1) Do NOT install the following: C1, R2, R3, R4, R5, R7, R8, R14 and RP1.
(2) Default parts for the negative reference circuit: C6, C13, C15, R26, R27 and U4.

Table 1. Bill of Materials (continued)

Qty.	Value	Designators	Description	Vendor	Vendor Part Number
1	5 × 2 × 0.1 SMT	J3 (Top Side)	5 Pin, Dual Row, TH Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
2	10 × 2 × 0.1 SMT	P1 P2 (3)(Bottom Side)	10 Pin, Dual Row, TH Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
1	5 × 2 × 0.1 SMT	P3(3)(Bottom Side)	5 Pin, Dual Row, TH Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
1	100Ω	R1	0603,1/4W	Yageo America	9C06031A1000JLHFT
3	0Ω	R13 R14 R26(1) (2)	0603	Yageo America	9C06031A0R00JLHFT
0	TBD	R2–R5 R7 R8(1)	Do Not Populate	TBD	TBD
1	1kΩ	R27(2)	0603,	Yageo America	9C06031A1001JLHFT
1	6.2kΩ	R9	1206		
3	10kΩ	R6 R10 R11	0603	Yageo America	9C06031A1002JLHFT
1	25kΩ	RP1(1)	Chip Resistor Array	CTS	742C083223FP
2	1 × 1 × 0.061D TH	TP1 TP2	Test Point Turret	Mill-Max	2348-2-00-01-00-00-07-0
4	0.040 in. Mounting Hole	TP3–TP6	Through Hole Test Point Loop, Black	Keystone	5000
1	16-Bit R2R DAC	U1	16-Bit, Unbuffered Voltage Output DAC	Texas Instruments	DAC8871
0	±2V to ±18V Supply	U2	High Precision Op-Amp	Texas Instruments	OPA277UA
1	+10V Output	U3	Precision Voltage Reference	Texas Instruments	REF102CU
1	±5V to ±18V Supply	U4(2)	Precision Unity Gain Differential Amplifier	Texas Instruments	INA105KU
1	±2.5V to ±18V Supply	U5	High Precision, Low Noise, Quad Op-Amp	Texas Instruments	OPA4227UA
7	2 × 1 × 0.1 TH	W1–W6 W9	3 Pin Mini Header	Samtec	TMMH-103-01-T-T
2	3 × 1 × 0.1 TH	W7 W8	2 Pin Mini Header	Samtec	TMMH-102-01-T-T
5	Do Not Populate	C6 R5 R7 R16 R25	Do not install these components(1) (2)	TBD	TBD
1	2mm Shunt	N/A	Shorting Block for W2	Samtec	2SN-BK-G
6	0.100 Shorting Blocks	N/A	Shorting Blocks	Samtec	SNT-100-BK-G-H

(3) P1, P2 and P3 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC Board opposite the J designated counterpart. Example, J2 is installed on the topside while P2 is installed in the bottom side opposite of J2.

3 EVM Operation

This section covers the EVM operation in detail to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

See the DAC8871 data sheet (SBAS396) for information about its serial interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

3.1 Factory Default Setting

The EVM board is set to its default configuration from the factory as described in the Table 2 to operate in bipolar ±10-V mode of operation. Figure 8 shows the default jumper configuration as described in the table for the DAC8871.

Table 2. Factory Default Jumper Setting

Reference	Jumper Position	Function
W1	1-2	The onboard reference of –10 V is routed to $V_{REF}L$ of the DAC8871.
W2	1-2	RSTSEL is pulled high to V_{DD} and sets the default output pf the DAC8871 on power up to midscale (0x8000).
W3	1-2	The onboard reference of +10 V is routed to $V_{REF}H$ of the DAC8871.
W4	1-2	$\overline{RST}$ is pulled high to V_{DD}.
W5	1-2	$\overline{FS}$ signal from J2-7 is used to control the $\overline{CS}$ pin of the DAC8871 for DAC access and frame synchronization.
W6	1-2	GPIO signal from J2-17 is used to control the $\overline{LDAC}$ pin of the DAC8871 to allow the DAC output latch to be updated.
W7	CLOSE	Allows the onboard REF102 output of +10 V to propagate through for the DAC8871's voltage reference high and low source ($V_{REF}H$, $V_{REF}L$).
W8	OPEN	Not used.
W9	1-2	The digital logic interface of the DAC8871 is powered with +3.3 VD.

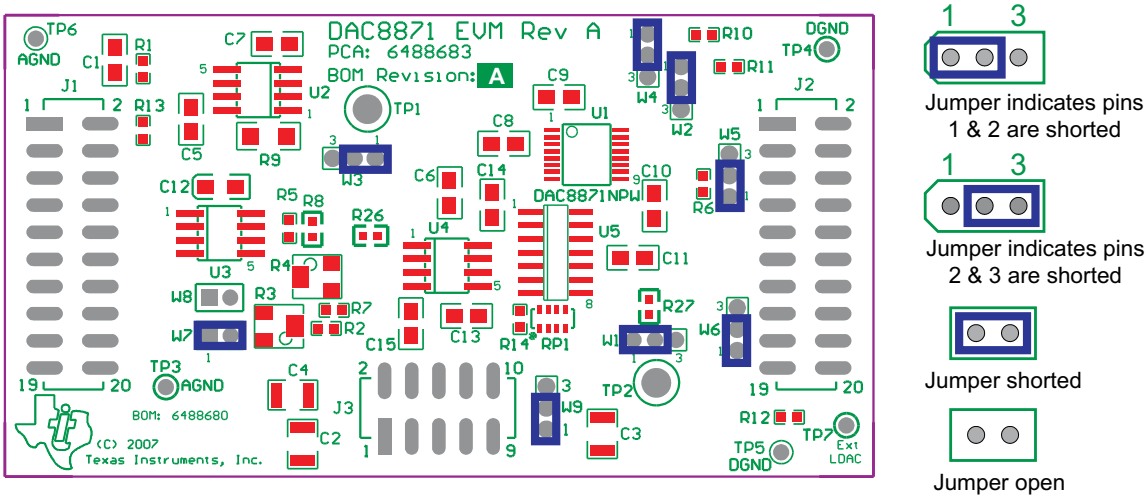

Figure 8. DAC8871 EVM Default Jumper Configuration

3.2 Host Processor Interface

The host processor basically drives the DAC; therefore, the DAC's proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform that the user selects. The EVM allows interface to the host processor through the J2 header connector for the serial control signals and the serial data input.

An interface adapter board is also available for a specific TI DSP starter kit as well as an MSP430-based microprocessor as previously mentioned in this manual. Using the interface board eliminates the task of building customize cables and allows easy configuration of a simple evaluation system.

The DAC8871 interfaces with any host processor capable of handling SPI™ protocols or the TI DSP. For more information regarding the DAC8871 data interface, see the DAC8871 data sheet (SBAS396).

3.3 Digital Control Interface

The DAC8871 supports the standard high-speed SPI serial interface to communicate with microprocessors or DSP devices. The EVM incorporates a pass-through connector to accommodate the digital control interface to the DAC8871 device via J2 (top side) and P2 (bottom side) header/socket connectors. The signals on this pass-through connector are shown in Table 3.

Table 3. Digital Control Interface Signal Mapping for J2/P2 Header/Socket Connectors

Pin Number	Signal	Function
J2.1/P2.1	$\overline{CS}$	Primary synchronization and device enable input for the DAC8871. Host microcontroller's STE signal for SPI interface.
J2.3/P2.3	SCLK	Serial interface clock.
J2.5/P2.5	Unused	
J2.7/P2.7	$\overline{FS}$	Secondary synchronization and device enable input for the DAC8871. Host microcontroller's STE signal for SPI interface or $\overline{FS}$ signal from DSP host system.
J2.9/P2/9	Unused	
J2.11/P2.11	SDI	Serial data input.
J2.13/P2.13	Unused	
J2.15/P2.15	GPIO1/$\overline{INT}$	GPIO signal to control $\overline{LDAC}$ for DAC output latch update.
J2.17/P2.17	GPIO2/TOUT	Alternate GPIO signal to control $\overline{LDAC}$ for DAC output latch update.
J2.19/P2.19	$\overline{RST}$	GPIO signal to control $\overline{RST}$ for DAC reset function.

3.3.1 $\overline{CS}$ or $\overline{FS}$ Signal

The $\overline{CS}$ and $\overline{FS}$ signals of the EVM are interchangeable, and therefore the signal to be used depends on the host controller that is selected to communicate with the DAC8871EVM. Either signal can be chosen to drive the DAC8871 Chip Select ($\overline{CS}$) pin. The basic function of the $\overline{CS}$ and $\overline{FS}$ signal is to drive the $\overline{CS}$ pin of the DAC8871 to enable the device communication port and to synchronize the data going into the device immediately following its high-to-low transition. This signal must be held low while the host processor is accessing the DAC. The low-to-high transition of this signal transfers the content of the serial shift register to the DAC input register.

3.3.2 SCLK Signal

The SCLK signal is the clock necessary to load the serial data input into the DAC's serial shift register. The serial clock rate can operate at speeds up to 50 MHz. The 16-bit data is shifted out of the bus master synchronously on the falling edge of SCLK and latched on the rising edge of SCLK into the DAC's serial shift register. The most-significant bit (MSB) is the first bit that is sent out to the DAC. After 16-bits are transferred or 16 SCLK cycles are generated, the bus master must take the $\overline{CS}$ signal high immediately. If the $\overline{CS}$ signal is held low and more than 16 SCLK cycles are applied, the last SCLK cycle is considered the location of the least-significant bit (LSB) of the 16-bit word that is loaded into the DAC's serial shift register. Hence, the user must know the data word alignment with respect to SCLK or the data input will be corrupted. If this happens, simply reload the DAC latch with the new 16-bit word.

3.3.3 SDI Signal

The SDI signal is the serial data input that is loaded into the DAC's serial shift register with respect to SCLK.

3.3.4 $\overline{LDAC}$ Signal

The $\overline{LDAC}$ signal is the control input signal necessary to load the DAC register with the content of the input register. This signal is active low and can be triggered synchronously or asynchronously.

3.3.5 $\overline{\text{RST}}$ Signal

The $\overline{\text{RST}}$ signal is the control input necessary to reset the device to a known state that is determined by the state of the RSTSEL pin when the $\overline{\text{RST}}$ pin is asserted. If RSTSEL is tied to DGND, the DAC latch is cleared (0 V) and V_{OUT} is minimum scale (i.e., $V_{REF}L$). If RSTSEL is tied to V_{DD}, the DAC latch is set to midscale and V_{OUT} is equal to ($V_{REF}H$ – $V_{REF}L$)/2. This pin is active low.

3.4 Analog Output

The EVM includes an external operational amplifier, U2, as the output buffer circuit for the DAC. The buffered output can be monitored through J1 pin 2, whereas the unbuffered output of the DAC can be monitored through J1 pin 6 if R13 is populated.

A low-pass filter circuit using R1 and C1 is also included for the DAC output, if desired. The components are not populated by default when it ships out of the factory; therefore, the user must provide the desired components. The resistor R1 is shunted using a jumper resistor.

3.5 Jumper Setting

Table 4 shows the function of each specific jumper setting of the EVM.

Table 4. Jumper Setting Function

Reference	Jumper Setting	Function
W1		Routes the onboard negative voltage reference, $V_{REF}L$ for the DAC.
		Disconnect onboard or external negative voltage reference, $V_{REF}L$ for the DAC via U4 or U5B or J1 pin 18. Allows user reference voltage to connect via TP2.
		Routes the external negative voltage reference, $V_{REF}L$ for the DAC via J1 pin 18.
W2		Tie RSTSEL to V_{DD}. DAC resets to midscale.
		Tie RSTSEL to DGND. DAC resets to minimum scale.
W3		Routes the onboard positive voltage reference, $V_{REF}H$ for the DAC.
		Disconnect onboard or external positive voltage reference, $V_{REF}H$ for the DAC via U5A or J1 pin 20. Allows user reference voltage to connect via TP1.
		Routes the external positive voltage reference, $V_{REF}H$ for the DAC via J1 pin 20.
W4		Tie $\overline{\text{RST}}$ to V_{DD}. DAC reset pin is pulled high.
		Tie $\overline{\text{RST}}$ to DGND. DAC is in permanent reset mode.
W5		$\overline{\text{FS}}$ signal from J2-7 is routed to drive the $\overline{\text{CS}}$ signal of the DAC8871.
		$\overline{\text{CS}}$ signal from J2-1 is routed to drive the $\overline{\text{CS}}$ signal of the DAC8871.

Table 4. Jumper Setting Function (continued)

Reference	Jumper Setting	Function
W6		GPIO2/TOUT signal from J2-15 is routed to drive the $\overline{\text{LDAC}}$ signal of the DAC8871.
		GPIO1/$\overline{\text{INT}}$ signal from J2-17 is routed to drive the $\overline{\text{LDAC}}$ signal of the DAC8871.
W7		Allows the onboard REF102 output of +10 V to propagate through for the DAC8871's voltage reference high and low source ($V_{REF}H$, $V_{REF}L$).
		Disconnects the onboard REF102 output of +10 V used for the DAC8871's voltage reference high and low source ($V_{REF}H$, $V_{REF}L$).
W8		Connect this jumper if trimming function is desired for U3. Trim potentiometer, R3, is not populated by default; so, this jumper is not used.
		This is the default position. Trim potentiometer, R3, is not populated by default; so, this jumper is not used.
W9		Routes +3.3 VD for V_{DD} to power digital voltage pin of DAC8871.
		Routes +5 VD for V_{DD} to power the digital voltage pin of DAC8871.
Legend:		Indicates the corresponding pins that are shorted or closed.

3.6 Schematic

The DAC8871EVM evaluation module schematic appears on the following page.

Revision History		
REV	ECN Number	Approved
2	Prototype	JLP
A	Production Release	JLP

DAC8871EVM BOM = 6488680
DAC8871EVM PWB = 6488681
DAC8871EVM DDB (BLOCK) = 6488682
DAC8871EVM PCA = 6488683
DAC8871EVM KIT (BLOCK) = 6488684
DAC8871EVM SFT = 6488685

NOTES:
(1) U5B and RP1 should only be utilize as replacement circuit When INA105 is not available. See BOM for assembly instructions.

J1 TP3 EXT_REF_INP EXT_REF_INM R13 0 R1 100 C1 DNP R9 6.2K U2 OPA211 SO-8 C7 0.1µF C5 0.1µF VSS VCC Other Op-Amps Recommended: OPA277

VDD R10 10K R11 10K W4 W2 C9 0.1µF R6 10K U1 DAC8871SPW Vout C8 VSS AGND RSTSEL RST DGND SCLK CS SDI LDAC VCC VrefHF VrefHS VrefLF VrefLS VDD C10 0.1µF W5 W6 TP7 R12 50 J2 TP4 CS SCLK FS SDI GPIO1/INT GPIO2/TOUT RST

U3 +10V C14 0.1µF U5A OPA4227UA +REF C11 0.1µF W3 C12 1uF U3 REF102 N/C VIN TEMP GND TRIM OUT W7 W8 R3 DNP R2 DNP R7 DNP R5 DNP R8 DNP R4 DNP

RP1 25K U5B OPA4227UA # See Note (1) In this schematic R14 0

U4 INA105 -IN +IN REF V- NC V+ Output Sense C6 0.1µF C13 0.1µF -REF

TP1 U5D OPA4227UA TP2 W1 U5C OPA4227UA R27 3K R26 0 ohm C15 0.1µF

+3.3VD VD2 +5VA VCC VSS -5VA VD1 +5VD J3 TP5 TP6 C2 10µF C4 10µF W9 VDD C3 10µF

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: DAC8871 EVM			
Engineer: Jojo Parguian	DOCUMENTCONTROL # 6488682		REV: A
Drawn By: Jojo Parguian			
FILE: DAC8871_Rev_A.Sch	DATE: 24-Sep-2007	SIZE:	SHEET: 1 OF: 1

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -18 V to 18 V and the output voltage range of -18 V to 18 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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