PI74FCT3244

Fast CMOS 3.3V 8-Bit Buffer/Line Driver

Features

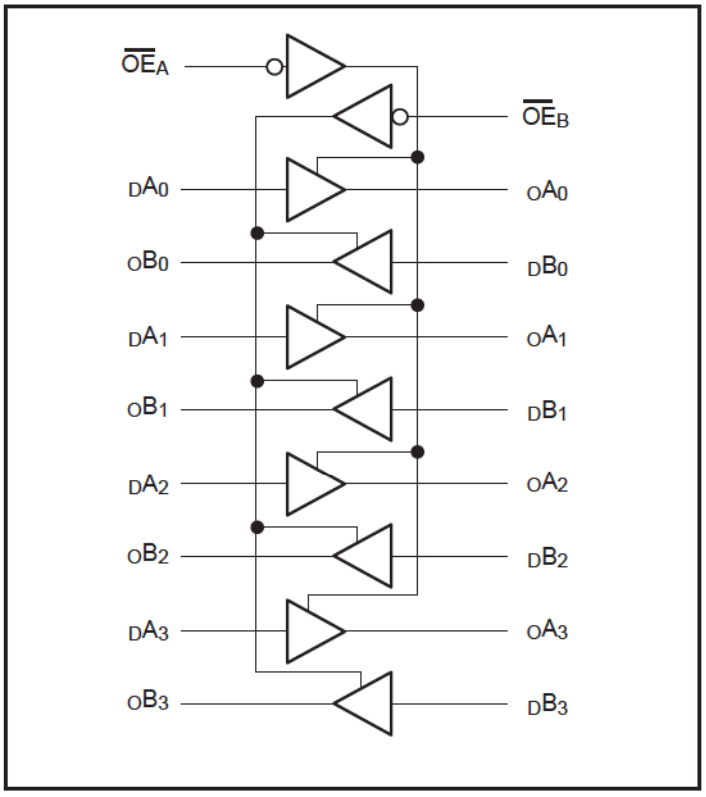
- Advanced Low Power CMOS operation
- Compatible with LVC class of products
- Compatible with industry standard octal pinouts
- Excellent output drive capability:
  Balanced Drives (24mA sink and source)
- Can serve as a 5V to 3V translator
- Inputs can be driven by 3.3 V or 5V devices
- Low ground bounce outputs
- Hysteresis on all inputs
- Industrial operating temperature range:
  –40°C to +85°C
- Packaging (Pb-free & Green available):
  – 20-pin 173-mil wide plastic TSSOP (L)
  – 20-pin 150-mil wide plastic QSOP (Q)
  – 20-pin 300-mil wide plastic SOIC (S)

Description

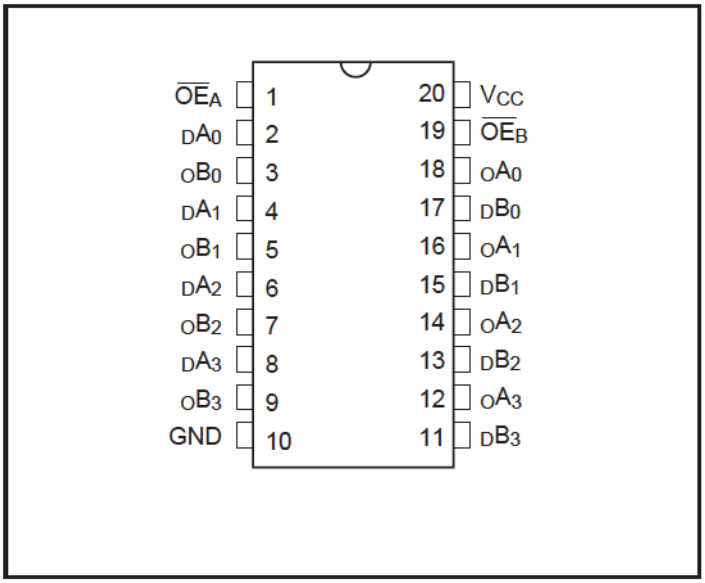
The PI74FCT3244 is an 8-bit buffer/line driver designed for driving high capacitive memory loads. With its balanced-drive characteristics, this high-speed, low power device provides lower ground bounce, transmission line matching, fewer line reflections and lower EMI and RFI. This makes it ideal for driving on-board buses and transmission lines.

The PI74FCT3244 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator.

Block Diagram



Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V_{CC} Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table(1)

Inputs			Outputs
$\overline{OE}_A$	$\overline{OE}_B$	D_{XX}	O_{XX}
L	L	L	L
L	L	H	H
H	H	X	Z

Note:
1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Pin Description

Pin Name	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
D_{XX}	Inputs
O_{XX}	Outputs
GND	Ground
V_{CC}	Power

DC Electrical Characteristics (T_A = –40°C to +85°C, Vcc = 2.7V to 3.6V)

Parameters	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
V_{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2		5.5	V
	Input HIGH Voltage (I/O pins)			2.0		5.5	
V_{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5		0.8	
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_{IN} = 5.5V			±1	µA
	Input HIGH Current (I/O pins)	V_{CC} = Max.	V_{IN} = Vcc			±1	
I_{IL}	Input LOW Current (Input pins)	V_{CC} = Max.	V_{IN} = GND			±1	
	Input LOW Current (I/O pins)	V_{CC} = Max.	V_{IN} = GND			±1	
I_{OZH}	High Impedance Output Current (3-State Output pins)	V_{CC} = Max.	V_{OUT} = 5.5V			±1	
I_{OZL}		V_{CC} = Max.	V_{OUT} = GND			±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA			–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –0.1mA	V_{CC}-0.2			V
			I_{OH} = –3mA	2.4	3.0		
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA	2.4[5]	3.0		
			I_{OH} = –24mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA			0.2	
			I_{OL} = 16mA		0.2	0.4	
			I_{OL} = 24mA		0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max.[3], V_{OUT} = GND		–60	–85	–240	mA
I_{OFF}	Power Down Disable	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 4.5V				±100	µA
V_H	Input Hysteresis				150		mV

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = Vcc – 0.6V at rated current.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[1]	Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	

Notes:
1. Determined by device characterization.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	10	mA
ΔI_{CC}	Quiescent Power Supply Current, TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]			500	µA
I_{CCD}	Dynamic Power Supply[4]	V_{CC} = Max., Outputs Open $\overline{OE}x$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		95	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_I = 10 MHz 50% Duty Cycle $\overline{OE}x$ = GND One Bit Toggling	V_{IN} = V_{CC} – 0.6V V_{IN} = GND		0.97	2.3	mA
		V_{CC} = Max., Outputs Open f_I = 2.5 MHz 50% Duty Cycle $\overline{OE}x$ = GND 8 Bits Toggling	V_{IN} = V_{CC} – 0.6V V_{IN} = GND		1.9	4.7[5]	

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 3.3V, T_A=+25°C.
3. Per TTL driven input; all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIECSENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_I = Number of Inputs at f_i

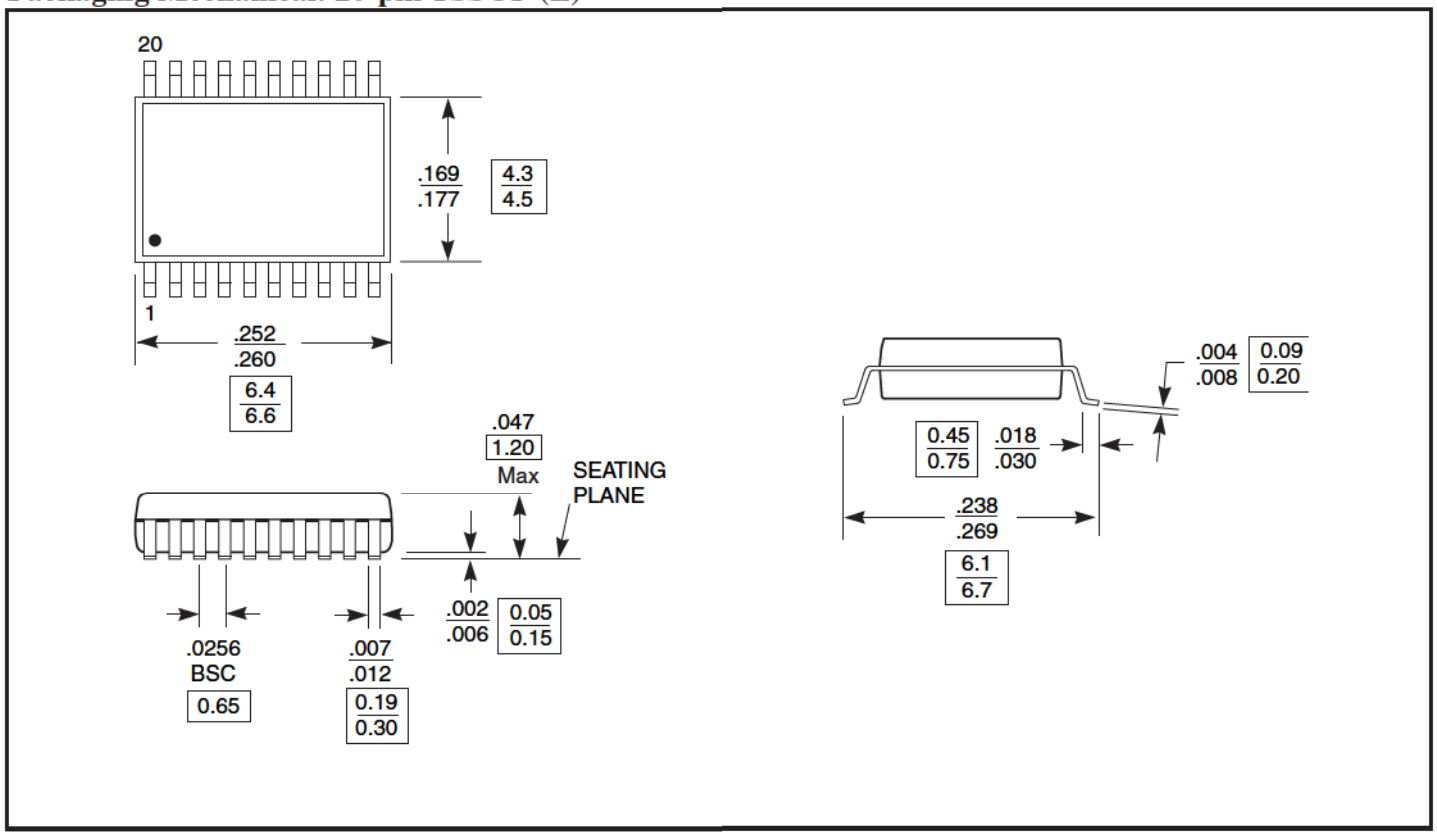
Switching Characteristics over Operating Range[1]

Parameters	Description	Conditions	FCT3244 Com. Min.[2]	FCT3244 Com. Max.	Units
t_{PHL} t_{PHL}	Propagation Delay, D_{XX} to O_{XX}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	4.1	ns
t_{PZH} t_{PZL}	Output Enable Time, $\overline{OE}_X$ to O_{XX}		1.5	5.8	
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{OE}_X$ to O_{XX}		1.5	5.2	
$t_{SK(o)}$	Output Skew[3]			0.5	

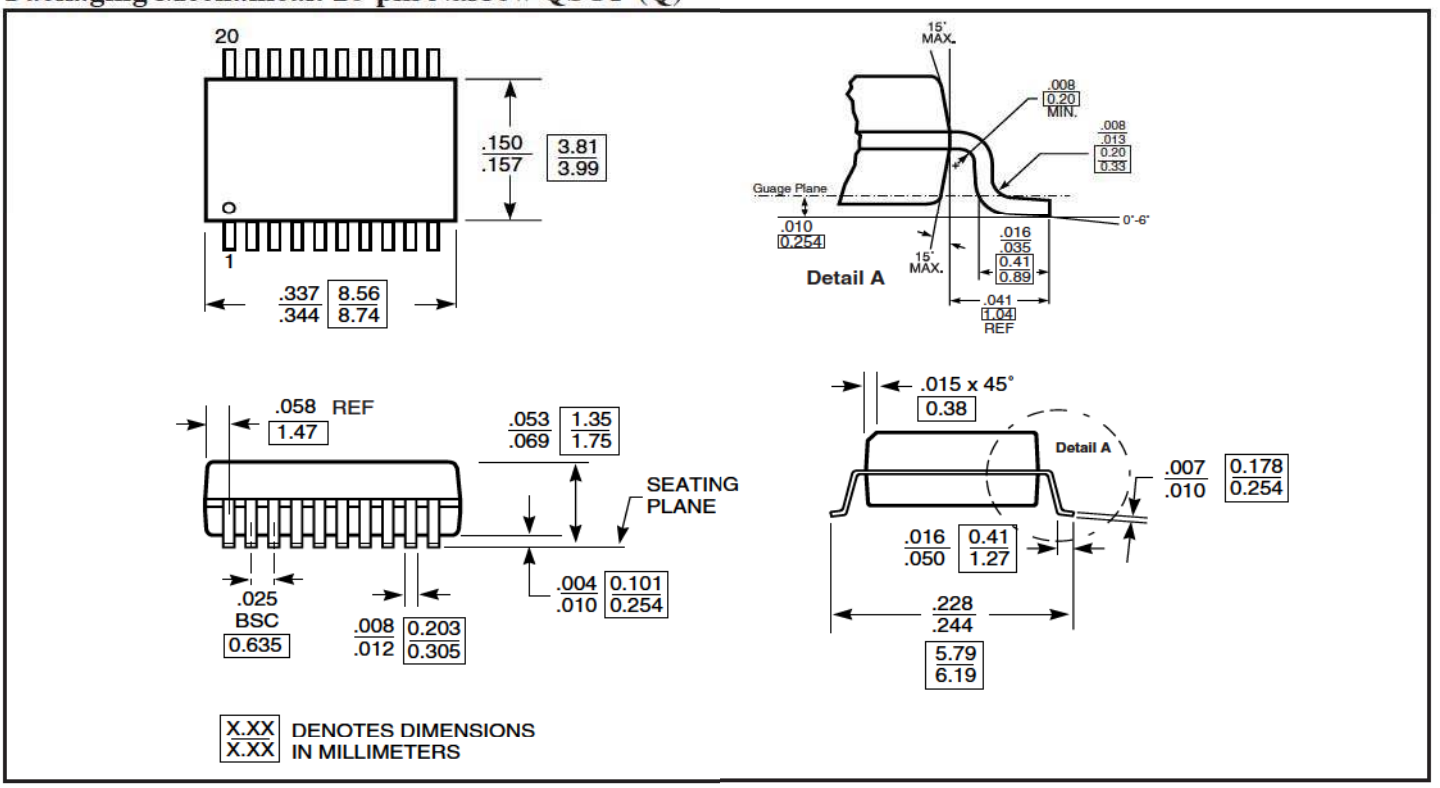
Notes:

1. Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, normal range. At $V_{CC} = 2.7V$, all Propagation Delay and Enable/Disable times are degraded by 20%.
2. Minimum limits are guaranteed by design and characterization.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design and characterization.

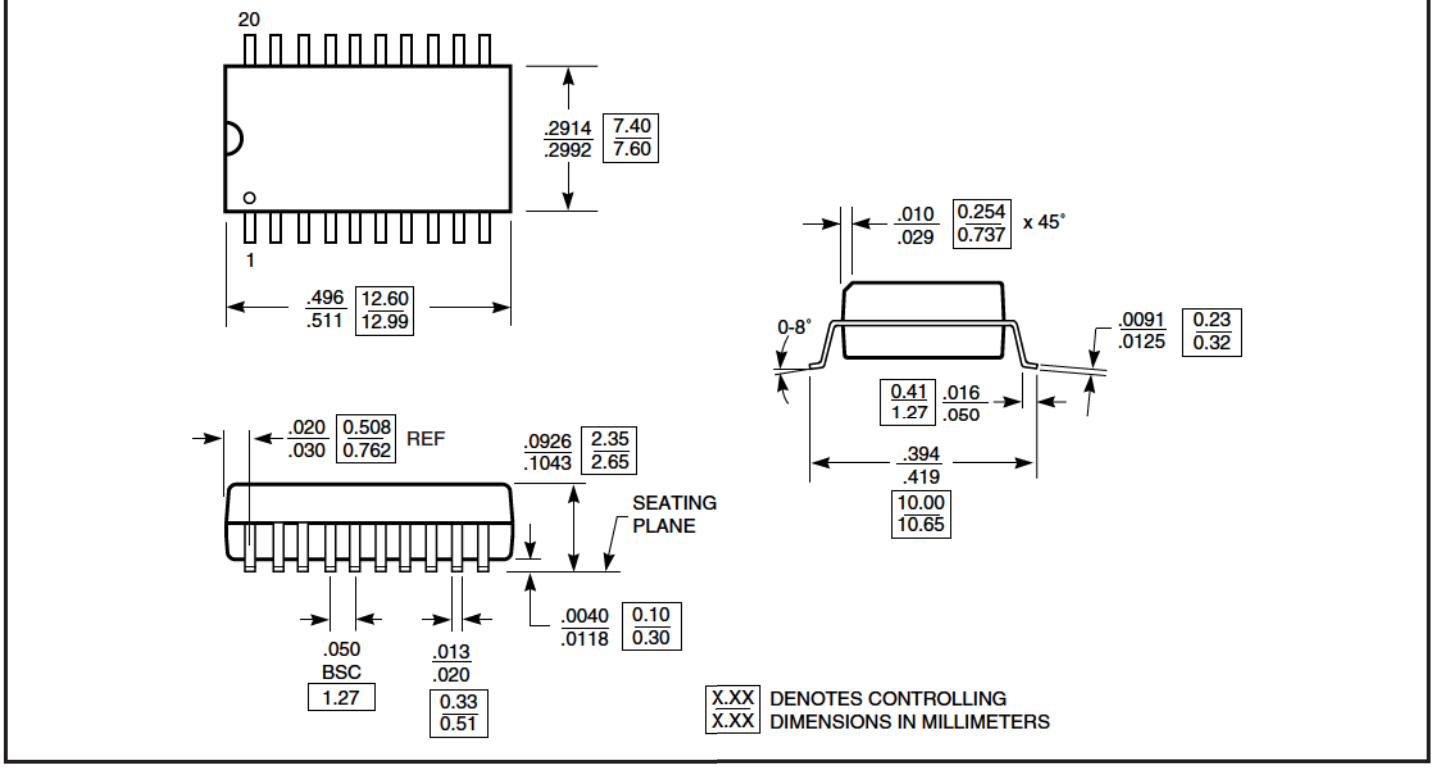
Packaging Mechanical: 20-pin TSSOP (L)



Packaging Mechanical: 20-pin Narrow QSOP (Q)



Packaging Mechanical: 20-pin SOIC (S)



Ordering Information

Ordering Code	Package Code	Package Description
PI74FCT3244L	L	20-pin 173-mil wide plastic TSSOP
PI74FCT3244LE	L	Pb-free & Green, 20-pin 173-mil wide plastic TSSOP
PI74FCT3244Q	Q	20-pin 150-mil narrow plastic QSOP
PI74FCT3244QE	Q	Pb-free & Green, 20-pin 150-mil narrow plastic QSOP
PI74FCT3244S	S	20-pin 300-mil wide plastic SSOP
PI74FCT3244SE	S	Pb-free & Green, 20-pin 300-mil wide plastic SSOP

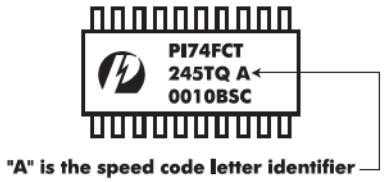
Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- Adding an X suffix = Tape/Reel

Part Marking Information

Pericom's standard product mark follows our standard part number ordering information, except for those products with a speed letter code. For marking purposes, the speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered.

Although all products are marked immediately after assembly to assure material traceability, Pericom does not usually mark the speed code at that time. After electrical test screening and speed binning have been completed, we then perform an "add mark" operation which places the speed code letter at the end of the complete part number.

Please refer to the example shown below:
- Part Number as ordered: PI74FCT245ATQ
- Example of Part Number as marked:



Notes:
1) 8-pin DIP, 8-pin SOIC, 8-pin TSSOP, 14-pin SOIC, 16-pin QSOP, SC70, MSOP, and SOT23 packages are not marked with the Pericom logo due to space limitations on the package.