P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[e]	Q_g (Typ.)
- 20	0.084 at V_{GS} = - 4.5 V	- 9.8	9.5 nC
	0.100 at V_{GS} = - 2.5 V	- 9.0	
	0.120 at V_{GS} = - 1.8 V	- 5.0	
	0.155 at V_{GS} = - 1.5 V	- 2.0	
	0.495 at V_{GS} = - 1.2 V	- 0.5	

FEATURES

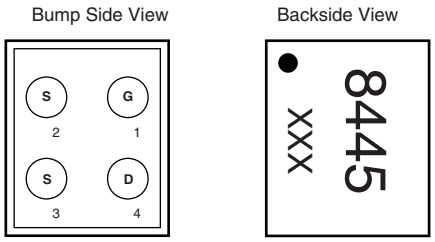
- TrenchFET® Power MOSFET
- Ultra Small 1.2 mm Length x 1 mm Width
- Ultra Thin 0.59 mm Height

Pb-free
RoHS COMPLIANT

APPLICATIONS

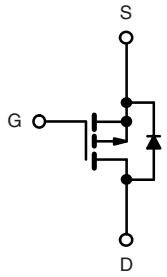
- Portable Devices
  - Battery Management
  - Low Threshold Load Switch
  - Battery Protection

MICRO FOOT



Device Marking: 8445
xxx = Date/Lot Traceability Code

Ordering Information: Si8445DB-T2-E1 (Lead (Pb)-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 20	V
Gate-Source Voltage		V_{GS}	± 5	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 9.8	A
	T_C = 70 °C		- 7.9	
	T_A = 25 °C		- 3.9[a, b]	
	T_A = 70 °C		- 3.1[a, b]	
Pulsed Drain Current		I_{DM}	- 10	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 9.5	
	T_A = 25 °C		- 1.5[a, b]	
Maximum Power Dissipation	T_C = 25 °C	P_D	11.4	W
	T_C = 70 °C		7.3	
	T_A = 25 °C		1.8[a, b]	
	T_A = 70 °C		1.1[a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Package Reflow Conditions[c]	IR/Convection		260	

Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. t = 5 s.
c. Refer to IPC/JEDEC (J-STD-020C), no manual or hand soldering.
d. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
e. Based on T_C = 25 °C.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, b]		R_{thJA}	55	70	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	8.5	11	

Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. Maximum under Steady State conditions is 100 °C/W.
c. Case is defined as top surface of the package.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

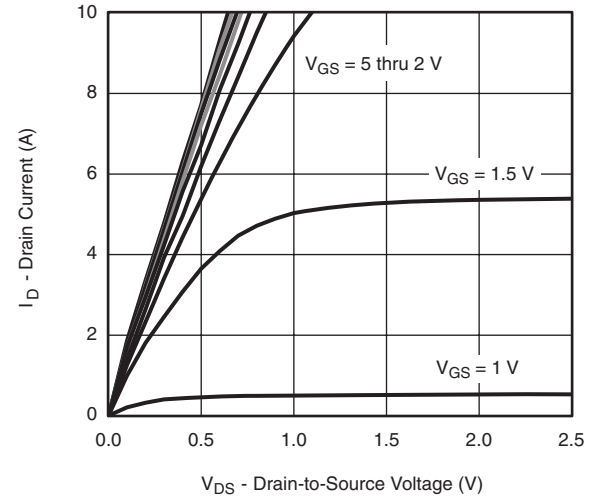
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 19		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.35		- 0.85	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 5 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 70 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 5			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 1 A		0.070	0.084	Ω
		V_{GS} = - 2.5 V, I_D = - 1 A		0.082	0.100	
		V_{GS} = - 1.8 V, I_D = - 1 A		0.097	0.120	
		V_{GS} = - 1.5 V, I_D = - 0.7 A		0.115	0.155	
		V_{GS} = - 1.2 V, I_D = - 0.2 A		0.165	0.495	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 1 A		6.5		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		700		pF
Output Capacitance	C_{oss}			130		
Reverse Transfer Capacitance	C_{rss}			80		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 5 V, I_D = - 1 A		10.5	16	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = 1 A		9.5	15	
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			2.2		
Gate Resistance	R_g	V_{GS} = - 0.1 V, f = 1 MHz		5.5		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω $I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		11	20	ns
Rise Time	t_r			25	40	
Turn-Off Delay Time	$t_{d(off)}$			37	55	
Fall Time	t_f			10	15	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 9.5	A
Pulse Diode Forward Current	I_{SM}				- 10	
Body Diode Voltage	V_{SD}	I_S = - 1 A, V_{GS} = 0 V		- 0.7	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 1 A, dI/dt = 100 A/µs, T_J = 25 °C		25	50	ns
Body Diode Reverse Recovery Charge	Q_{rr}			10	20	nC
Reverse Recovery Fall Time	t_a			9		ns
Reverse Recovery Rise Time	t_b			16		

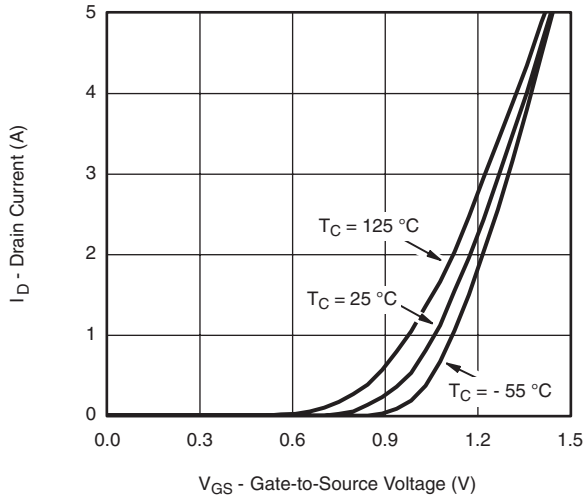
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

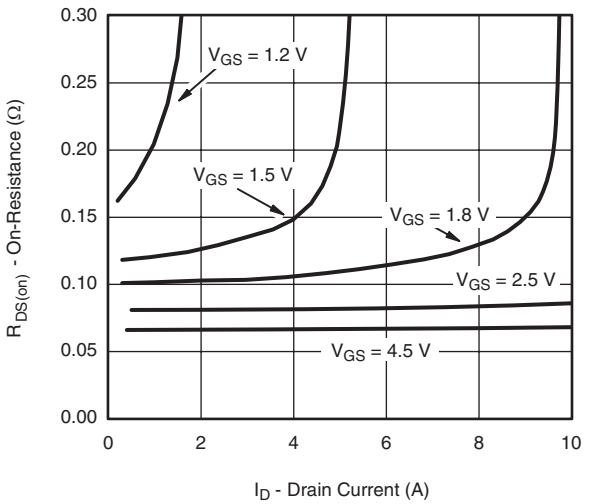
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



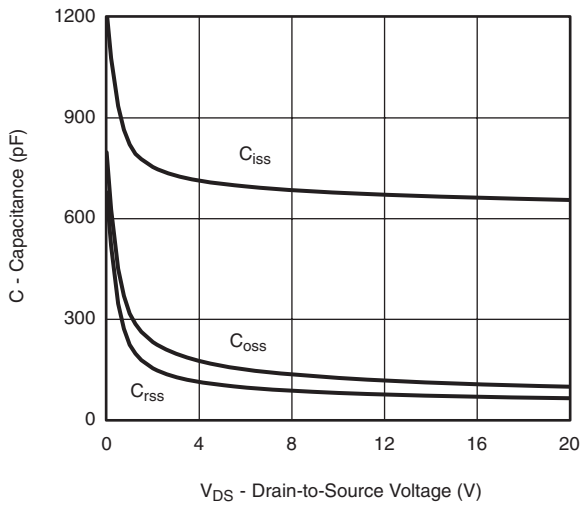
Output Characteristics



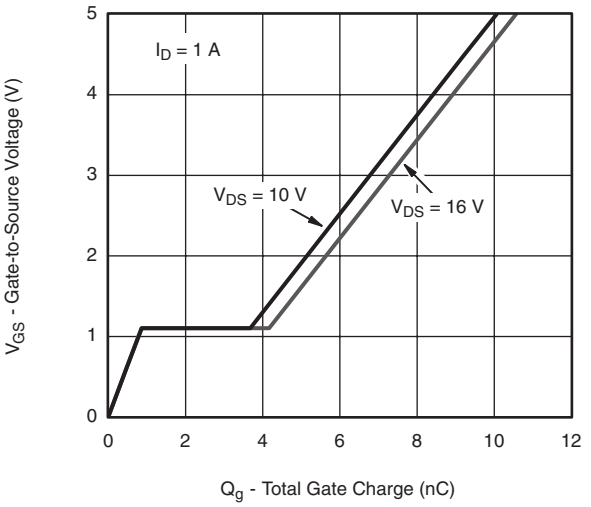
Transfer Characteristics



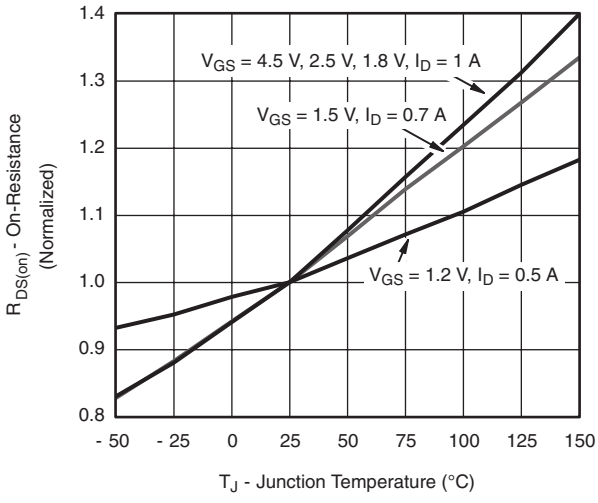
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

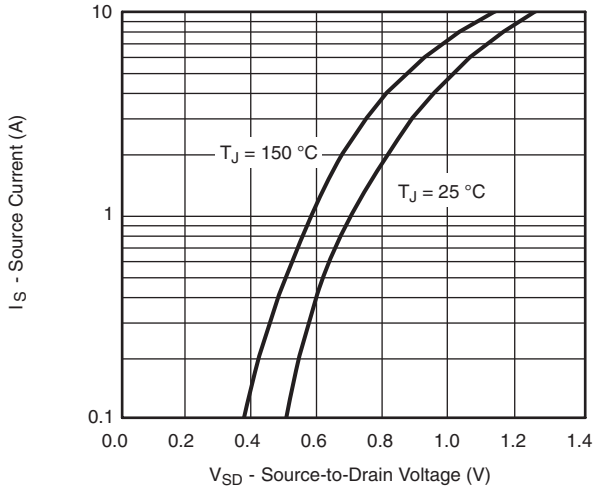


Gate Charge

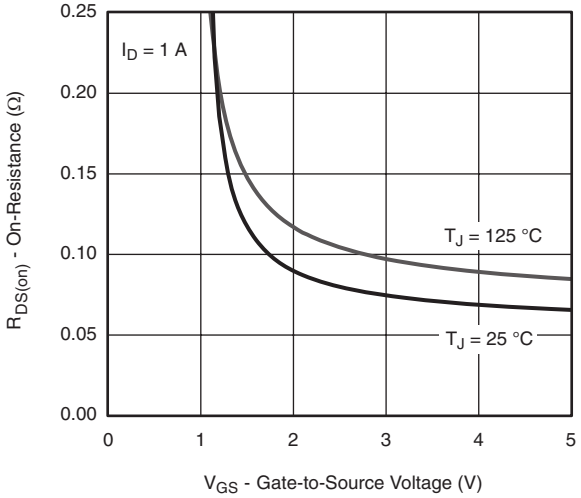


On-Resistance vs. Junction Temperature

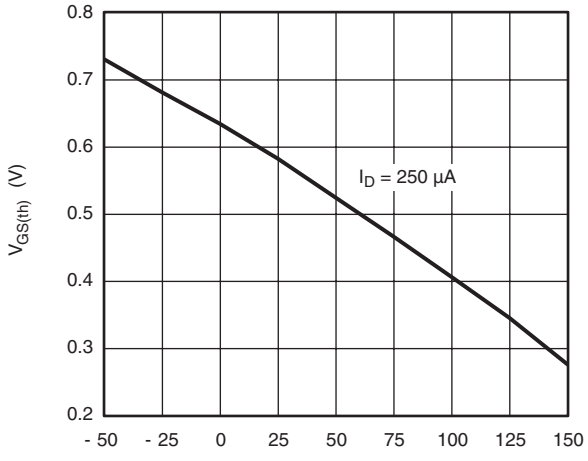
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



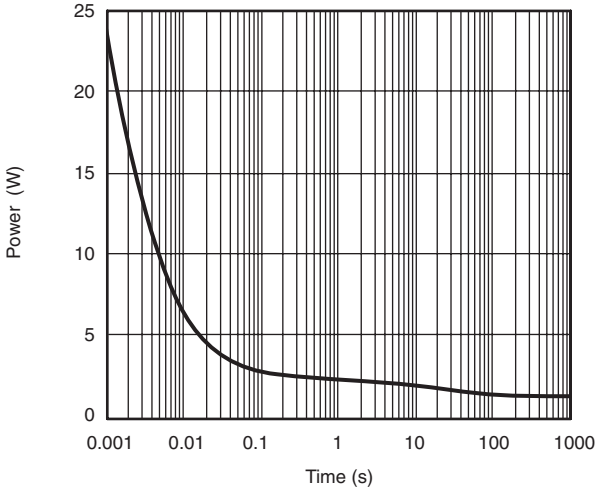
Source-Drain Diode Forward Voltage



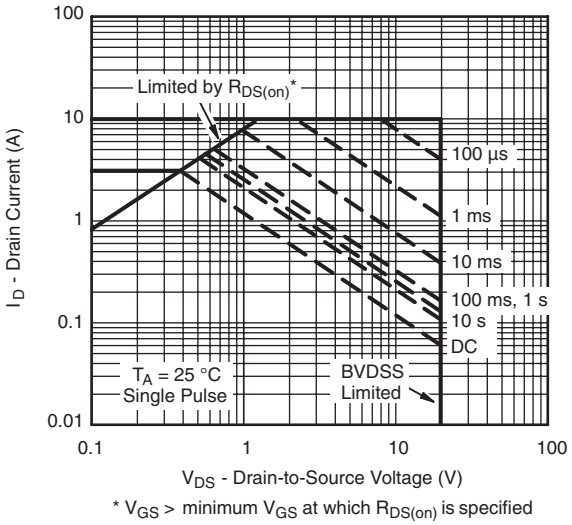
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



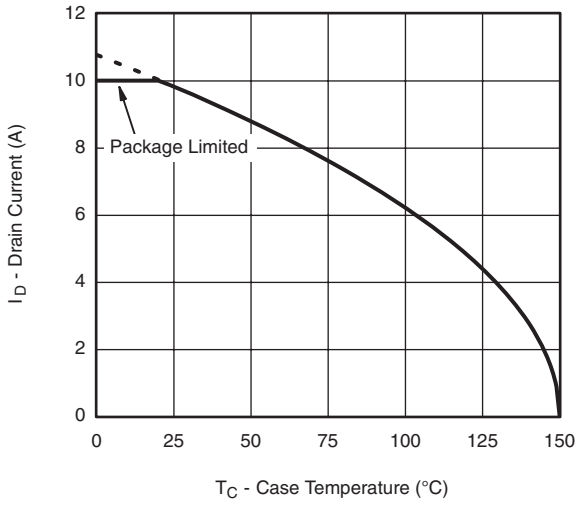
Single Pulse Power, Junction-to-Ambient



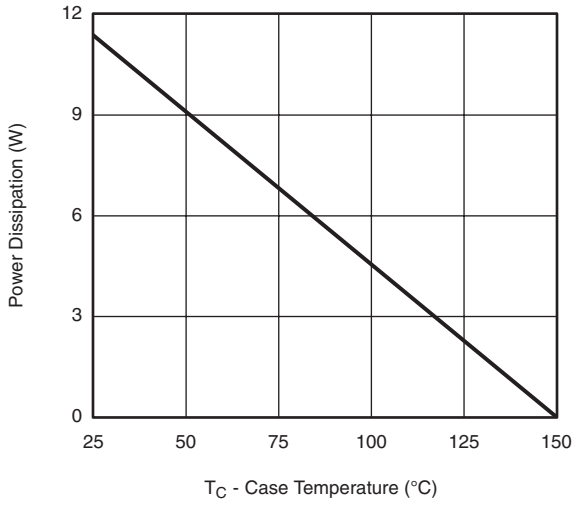
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



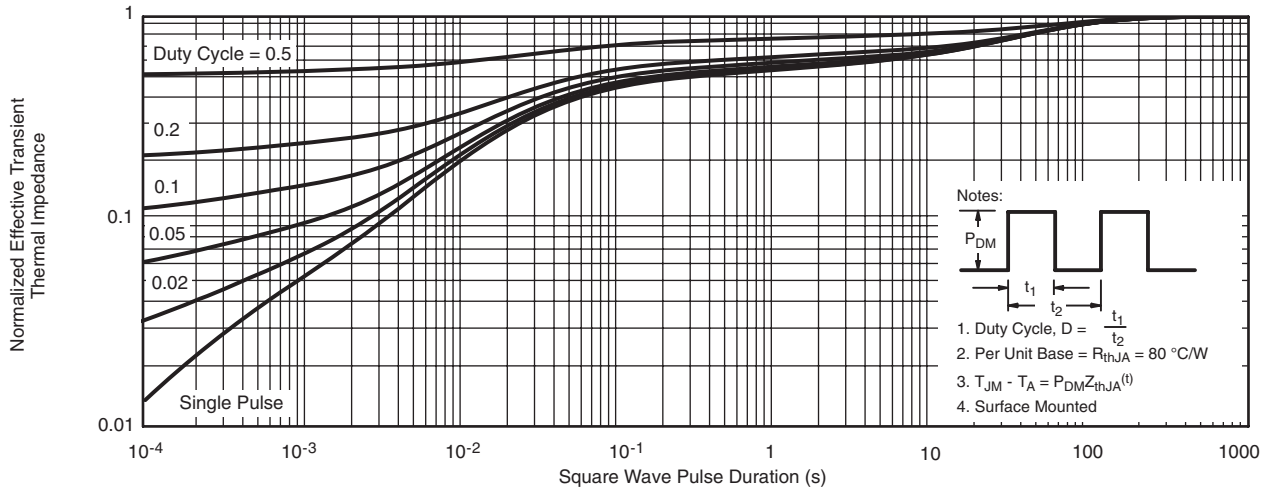
Current Derating*



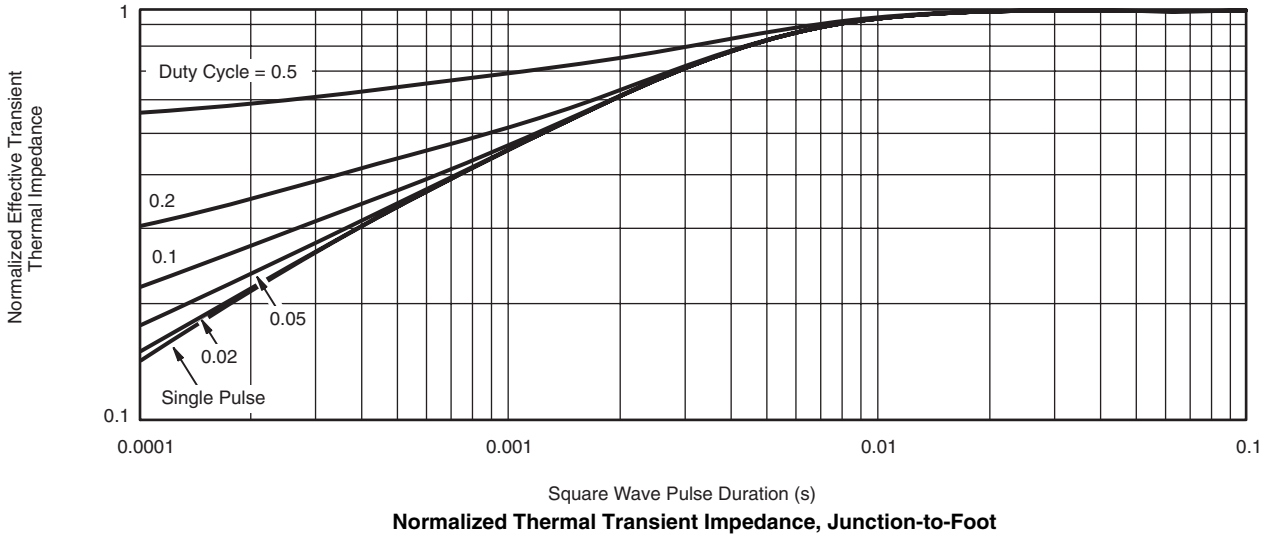
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



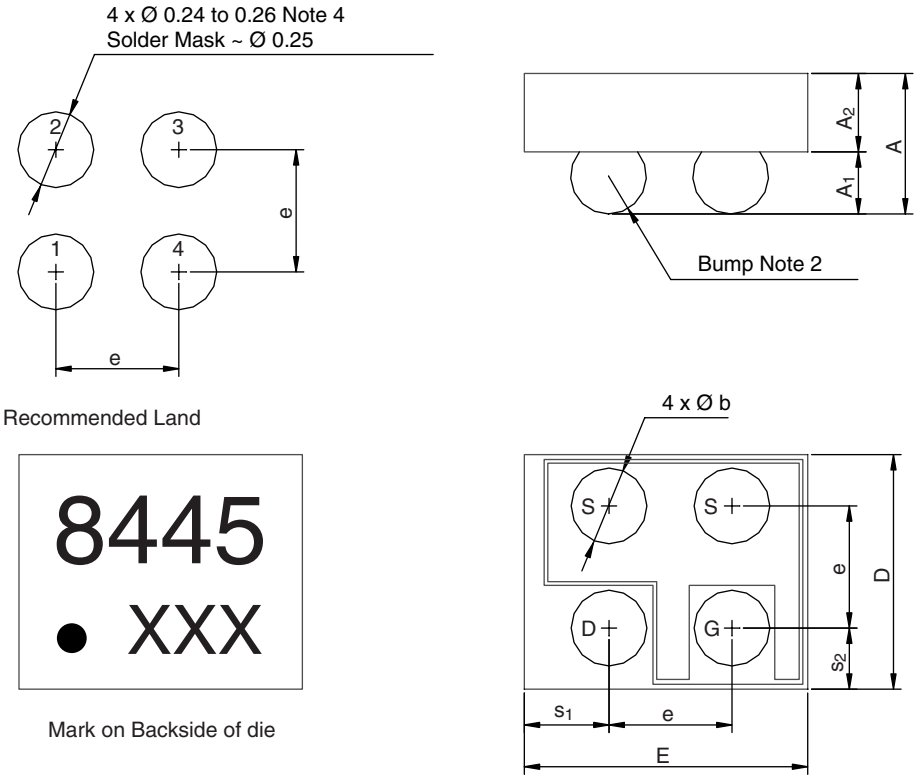
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (2 x 2, 0.5 mm PITCH)



Notes (Unless otherwise specified):
1. All dimensions are in millimeters.
2. Four (4) solder bumps are lead (Pb)-free 95.5Sn/3.8Ag/0.7Cu with diameter ∅ 0.30 to 0.32 mm.
3. Backside surface is coated with a Ti/Ni/Ag layer.
4. Non-solder mask defined copper landing pad.
5. • is location of pin 1.

Dim.	Millimeters[a]			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.510	0.550	0.590	0.0201	0.0217	0.0232
A_1	0.220	0.250	0.280	0.0087	0.0098	0.0110
A_2	0.290	0.300	0.310	0.0114	0.0118	0.0122
b	0.300	0.310	0.320	0.0118	0.0122	0.0126
e		0.500			0.0197	
s_1	0.330	0.340	0.350	0.0130	0.0134	0.0138
s_2	0.230	0.240	0.250	0.0090	0.0094	0.0098
D	0.960	0.980	1.000	0.0378	0.0388	0.0394
E	1.160	1.180	1.200	0.0457	0.0465	0.0472

Notes:
a. Use millimeters as the primary measurement.

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