User's Guide

TPSI3052Q1EVM Automotive Reinforced Isolated Switch Driver with Integrated 15-V Gate Supply EVM User's Guide

ABSTRACT

TPSI3052Q1EVM EVM (Evaluation Module) helps designers evaluate the operation and performance of the isolated switch driver, TPSI3052-Q1. This user's guide provides the connectors, test point descriptions, operational modes, schematic, bill of materials, and board layout of the EVM. The TPSI3052-Q1 is a 5-kV_{RMS} reinforced isolated switch driver with 1.5-A peak source current and 3-A peak sink current. The device is able to generate a regulated secondary power supply of 15 V. This regulated power supply allows for a wide selection of power switches, such as MOSFETs, IGBTs, and SiC. The EVM includes two back-to-back N-Channel 750-V 28-A silicon carbide (*SiC*) MOSFET in a TO-247-3L package. The inputs and outputs connections to the board are terminal blocks, which allow for easy wired connections. The EVM is rated for a load up to 500-V_{DC}/350-V_{RMS} and 4 A. The board contains multiple test points to monitor the TPSI3052-Q1 functionality. In addition, the EVM contains an adjustable LDO to supply VDDP from a battery to the input of the TPSI3052-Q1 with an output of 5 V. The EVM allows the user to test multiple applications, such as AC/DC solid state relay (SSR), battery management, and precharge circuits.

	**Caution**	**Do not leave EVM powered when unattended**
	**Caution**	**Read the user's guide before use**
	**Caution**	**Caution hot surface Contact can cause burns Do not touch!**
	**Danger**	**Do not use EVM to test Isolation above V_{IOWM} = 1414-V_{DC} High voltage**

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Trademarks

General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://ti.com/customer support for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitably qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety:
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non-conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:
   a. As a precautionary measure, it is always good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   b. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   d. Once EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety
   a. Wear personal protective equipment e.g. latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

1 Introduction

The TPSI3052-Q1 is a fully integrated isolated switch driver, that when combined with an external power switch, forms a complete isolated solid state relay solution. The TPSI3052-Q1 is designed for automotive and industrial applications such as battery management systems, EV/HEV on-board chargers, replacing mechanical relays with SSR, DC link pre-charging, and more. The TPSI3052-Q1 seamlessly replaces relays without need for a secondary side supply while leveraging unique isolation technology integrated in a compact SOIC package. The TPSI3052-Q1 integrated isolation protection is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than those found using traditional mechanical relays and optocouplers.

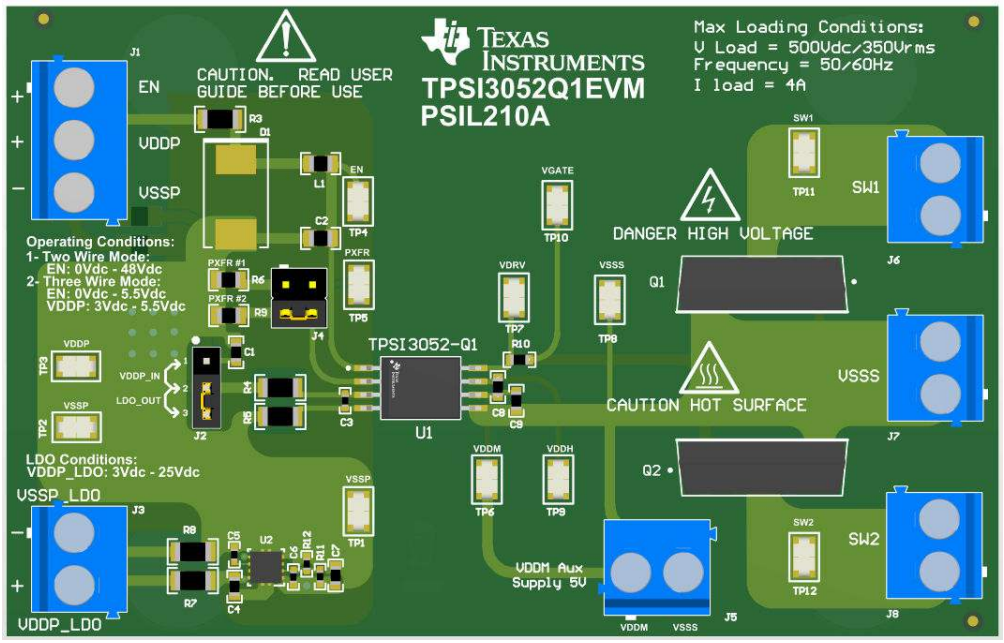

Figure 1-1. PCB View

1.1 Features

- No isolated secondary supply required
- Drives external power transistors or SCRs
- 5-kV_{RMS} reinforced isolation
- 15-V gate drive with 1.5-A peak source current and 3-A peak sink current
- Up to 50-mW supply for external auxiliary circuitry
- Supports AC or DC switching
- Supports two-wire or three-wire modes
- Seven levels of power transfer, resistor selectable

1.2 Applications

- Solid State Relay (SSR)
- Hybrid, electric, and powertrain systems
- Building automation
- Factory automation and control

1.3 Description

TPSI3052Q1EVM allows users to easily switch between the two operational modes for evaluation. The EVM is designed with the flexibility to add Common Mode Chokes to minimize EMI. Figure 1-2 shows the functional block diagram for the isolated switch. The TPSI3052-Q1 is able to generate a floating secondary supply of 15 V with a 1.5-A peak source current and 3-A peak sink current. In addition, TPSI3052-Q1 supports two operation modes: two-wire and three-wire mode. In two-wire mode, the EN pin provides the power on the primary side. Use three-wire mode for applications that require higher levels of power transfer and the fastest enable and disable switch times the TPSI3052-Q1 can offer.

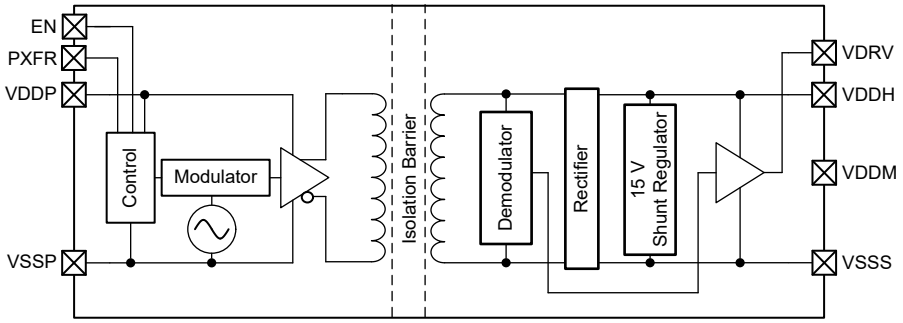

Figure 1-2. TPSI3052-Q1 Functional Block Diagram

Table 1-1. Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)	FUNCTIONALITY
TPSI3052-Q1	SOIC 8 pin (DWZ)	7.50 mm × 5.85 mm	Standard Enable
TPSI3052S-Q1	SOIC 8 pin (DWZ)	7.50 mm × 5.85 mm	Available in three-wire mode only, the TPSI3052S features a one-shot enable for the switch control. This feature is useful for driving SCRs that typically require only one pulse of current to trigger.

(1) For all available packages, see the orderable addendum at the end of the data sheet.

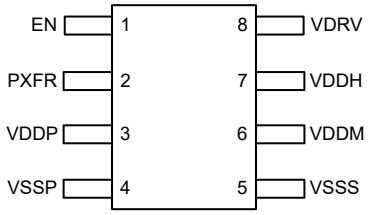

Figure 1-3. TPSI3052-Q1, TPSI3052S-Q1 DWZ Package 8-Pin SOIC Top View

2 Connection Descriptions

Table 2-1 shows the functionality of the test points, connectors, and terminal block.Table 2-2 shows the pin functions.

Table 2-1. Test Points and Jumpers

Name	Description
J2	VDDP power select input
J4	Power transfer select
TP1, TP2	VSSP test point
TP3	VDDP signal test point
TP4	EN signal test point
TP5	PXFR signal test point
TP6	VDDM signal test point
TP7	VDRV signal test point
TP8	VSSS signal test point
TP9	VGATE signal test point
TP10	VDDH signal test point
TP11	SW1 signal test point
TP12	SW2 signal test point

Table 2-2. Pin Functions

Pin Name	Description
EN	Active high driver enable
PXFR	Power transfer may be adjusted by selecting one of seven power level settings using an external resistor from the PXFR pin to VSSP.
VDDP	Power supply for primary side
VSSP	Ground supply for primary side
VSSS	Ground supply for secondary side
VDDM	Generated mid supply
VDDH	Generated high supply
VDRV	Active high driver output

3 Operating Modes

3.1 Two-Wire Mode

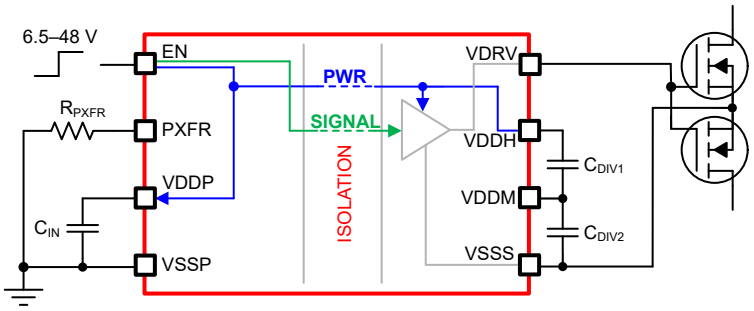

Figure 3-1. Two-Wire Mode Simplified Schematic

In two-wire mode, the TPSI3052-Q1 can be controlled using two pins, EN and VSSP. When EN is greater or equal to 6.5 V, power is drive to the device. When the EN voltage is high, power gets delivered into the secondary side of the device. When EN is low, then power transfer into the secondary side stops and the MOSFETs or SCRs turns off.

To configure the EVM for two-wire mode, the following changes must be made:

1. Remove J2-Header. Leave VDDP floating with Cin to VSSP.
2. Supply the EN voltage using the terminal block J1.

Figure 3-2 provides a visual representation of how to configure the board for the two-wire mode:

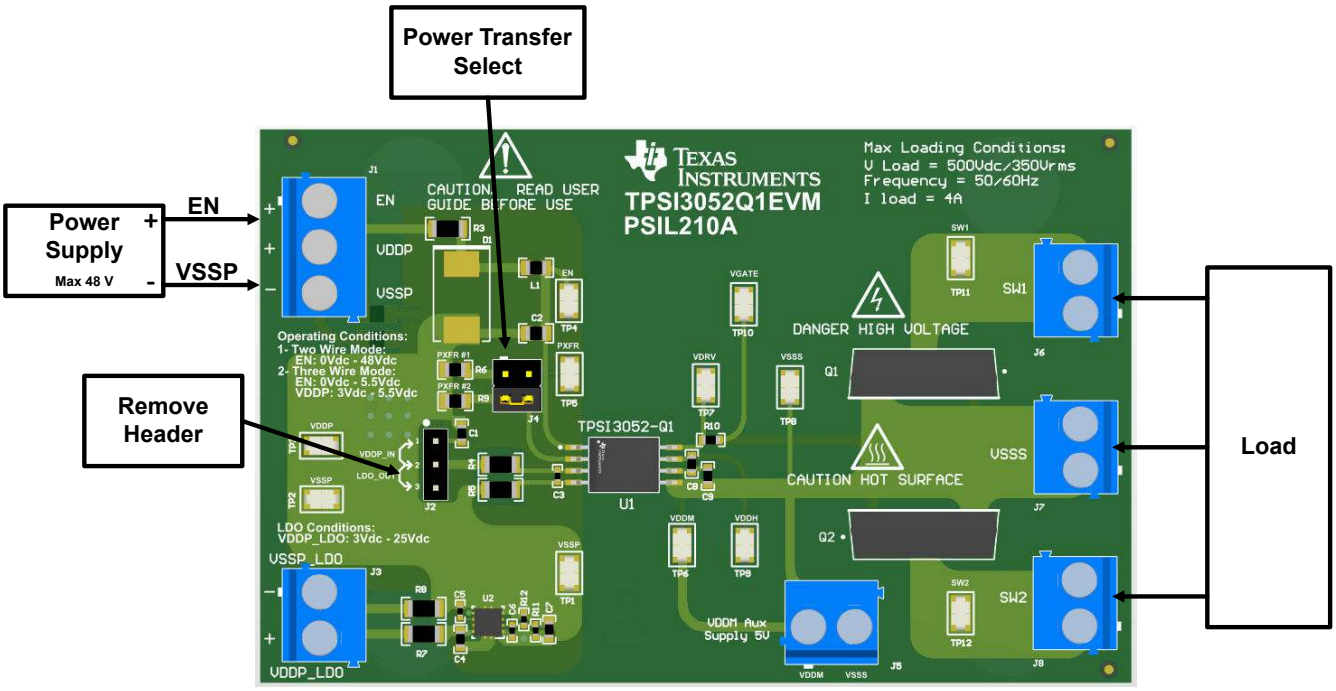

Figure 3-2. Two-Wire Mode Setup

Table 3-1. Power Selection for Two-Wire Mode

J4-Header	I_{EN}
PXFR #1 (7.32 kΩ)	1.9 mA
PXFR #2 (20 kΩ)	6.7 mA

Measurements

Figure 3-3 shows the powering up delay from EN rising to VDDM and VDDP rising using the highest power transfer PXFR #2 (20 kΩ) in two-wire mode. The power up delay is directly related to the power transfer selection and to the capacitors from VDDH to VDDM and VDDM to VSSS. The delay from EN to VDDM is 2 ms and the delay from EN to VDDH is 1.83 ms. Figure 3-3 shows the delay from EN rising to VDRV rising using the highest power transfer PXFR #2 (20 kΩ) in two-wire mode. The delay from EN to VDRV is 3.533 ms. Figure 3-5 shows the delay from EN falling to VDRV falling. The delay is 2.463 us.

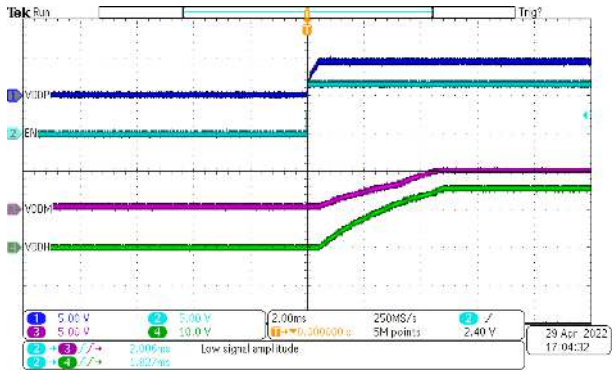

Figure 3-3. Two-Wire Mode Powering Up

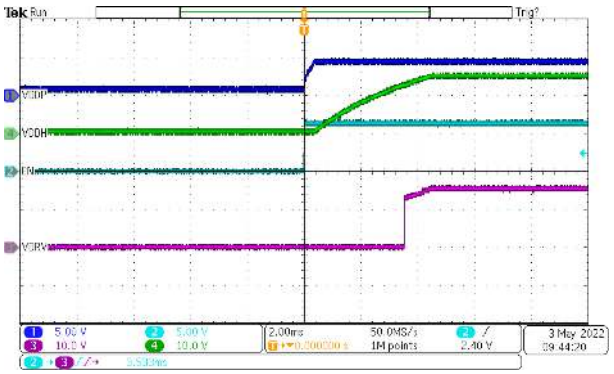

Figure 3-4. Two-Wire Mode Switching ON

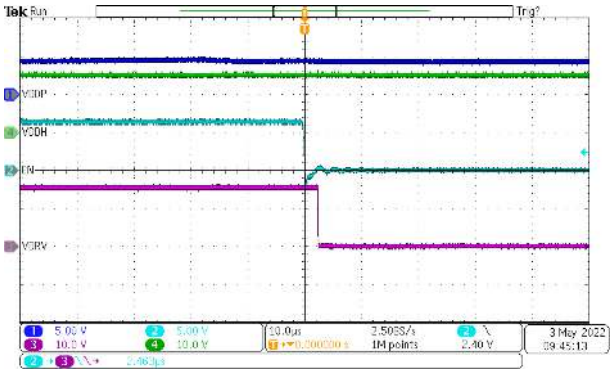

Figure 3-5. Two-Wire Mode Switching OFF

3.2 Three-Wire Mode

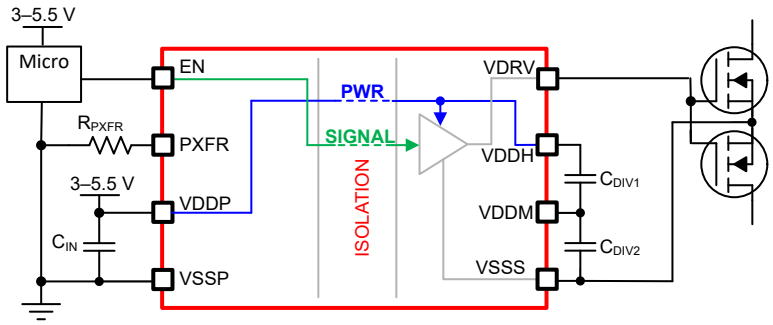

Figure 3-6. Three-Wire Mode Simplified Schematic

Use three-wire mode for applications that require higher levels of power transfer and the fastest enable and disable switch times the TPSI3052-Q1 can offer. In this mode, power transfers from the primary to secondary side independent of the enable pin state. Setting EN pin high or low asserts the V_{DRV} to drive the external power MOSFETs or SCRs.

To configure the EVM for three-wire mode, the following changes must be made:

1. J2 header allows to supply VDDP directly or indirectly through an LDO with a 5-V output.

a. Supply VDDP directly: place J2 shunt between positions 1-2. This action allows the user to supply VDDP directly.

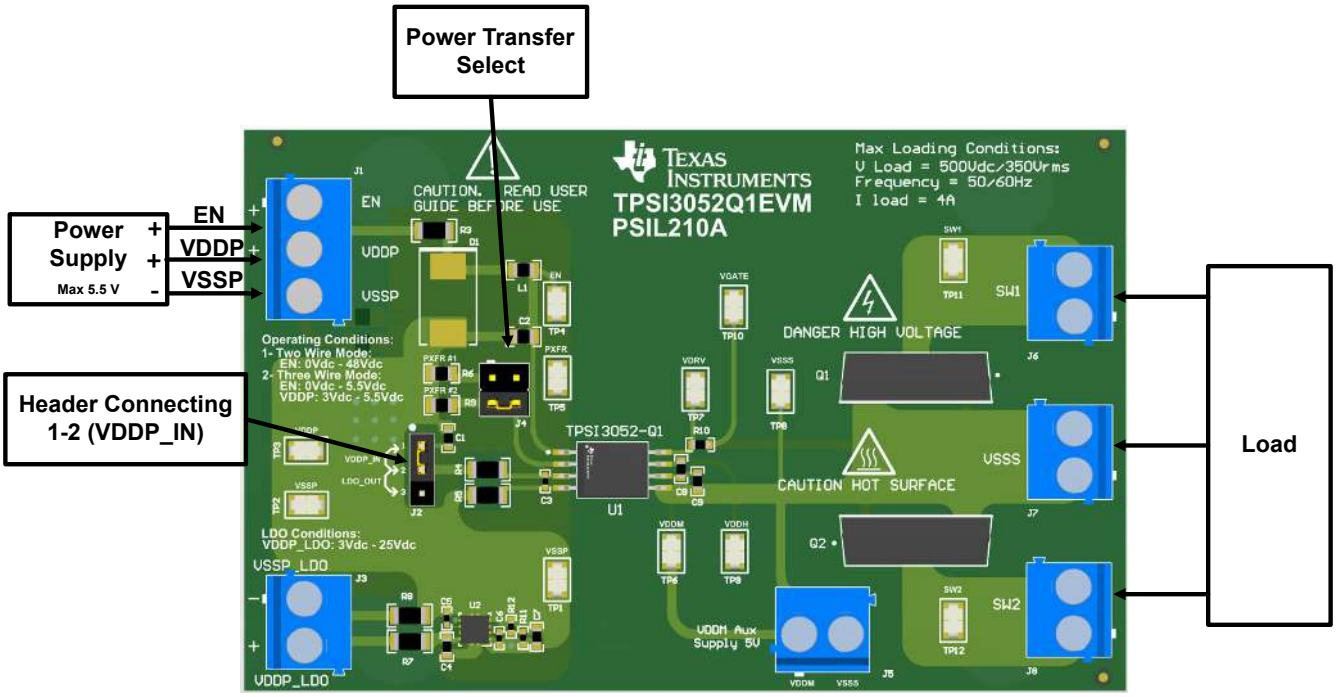

Figure 3-7. Three-Wire Mode VDDP Direct Supply

b. Supply VDDP through LDO: place the J2 shunt between positions 2-3. The user can supply VDDP indirectly through an LDO with a 5-V output.

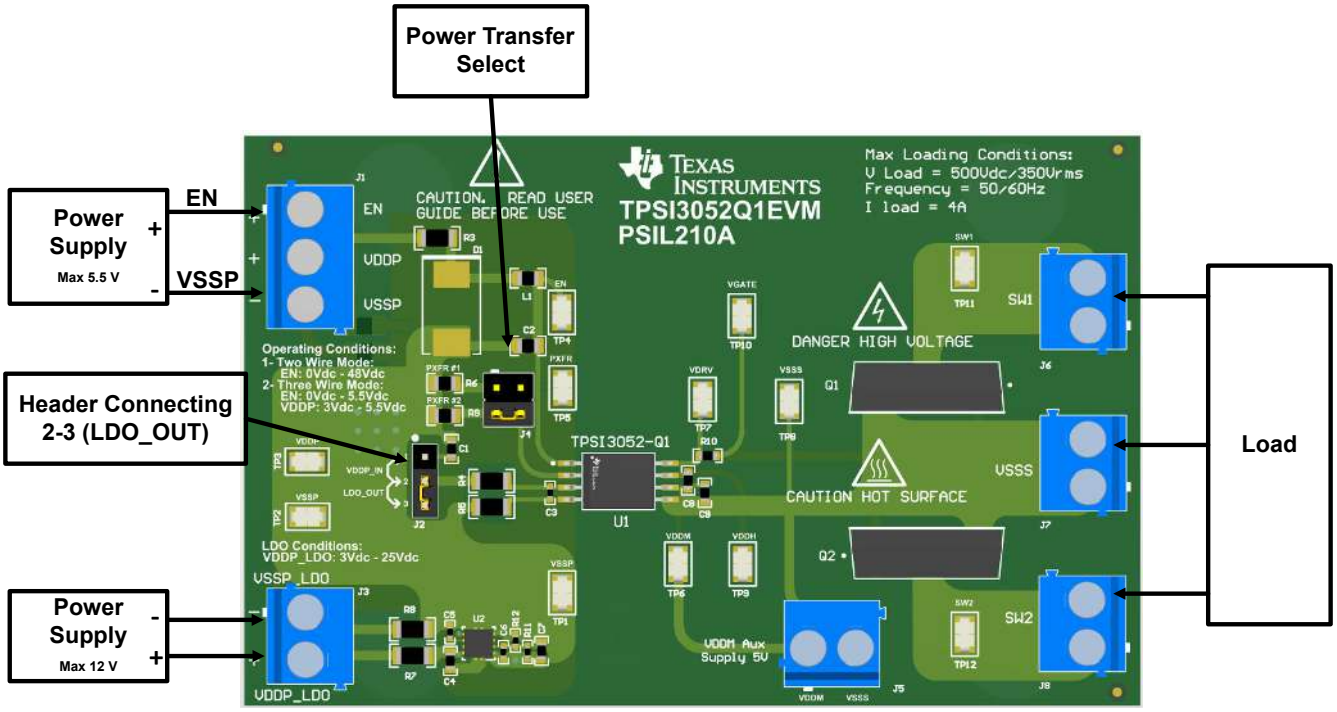

Figure 3-8. Three-Wire Mode VDDP Supply Through 5-V LDO

2. Supply the EN voltage using the terminal block J2.

Table 3-2. Power Selection for Three-Wire Mode

J4-Header	Power Converter Duty Cycle (Three-Wire Mode, Nominal)
PXFR #1 (7.32 kΩ)	13.3%
PXFR #2 (20 kΩ)	93.3%

Measurements

Figure 3-9 shows the powering up delay from VDDP rising to VDDM and VDDP rising using the highest power transfer PXFR #2 (20 kΩ) in three-wire mode. The power up delay is directly related to the power transfer selection and to the capacitors from VDDH to VDDM and VDDM to VSSS. The delay from VDDP to VDDM is 425.7 us and the delay from VDDP to VDDH is 395 us. Figure 3-9 shows the delay from EN rising to VDRV rising using the highest power transfer PXFR #2 (20 kΩ) in three-wire mode. The delay from EN to VDRV is 3.141 us. Figure 3-11 shows the delay from EN falling to VDRV falling. The delay is 2.489 us.

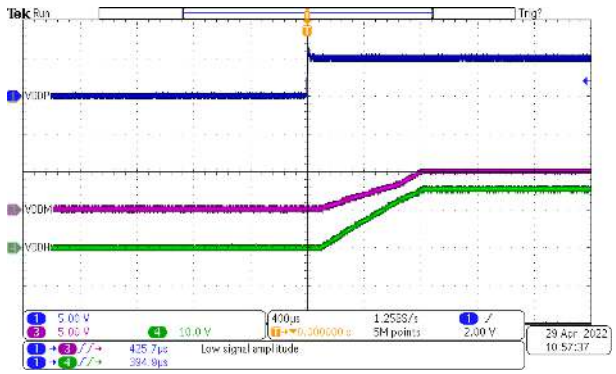

Figure 3-9. Three-Wire Mode Powering Up

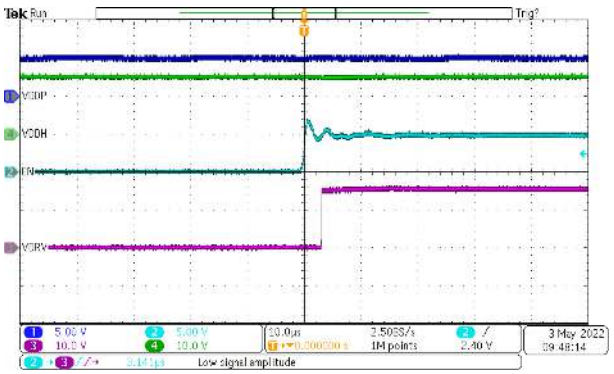

Figure 3-10. Three-Wire Mode Switching ON

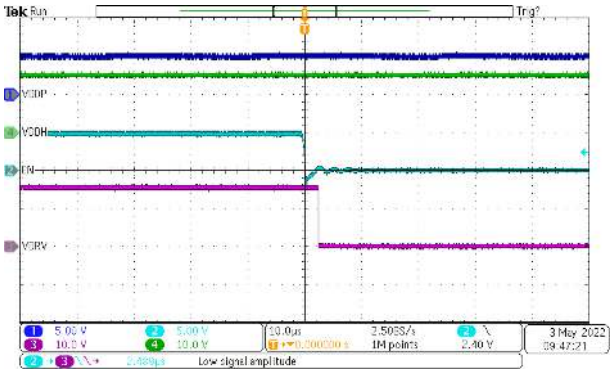

Figure 3-11. Three-Wire Mode Switching OFF

4 Load Configurations

This EVM is designed to support different load configurations to maximize flexibility to the user.

1. MOSFET configurations:
   a. Figure 4-1 shows an application using two back-to-back common source MOSFETs. By connecting the load between terminals SW1-SW2, the user can load the EVM with an AC or a DC load. By using two back-to-back FETs, the body diodes are able to stand off both positive and negative voltages. In addition, an RC snubber can be added for damping the switching oscillations in presence of a highly inductive load.

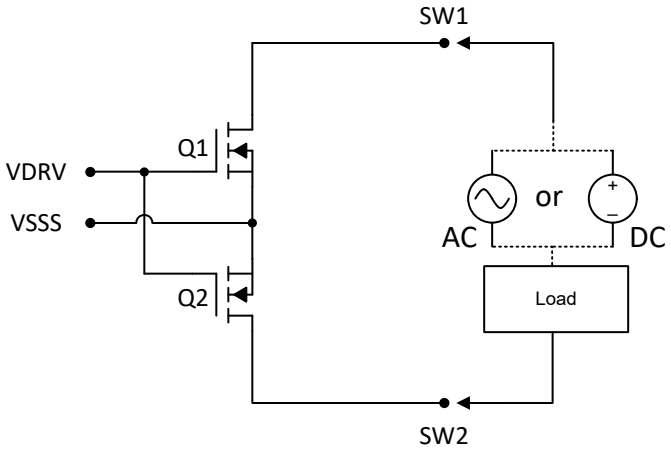

Figure 4-1. AC/DC Load

   b. Figure 4-2 shows an application using two parallel common source MOSFETs. This action allows the users to achieve lower RDSON. Because one MOSFET cannot block reverse current when off, the recommended load for this configuration is a DC load.

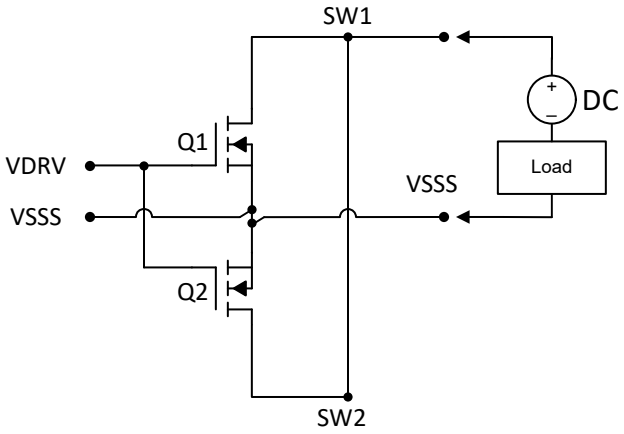

Figure 4-2. DC Load

5 Schematic

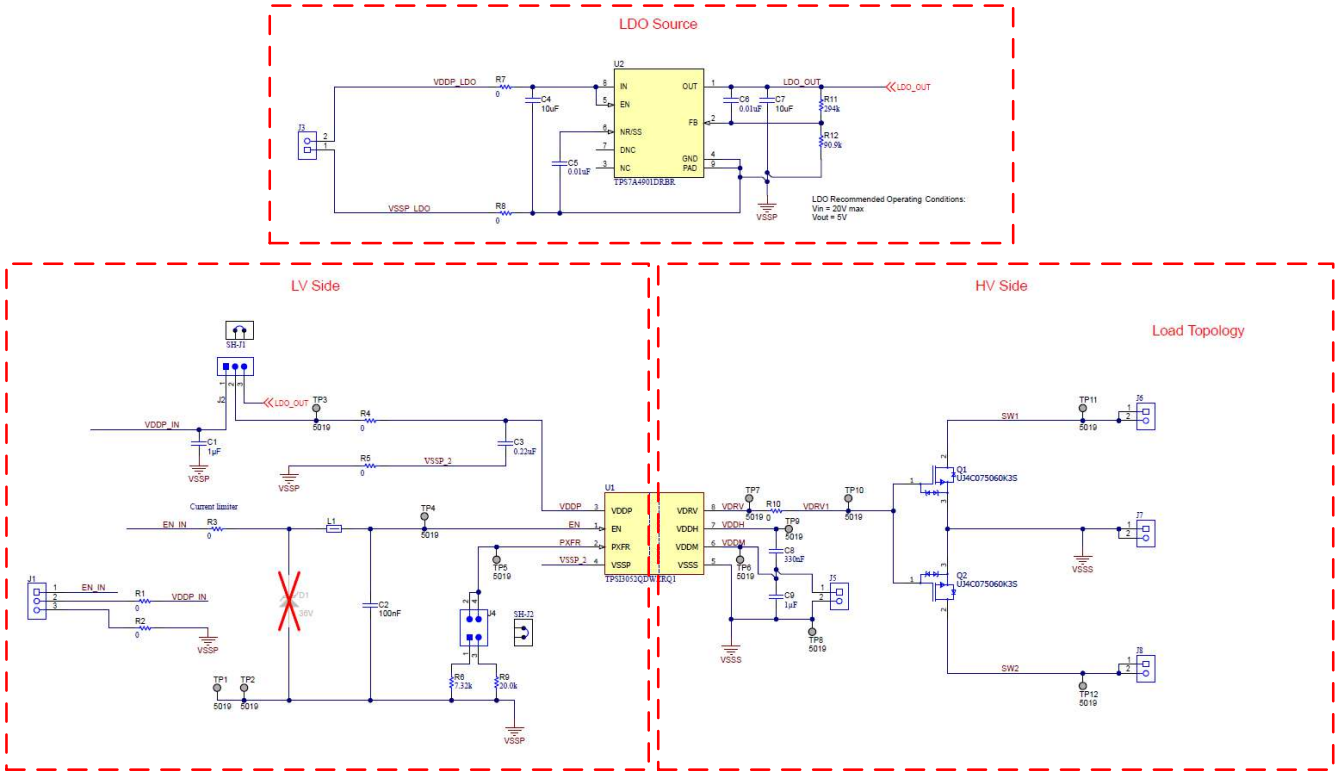

Figure 5-1. PSIL210 Schematic

6 Layout

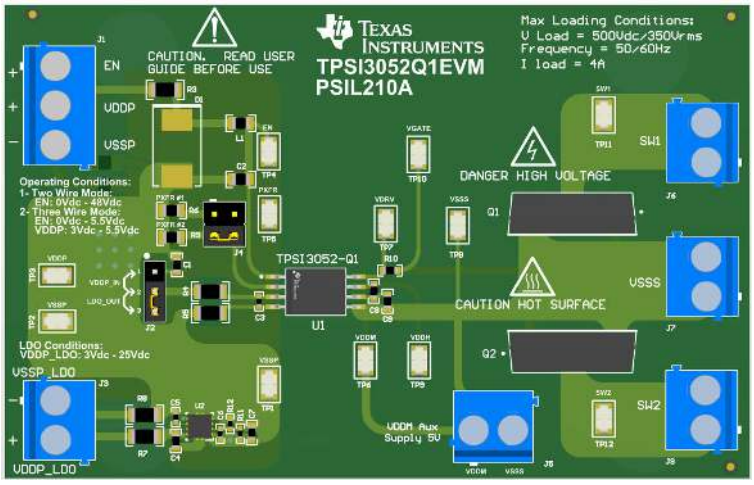

Figure 6-1. 3D View

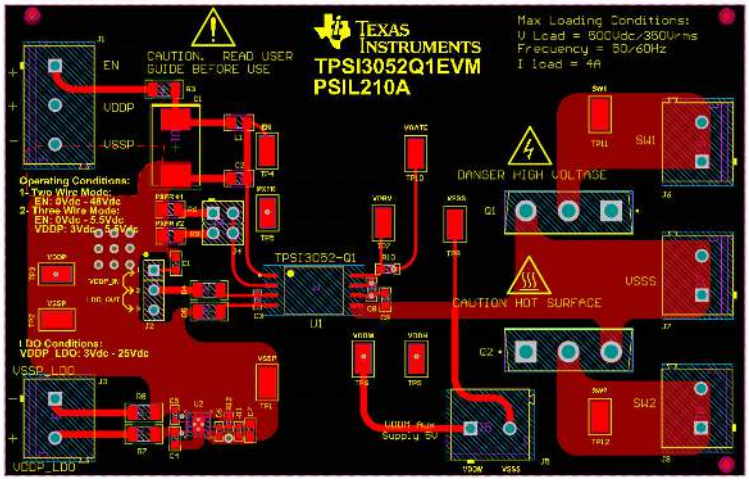

Figure 6-2. PCB Top Layer

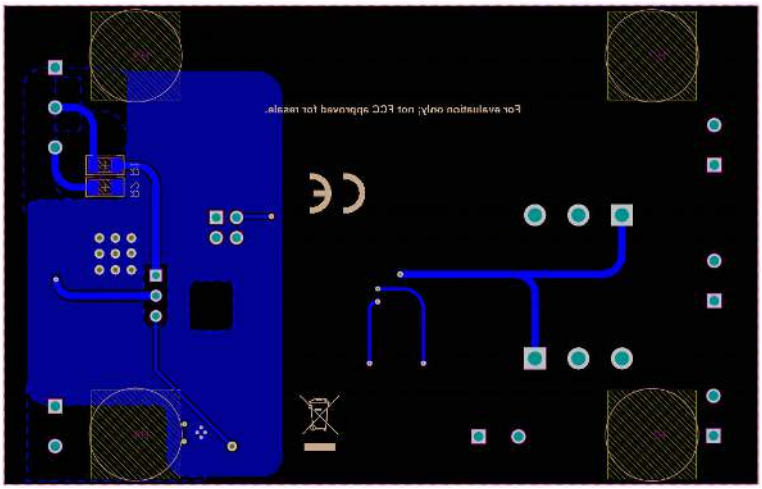

Figure 6-3. PCB Bottom Layer

7 Bill of Materials

Table 7-1. Bill of Materials

Designator	Quantity	Description	Part Number	Manufacturer
C1, C9	2	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R71E105KA64D	MuRata
C2	1	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	GCM21BR71H104KA37K	MuRata
C3	1	CAP, CERM, 0.22 uF, 16 V, +/- 10%, X7R, 0402	GRM155R71C224KA12D	MuRata
C4, C7	2	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603	GRT188R61E106ME13D	MuRata
C5, C6	2	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0402	GRM155R71E103KA01D	MuRata
C8	1	CAP, CERM, 0.33 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E3X7R1H334K080AB	TDK
H1, H2, H3, H4	4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	SJ-5303 (CLEAR)	3M
J1	1	Terminal Block, 5 mm, 3x1, Tin, TH	691 101 710 003	Wurth Elektronik
J2	1	Header, 100mil, 3x1, Tin, TH	PEC03SAAN	Sullins Connector Solutions
J3, J5, J6, J7, J8	5	Terminal Block, 5 mm, 2x1, Tin, TH	691 101 710 002	Wurth Elektronik
J4	1	Header, 2.54mm, 2x2, Gold, TH	PBC02DAAN	Sullins Connector Solutions
L1	1	Ferrite Bead, 2200 ohm @ 100 MHz, 0.2 A, 0805	742792094	Wurth Elektronik
Q1, Q2	2	N-Channel 750 V 28A (Tc) 155W (Tc) Through Hole TO-247-3	UJ4C075060K3S	UnitedSiC
R1, R2, R4, R5, R7, R8	6	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	ERJ-8GEY0R00V	Panasonic
R3	1	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	CRCW12060000Z0EA	Vishay-Dale
R6	1	RES, 7.32 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	ERJ-6ENF7321V	Panasonic
R9	1	RES, 20.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	ERJ-6ENF2002V	Panasonic
R10	1	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3GEY0R00V	Panasonic
R11	1	RES, 294 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2RKF2943X	Panasonic
R12	1	RES, 90.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2RKF9092X	Panasonic
SH-J1, SH-J2	2	Shunt, 100mil, Gold plated, Black	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12	12	Test Point, Miniature, SMT	5019	Keystone
U1	1	Automotive Reinforced Isolated Switch Driver With Integrated 15 V Gate Supply	TPSI3052QDWZRQ1	Texas Instruments

Table 7-1. Bill of Materials (continued)

Designator	Quantity	Description	Part Number	Manufacturer
U2	1	Vin 3V to 36V, 150mA, Ultra-Low-Noise, High-PSRR Low-Dropout (LDO) Linear Regulator, DRB0008A (VSON-8)	TPS7A4901DRBR	Texas Instruments
D1	0	Diode, TVS, Uni, 36 V, 58.1 Vc, SMC	NOT POPULATED	NOT POPULATED
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	NOT POPULATED	NOT POPULATED

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