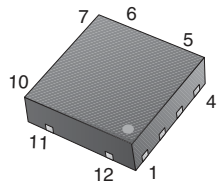
STL11N65M5

N-channel 650 V, 0.475 Ω typ., 8.5 A MDmesh™ M5 Power MOSFET in a PowerFLAT™ 5x5 package

Datasheet - production data



PowerFLAT™ 5x5

Features

Order code	V_{DS} @ $T_{j\ max.}$	$R_{DS(on)}$ max	I_D
STL11N65M5	710 V	0.530 Ω	8.5 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Figure 1. Internal schematic diagrams

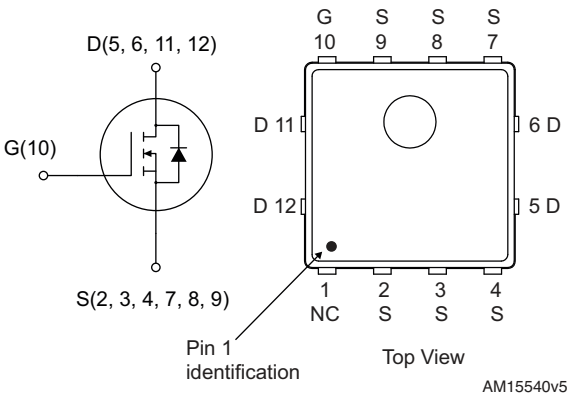


Table 1. Device summary

Order code	Marking	Package	Packaging
STL11N65M5	11N65M5	PowerFLAT™ 5x5	Tape and reel

This is information on a product in full production. www.st.com

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	8.5	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	4.9	A
I_{DM} (1),(2)	Drain current (pulsed)	34	A
I_D(3)	Drain current (continuous) at T_{pcb}=25°C	1.35	A
$I_{D(3)}$	Drain current (continuous) at T_{pcb}=100°C	0.86	A
$I_{DM(2),(3)}$	Drain current (pulsed)	5.4	A
P_{TOT}(1)	Total dissipation at T_C = 25 °C	70	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	1.9	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	130	mJ
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature		°C

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 Board of 1 inch², 2 oz Cu (t < 100 s)
4. I_{SD} ≤ 8.5 A, di/dt ≤ 400 A/µs, $V_{Peak} \leq V_{(BR)DSS}$, V_{DD} = 400 V.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.78	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb max	58.5	°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu, t<100 sec

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V			1	µA
		V_{DS} = 650 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.25 A		0.475	0.530	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	644	-	pF
C_{oss}	Output capacitance		-	18	-	pF
C_{rss}	Reverse transfer capacitance		-	2.5	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0	-	55	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	17	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 4.5 A, V_{GS} = 10 V (see *Figure 16*)	-	17	-	nC
Q_{gs}	Gate-source charge		-	4.6	-	nC
Q_{gd}	Gate-drain charge		-	8.5	-	nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d\ (v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17*), (see *Figure 20*)	-	23	-	ns
$t_{r(v)}$	Voltage rise time		-	10	-	ns
$t_{f(i)}$	Current fall time		-	13.5	-	ns
$t_{c(off)}$	Crossing time		-	13	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		8.5	A
I_{SDM} (1) (2)	Source-drain current (pulsed)		-		34	A
V_{SD} (3)	Forward on voltage	I_{SD} = 8.5 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 8.5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 17*)	-	232		ns
Q_{rr}	Reverse recovery charge		-	2		µC
I_{RRM}	Reverse recovery current		-	17.5		A
t_{rr}	Reverse recovery time	I_{SD} = 8.5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 17*)	-	328		ns
Q_{rr}	Reverse recovery charge		-	2.8		µC
I_{RRM}	Reverse recovery current		-	17		A

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

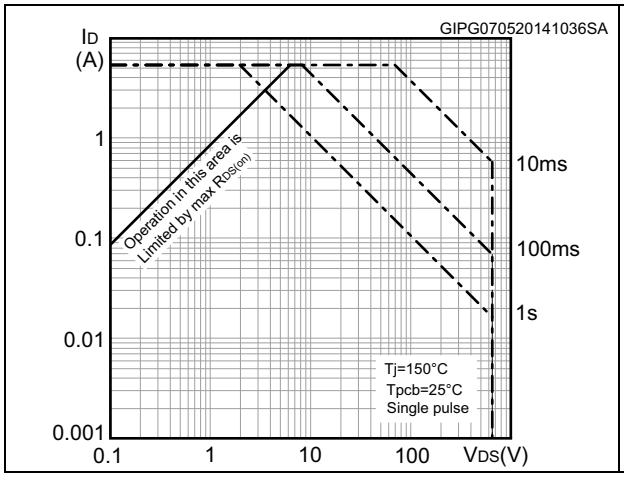


Figure 3. Thermal impedance

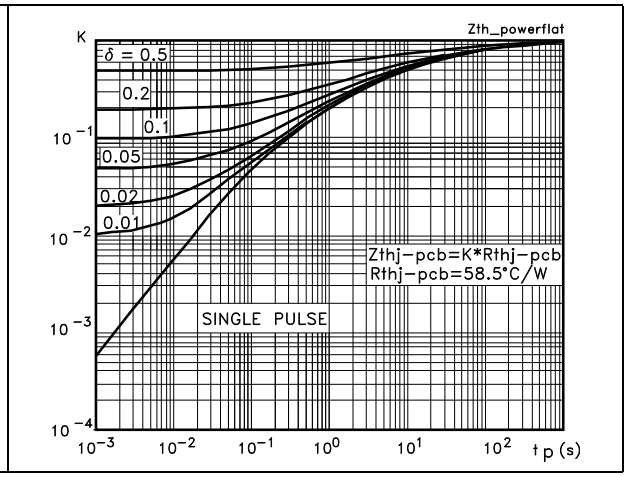


Figure 4. Output characteristics

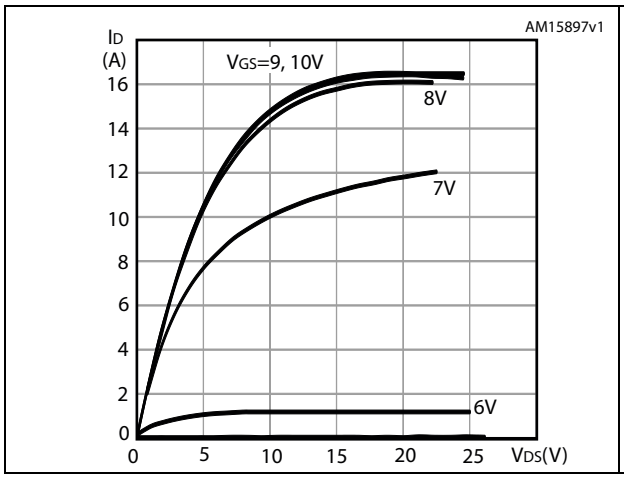


Figure 5. Transfer characteristics

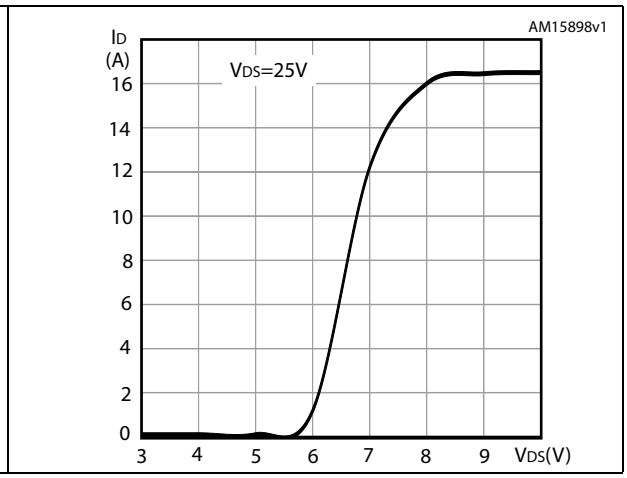


Figure 6. Static drain-source on-resistance

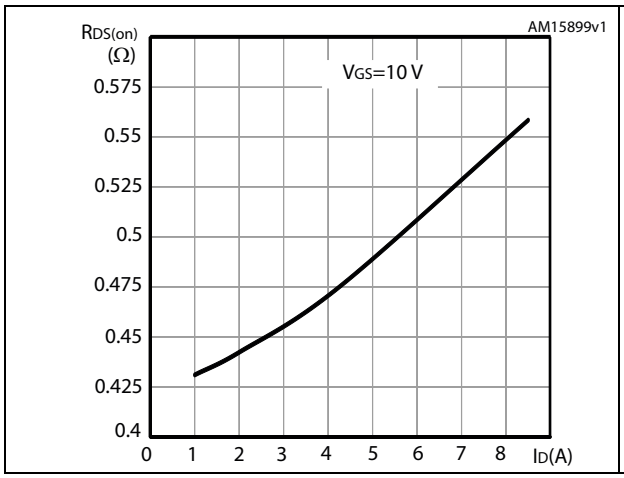


Figure 7. Gate charge vs gate-source voltage

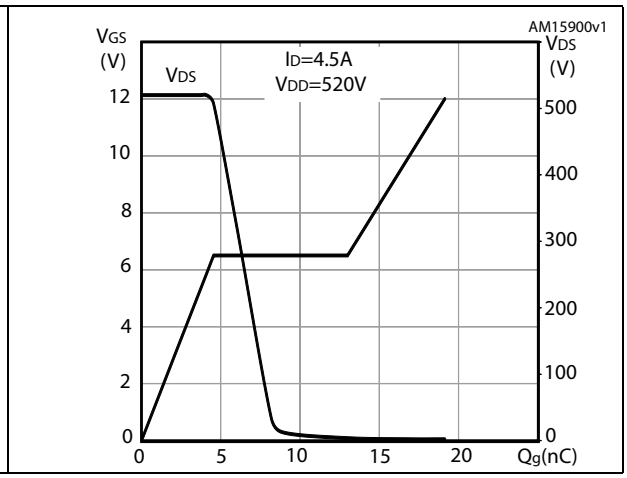


Figure 8. Capacitance variations

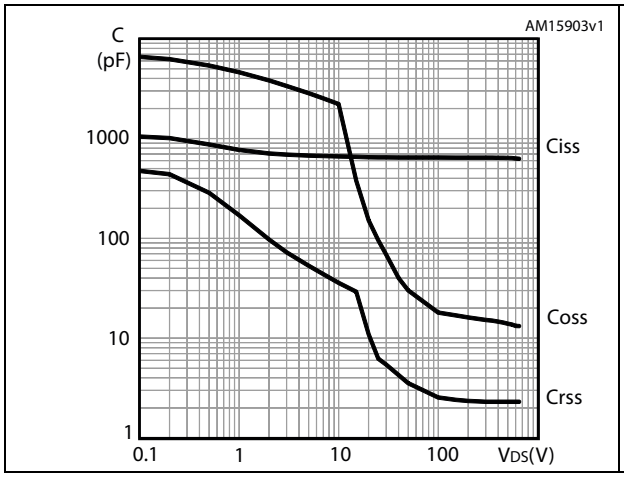


Figure 9. Output capacitance stored energy

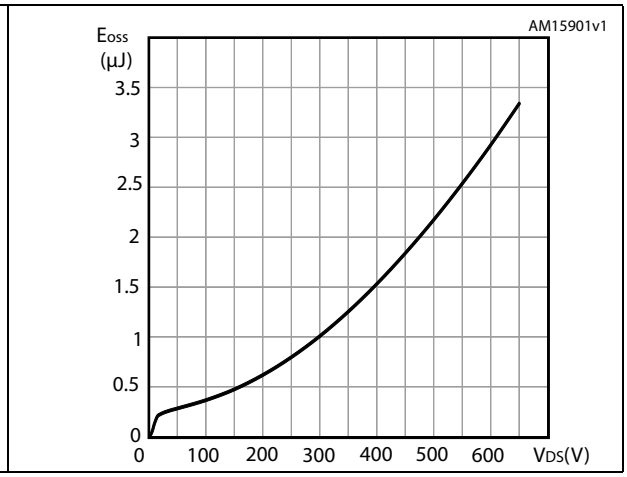


Figure 10. Normalized gate threshold voltage vs temperature

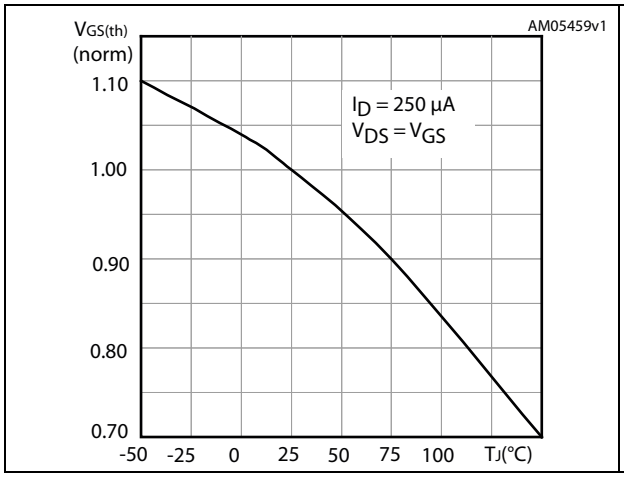


Figure 11. Normalized on-resistance vs temperature

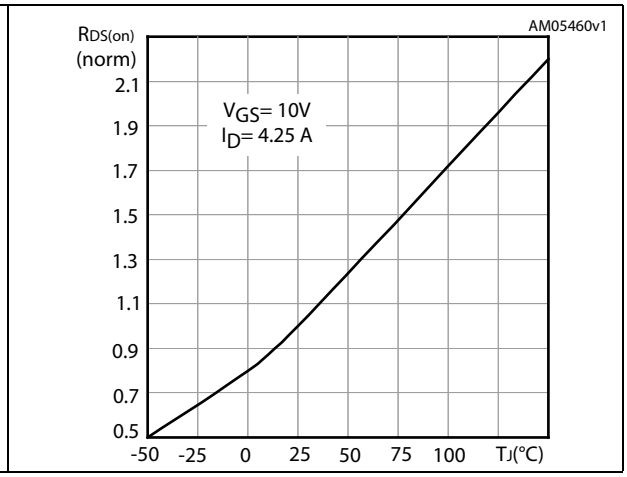


Figure 12. Source-drain diode forward characteristics

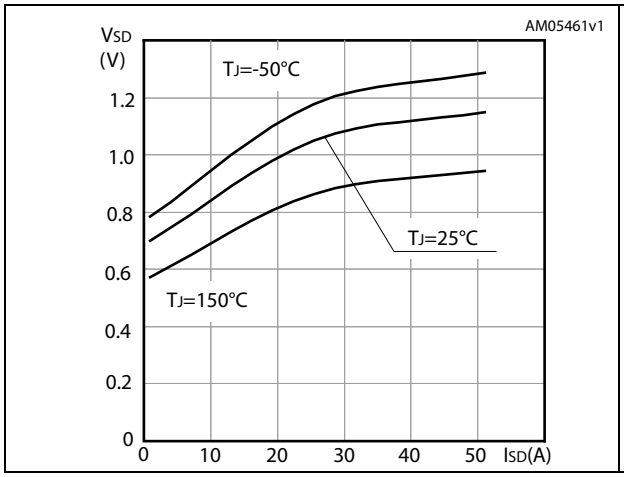


Figure 13. Normalized $V_{(BR)DSS}$ vs temperature

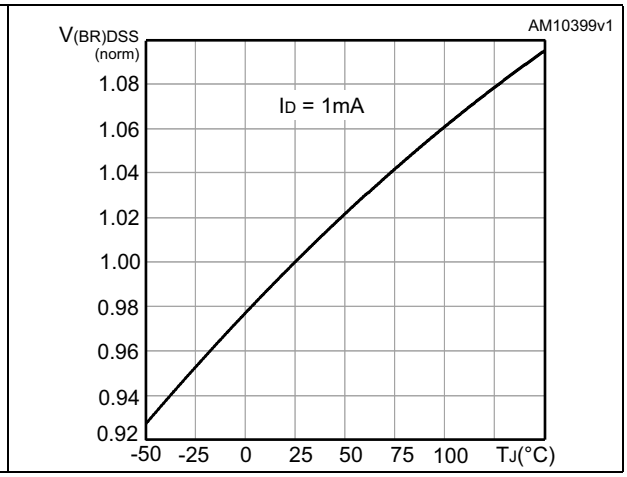
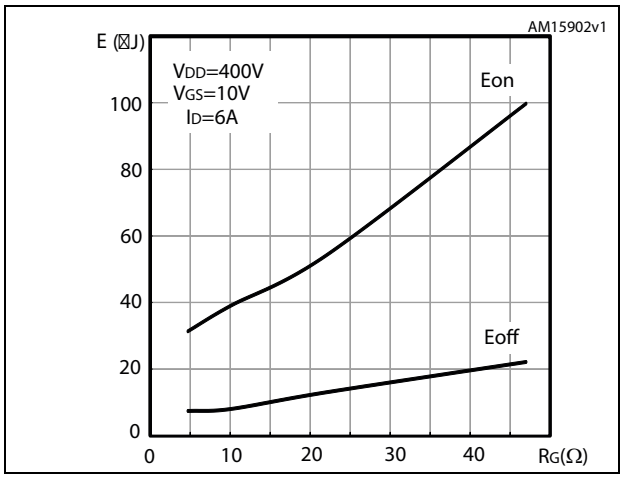


Figure 14. Switching losses vs gate resistance (1)



1. Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 15. Switching times test circuit for resistive load

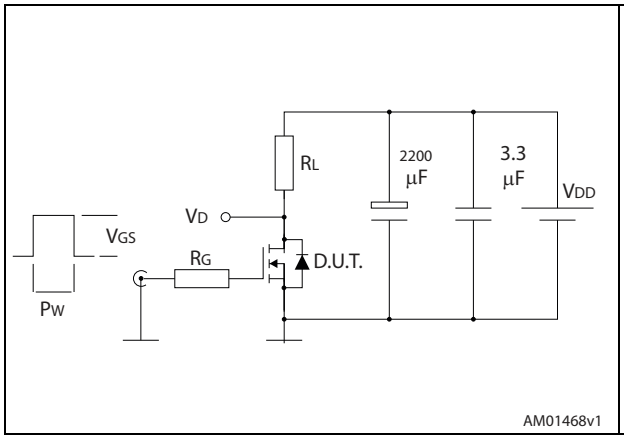


Figure 16. Gate charge test circuit

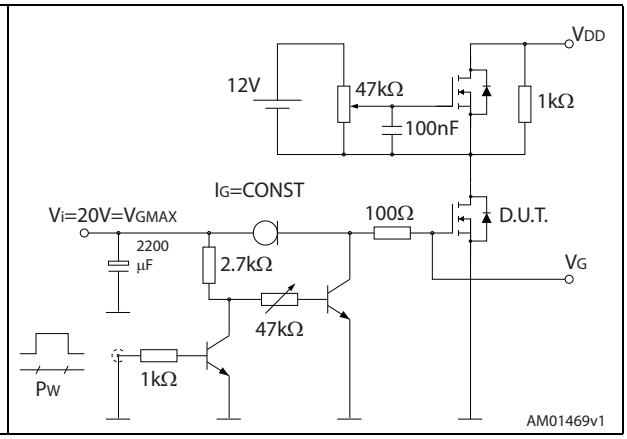


Figure 17. Test circuit for inductive load switching and diode recovery times

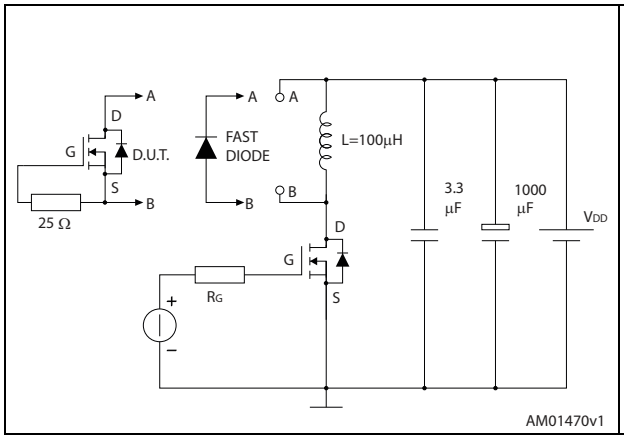


Figure 18. Unclamped inductive load test circuit

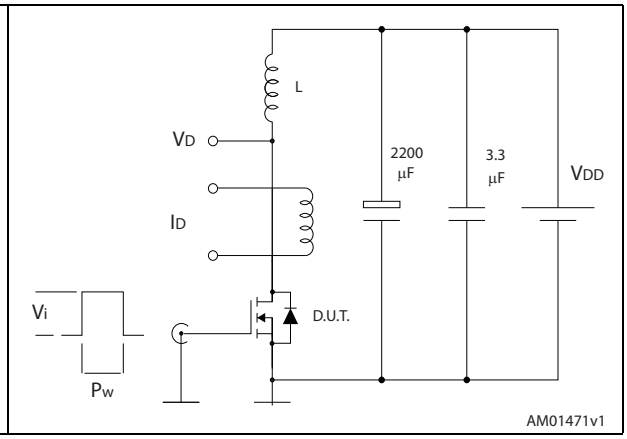


Figure 19. Unclamped inductive waveform

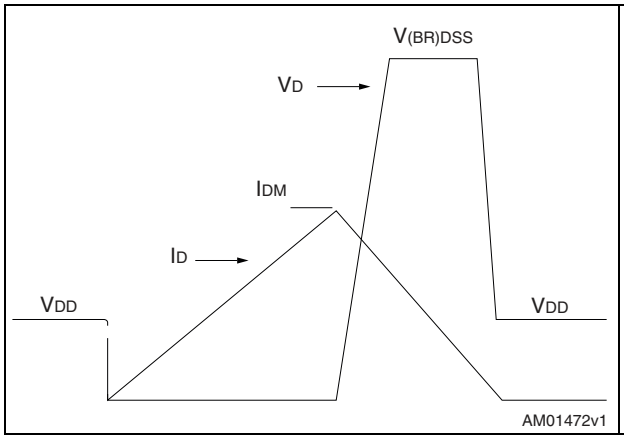
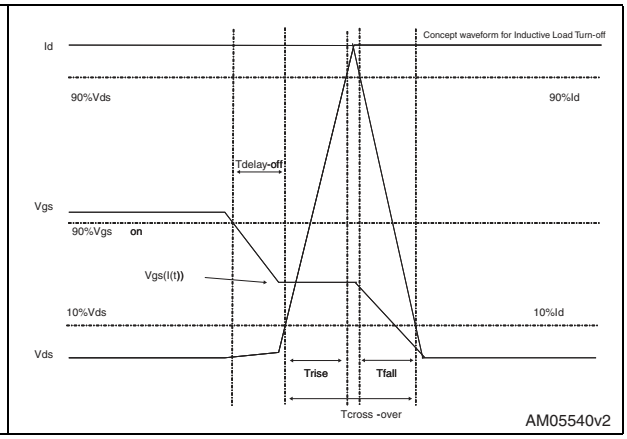


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 21. PowerFLAT™ 5x5 type S mechanical drawing

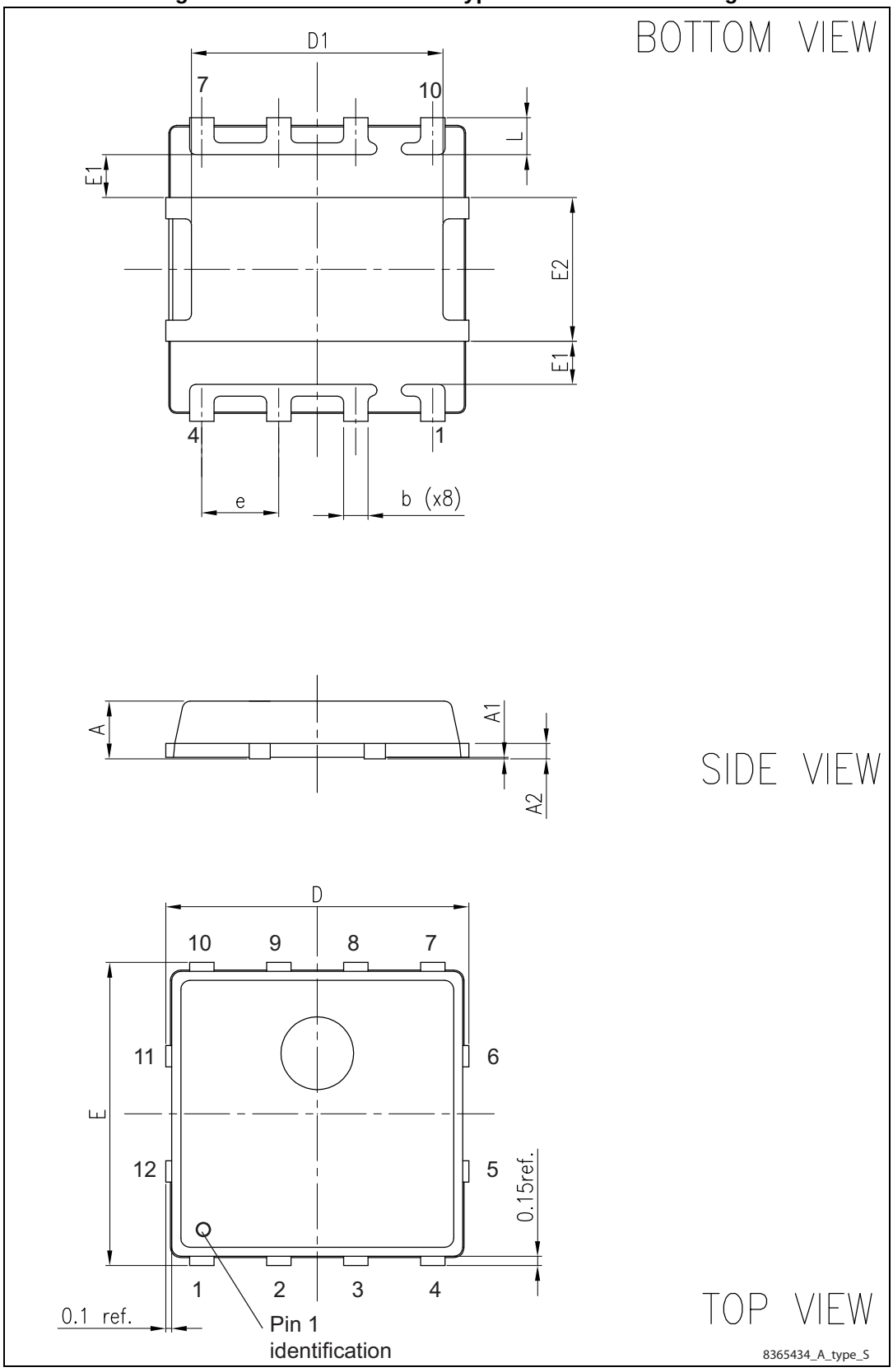
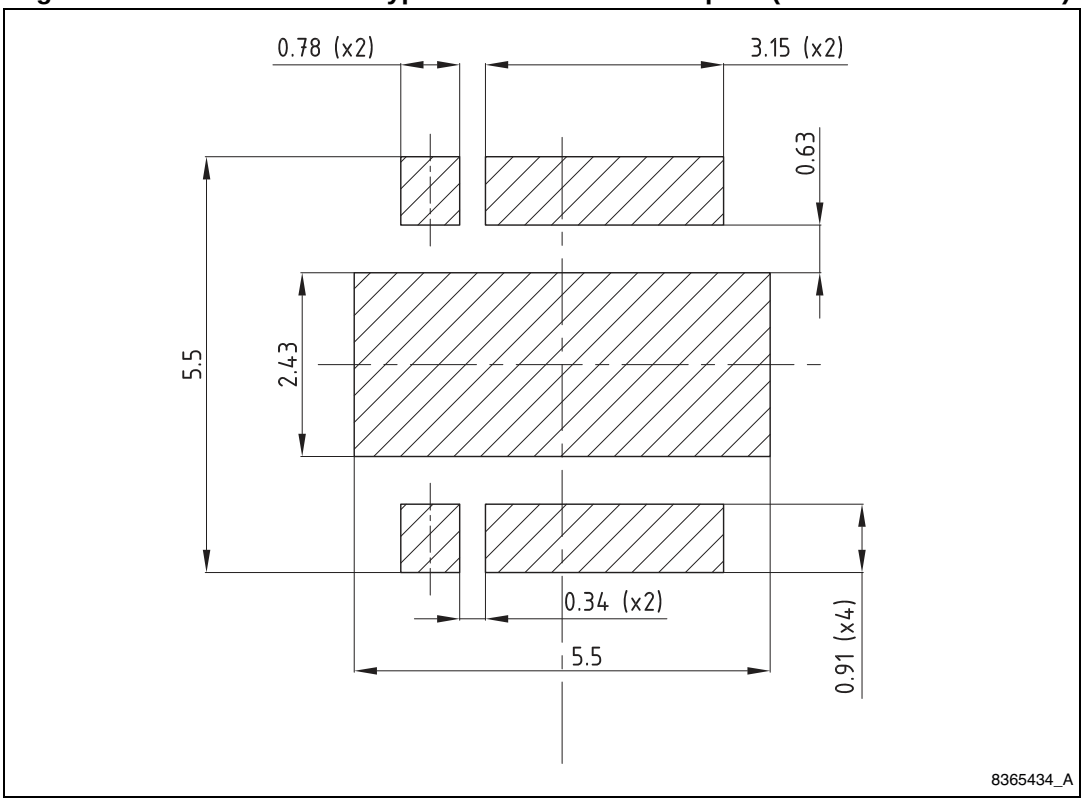


Table 8. PowerFLAT™ 5x5 type S mechanical dimensions

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.0
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.00	
D1	4.05		4.25
E		5.00	
E1	0.64		0.79
E2	2.25		2.45
e		1.27	
L	0.45		0.75

Figure 22. PowerFLAT™ 5x5 type S recommended footprint (dimensions are in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
09-May-2014	1	First release
29-Sep-2014	2	Updated title, features and description in cover page. Document status promoted from preliminary to production data.

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