National Semiconductor

January 2005

LM4906 Boomer® Audio Power Amplifier Series

1W, Bypass-Capacitor-less Audio Amplifier with Internal Selectable Gain

General Description

The LM4906 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1W of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a +5V power supply.

The LM4906 is the first National Semiconductor Boomer Power Amplifier that does not require an external PSRR bypass capacitor. The LM4906 also has an internal selectable gain of either 6dB or 12dB. In addition, no output coupling capacitors or bootstrap capacitors are required which makes the LM4906 ideally suited for cell phone and other low voltage portable applications.

The LM4906 contains advanced pop and click circuitry that eliminates noise, which would otherwise occur during turn-on and turn-off transitions.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4906 features a low -power consumption shutdown mode (the part is enabled by pulling the SD pin high). Additionally, the LM4906 features an internal thermal shutdown protection mechanism.

Key Specifications

- Improved PSRR at 217Hz for +3V — 71dB
- Power Output at +5V, THD+N = 1%, 8Ω — 1.0W (typ)
- Power Output at +3V, THD+N = 1%, 8Ω — 390mW (typ)
- Total shutdown power supply current — 0.1µA (typ)

Features

- Selectable gain of 6dB (2V/V) or 12dB (4V/V)
- No output or PSRR bypass capacitors required
- Improved “Click and Pop” suppression circuitry
- Very fast turn on time: 5ms (typ)
- Minimum external components
- 2.6 - 5.5V operation
- BTL output can drive capacitive loads
- Ultra low current shutdown mode (SD Low)

Applications

- Portable computers
- Desktop computers
- Multimedia monitors

Typical Application

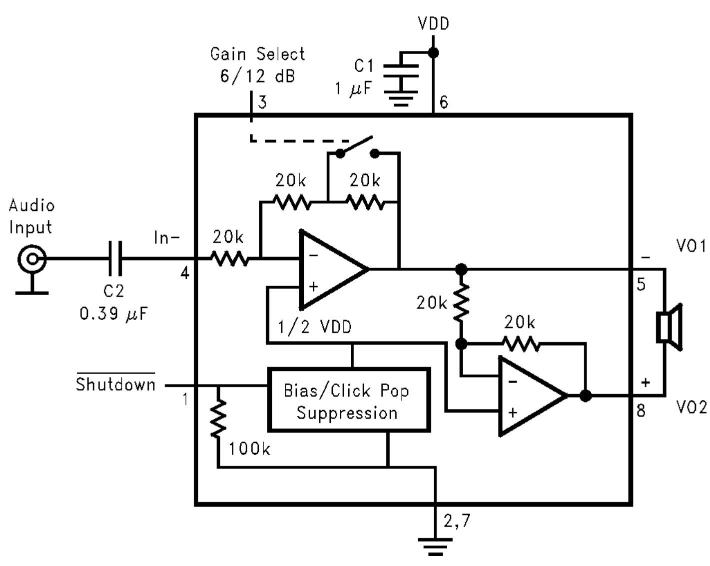

FIGURE 1. Typical Audio Amplifier Application Circuit

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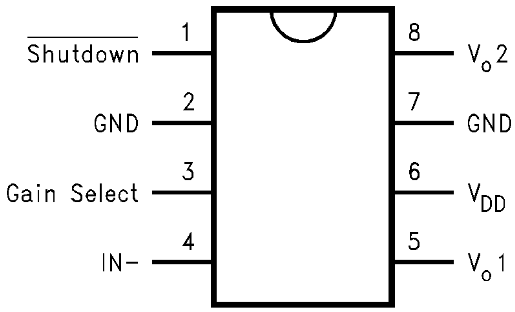
Connection Diagrams

MSOP Package



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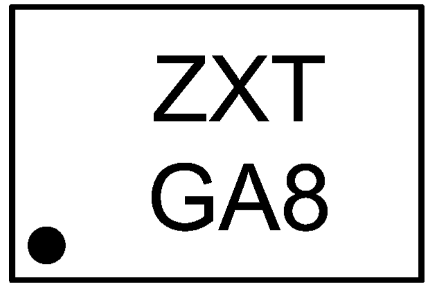
Top View
Order Number LM4906MM
See NS Package Number MUB08A

MSOP Marking



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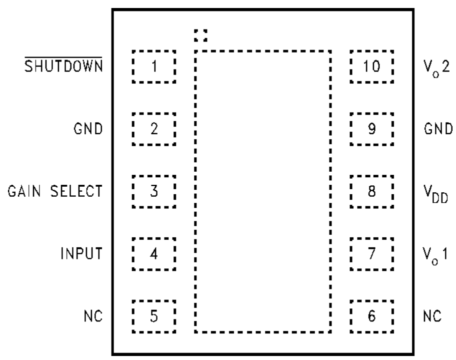
Z - Plant Code
X - Date Code
T - Die Traceability

LLP Package



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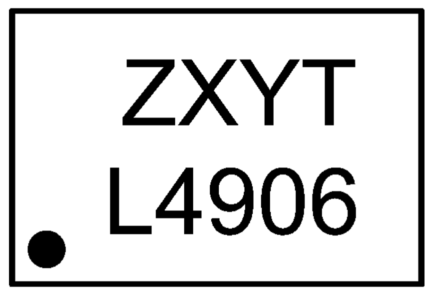
Top View
Order Number LM4906LD
See NS Package Number LDA10B

LD Marking



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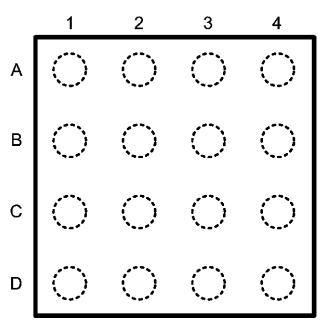
Z - Plant Code
XY - Date Code
T - Die Traceability

µArray LLP Package



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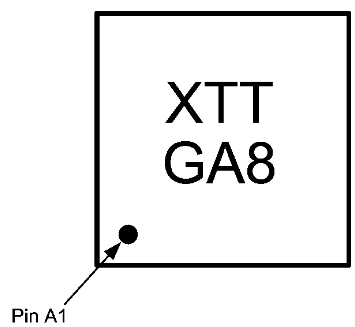
Top View (Bump_side down)
Order Number LM4906GR
See NS Package Number GRA16A

GR Marking



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X - Date Code
TT - Die Traceability

LM4906GR Pin Designation

Pin (Bump) Number	Pin Function
A1	Shutdown
A2	No Connect
A3	V_O2
A4	No Connect
B1	GND
B2	No Connect
B3	GND
B4	GND
C1	Gain Select
C2	IN
C3	No Connect
C4	V_{DD}
D1	No Connect
D2	No Connect
D3	V_O1
D4	V_{DD}

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 10)	6.0V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Notes 3, 11)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150˚C
Thermal Resistance	
θ_{JC} (MSOP)	56˚C/W
θ_{JA} (MSOP)	190˚C/W
θ_{JC} (LLP)	12˚C/W
θ_{JA} (LLP)	63˚C/W
θ_{JA} (GRA)	TBD˚C/W
θ_{JC} (GRA)	TBD˚C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40˚C \le T_A \le 85˚C$
Supply Voltage	$2.6V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 5V (Notes 1, 2)

The following specifications apply for the circuit shown in *Figure 1*, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4906		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	3.5	7	mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	4	8	mA (max)
I_{SD}	Shutdown Current	V_{SD} = GND	0.1	2	µA (max)
V_{OS}	Output Offset Voltage		7	35	mV (max)
P_o	Output Power	THD+N = 1% (max); f = 1 kHz R_L = 8Ω	1.0	0.9	W (min)
T_{WU}	Wake-up time		5		ms
THD+N	Total Harmonic Distortion+Noise	P_o = 0.4 Wrms; f = 1kHz	0.2		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω Gain at 6dB	67 (f = 217Hz) 70 (f = 1kHz)		dB
V_{SDIH}	Shutdown Voltage Input High	SD Pin High = Part On	1.5		V (min)
V_{SDIL}	Shutdown Voltage Input Low	SD Pin Low = Part Off	1.3		V (max)

Electrical Characteristics V_{DD} = 3V (Notes 1, 2)

The following specifications apply for the circuit shown in *Figure 1*, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4906		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	2.6	6	mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	3	7	mA (max)
I_{SD}	Shutdown Current	V_{SD} = GND	0.1	2	µA (max)
V_{OS}	Output Offset Voltage		7	35	mV (max)
P_o	Output Power	THD+N = 1% (max); f = 1 kHz R_L = 8Ω	390		mW
T_{WU}	Wake-up time		4		ms
THD+N	Total Harmonic Distortion+Noise	P_o = 0.15 Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω Gain at 6dB	71 (f = 217Hz) 73 (f = 1kHz)		dB
V_{SDIH}	Shutdown Voltage Input High	SD Pin High = Part On	1.1		V (min)
V_{SDIL}	Shutdown Voltage Input Low	SD Pin Low = Part Off	0.9		V (max)

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given; however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}-T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4906, see power derating curves for additional information.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF–240pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: R_{OUT} is measured from the output pin to ground. This value represents the parallel combination of the 10kΩ output resistors and the two 20kΩ resistors.

Note 10: If the product is in Shutdown mode and V_{DD} exceeds 6V (to a max of 8V V_{DD}), then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10mA, then the device will be protected. If the device is enabled when V_{DD} is greater than 5.5V and less than 6.5V, no damage will occur, although operation life will be reduced. Operation above 6.5V with no current limit will result in permanent damage.

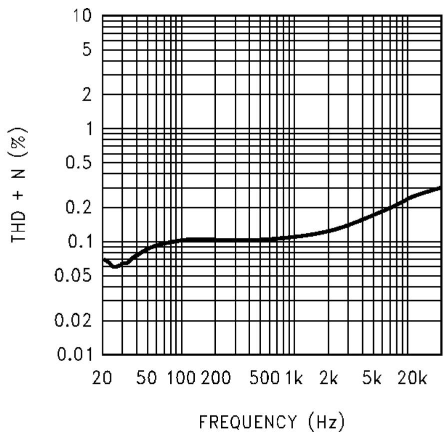
Note 11: Maximum power dissipation in the device (P_{DMAX}) occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation 1 shown in the **Application Information** section. It may also be obtained from the power dissipation graphs.

External Components Description

Components		Functional Description
1.	C_2	Input coupling capacitor which blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at $f_c = 1 / (2\pi R_i C_i)$. Refer to the section, **Proper Selection of External Components**, for an explanation of how to determine the value of C_i.
2.	C_1	Supply bypass capacitor which provides power supply filtering. Refer to the **Power Supply Bypassing** section for information concerning proper placement and selection of the supply bypass capacitor.

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω,
f = 1kHz, PWR = 500mW



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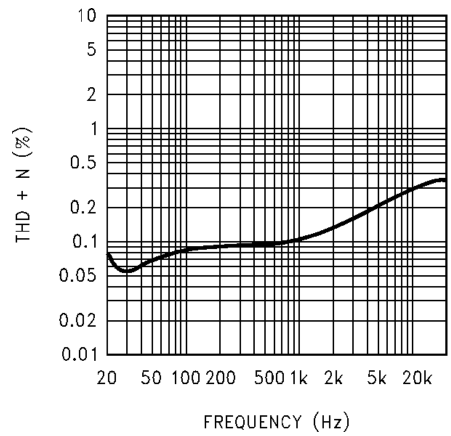
THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω,
f = 1kHz, PWR = 250mW



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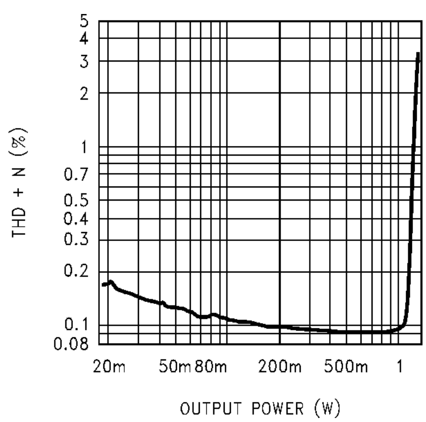
THD+N vs Power Out
V_{DD} = 5V, R_L = 8Ω, f = 1kHz



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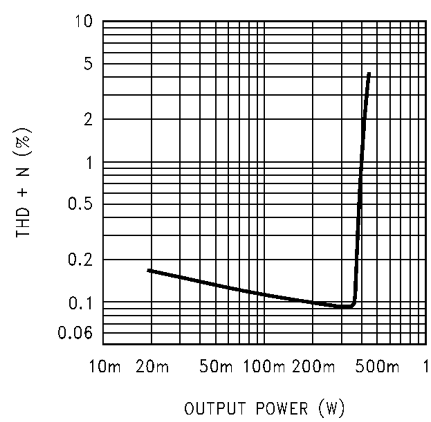
THD+N vs Power Out
V_{DD} = 3V, R_L = 8Ω, f = 1kHz



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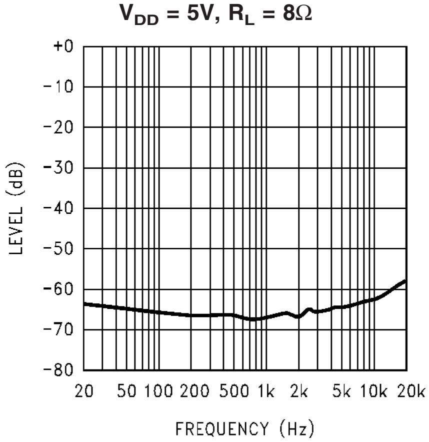
Power Supply Rejection Ratio
vs Frequency
V_{DD} = 5V, R_L = 8Ω



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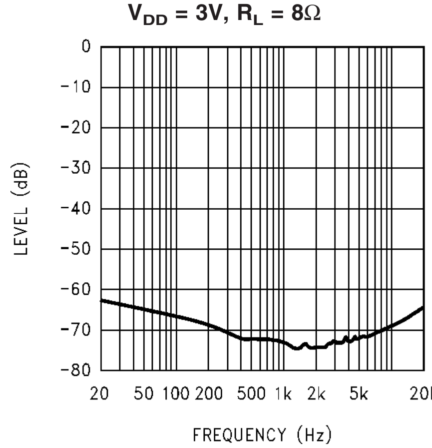
Power Supply Rejection Ratio
vs Frequency
V_{DD} = 3V, R_L = 8Ω



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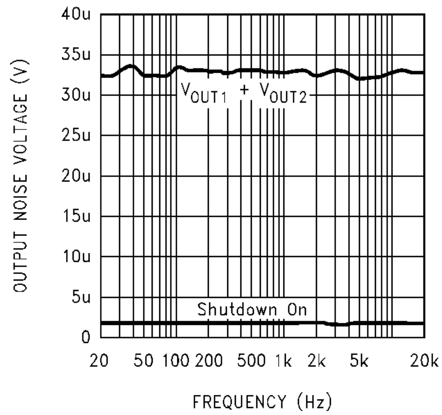
Typical Performance Characteristics (Continued)

Noise Floor
V_{DD} = 5V, R_L = 8Ω
80kHz Bandwith, Input to GND



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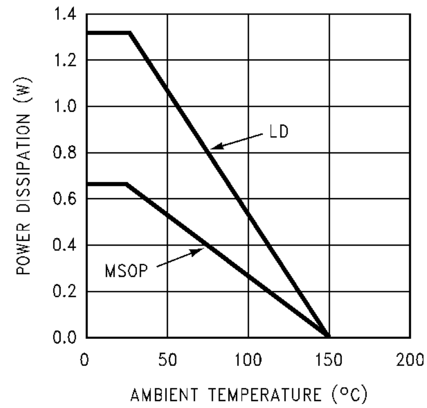
Power Derating Curve



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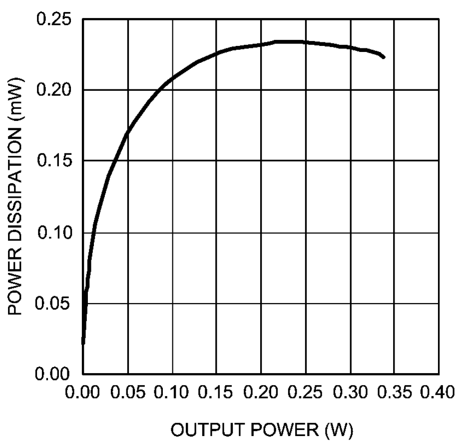
Power Dissipation
vs Output Power, V_{DD} = 3V, R_L = 8Ω



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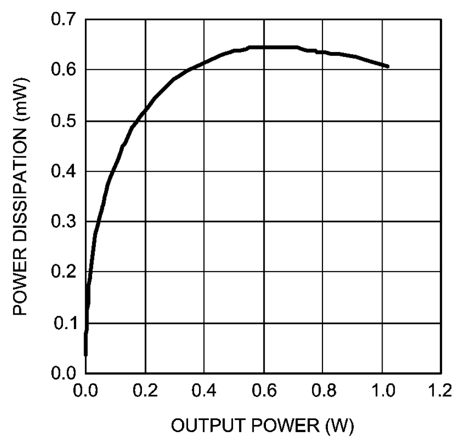
Power Dissipation
vs Output Power, V_{DD} = 5V, R_L = 8Ω



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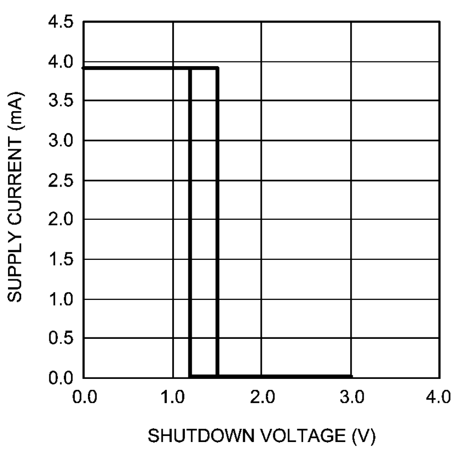
Shutdown Hysteresis Voltage
V_{DD} = 5V, SD Mode = V_{DD} (High)



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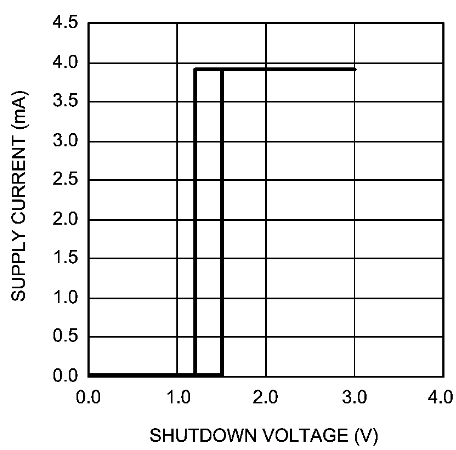
Shutdown Hysteresis Voltage
V_{DD} = 5V, SD Mode = V_{DD} (Low)



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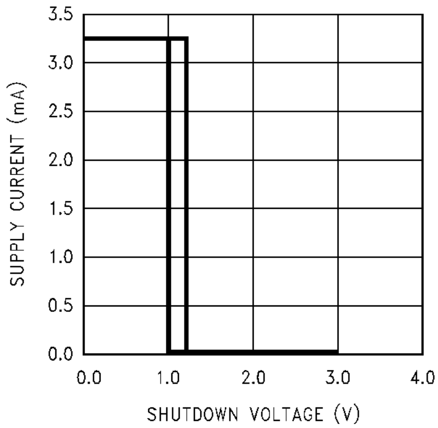
Typical Performance Characteristics (Continued)

Shutdown Hysteresis Voltage
V_{DD} = 3V, SD Mode = V_{DD} (High)



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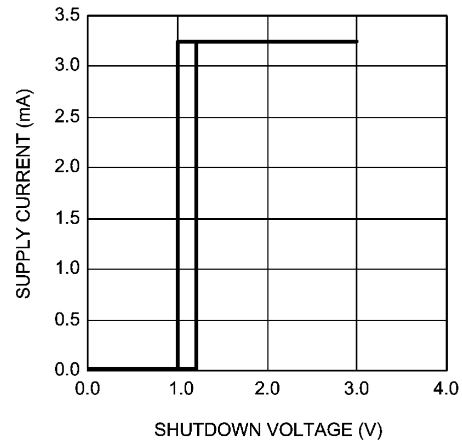
Shutdown Hysteresis Voltage
V_{DD} = 3V, SD Mode = GND (Low)



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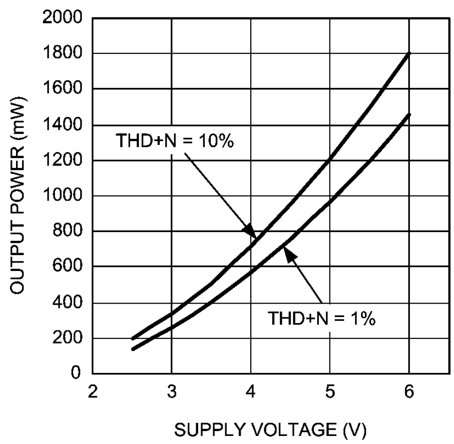
Output Power
vs Supply Voltage, R_L = 8Ω



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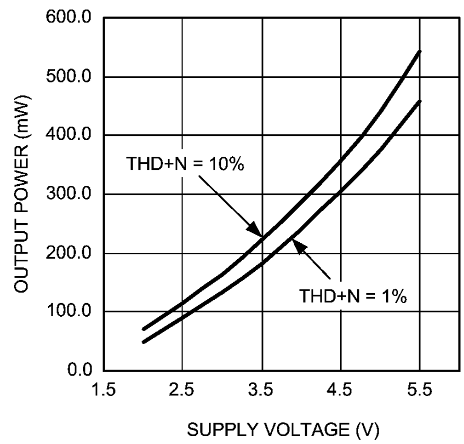
Output Power
vs Supply Voltage, R_L = 32Ω



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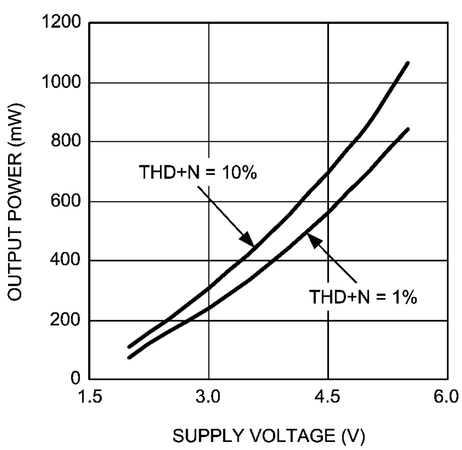
Output Power
vs Supply Voltage, R_L = 16Ω



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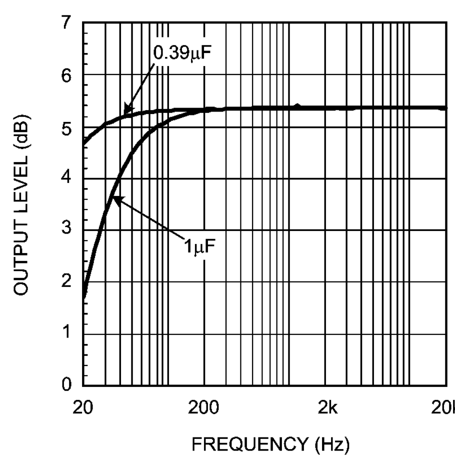
Frequency Response
vs Input Capacitor Size



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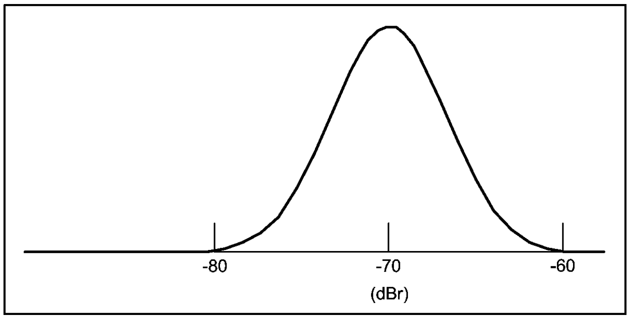
Typical Performance Characteristics (Continued)

PSRR Distribution
V_{DD} = 5V, f = 1kHz, R_L = 8Ω



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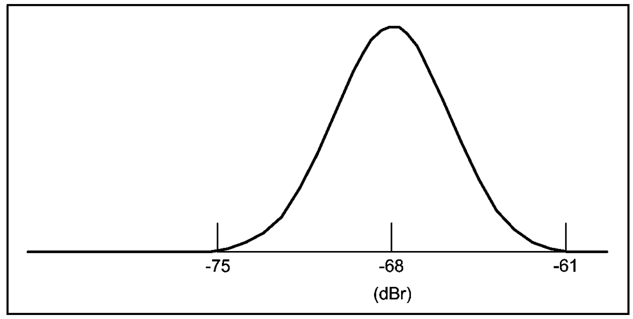
PSRR Distribution
V_{DD} = 5V, f = 217Hz, R_L = 8Ω



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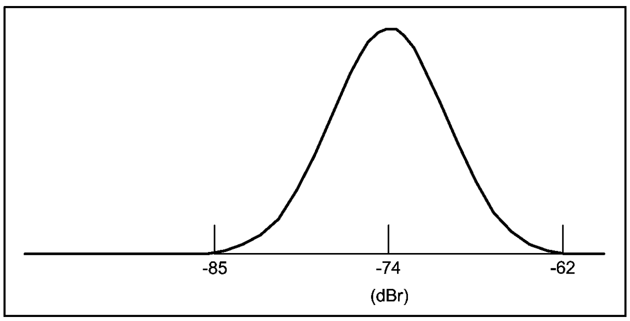
PSRR Distribution
V_{DD} = 3V, f = 1kHz, R_L = 8Ω



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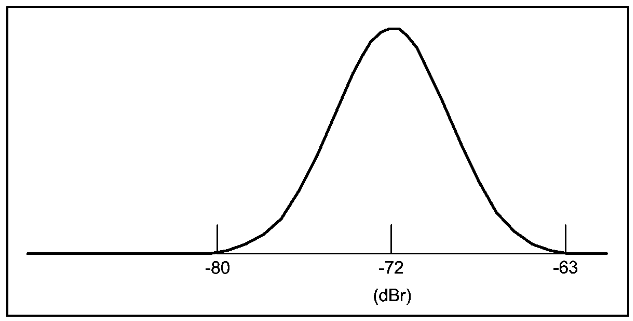
PSRR Distribution
V_{DD} = 3V, f = 217Hz, R_L = 8Ω



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Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 2*, the LM4906 has two internal operational amplifiers. The first amplifier's gain is either 6dB or 12dB depending on the gain select input (Low = 6dB, High = 12dB). The second amplifier's gain is fixed by the two internal 20kΩ resistors. *Figure 2* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180˚. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (20k / 20k) \text{ or } 2 * (40k / 20k)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in LM4906, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4906 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

It is critical that the maximum junction temperature T_{JMAX} of 150˚C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding copper foil, the thermal resistance of the application can be reduced from the free air value of θ_{JA}, resulting in higher P_{DMAX} values without thermal shutdown protection circuitry being activated. Additional copper foil can be added to any of the leads connected to the LM4906. It is especially effective when connected to V_{DD}, GND, and the output pins. Refer to the application information on the LM4906 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150˚C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on the power supply pin should be as close to the device as possible. Typical applications employ a 5V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4906.

TURNING ON THE LM4906

The power supply must first be applied before the application of an input signal to the device and the ramp time to V_{DD} must be less than 4ms, otherwise the wake-up time of the device will be affected. After applying V_{DD}, the LM4906 will turn-on after an initial minimum threshold input signal of $7mV_{RMS}$, resulting in a generated output differential signal. An input signal of less than $7mV_{RMS}$ will result in a negligible output voltage. Once the device is turned on, the input signal can go below the $7mV_{RMS}$ without shutting the device off. If, however, SHUTDOWN or V_{DD} is cycled, the minimum threshold requirement for the input signal must first be met again, with V_{DD} ramping first.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4906 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. The device is placed into shutdown mode by toggling the Shutdown pin Low/ground. The trigger point for shutdown low is shown as a typical value in the Supply Current vs Shutdown Voltage graphs in the **Typical Performance Characteristics** section. It is best to switch between ground and supply for maximum performance. While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.1µA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor (or pull-down, depending on shutdown high or low application). This scheme guarantees that the shutdown pin will not float, thus preventing unwanted state changes.

SELECTION OF INPUT CAPACITOR SIZE

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor,

Application Information (Continued)

C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found.

Extra supply voltage creates headroom that allows the LM4906 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

The gain of the LM4906 is internally set at either 6dB or 12dB.

The final design step is to address the bandwidth requirements which must be stated as a pair of −3dB frequency points. Five times away from a −3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

$$f_L = 100Hz / 5 = 20Hz$$

$$f_H = 20kHz * 5 = 100kHz$$

As stated in the **External Components** section, R_{in} (20k) in conjunction with C_2 create a highpass filter.

$$C_2 \geq 1 / (2\pi * 20k\Omega * 20Hz) = 0.397\mu F; \text{ use } 0.39\mu F$$

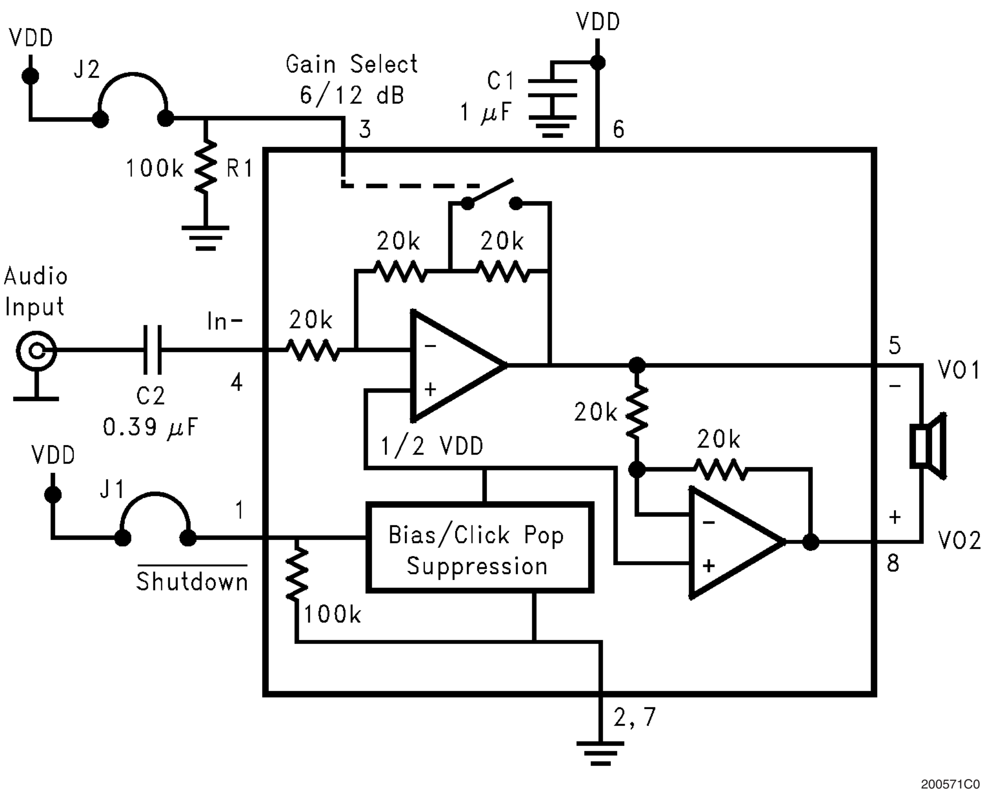
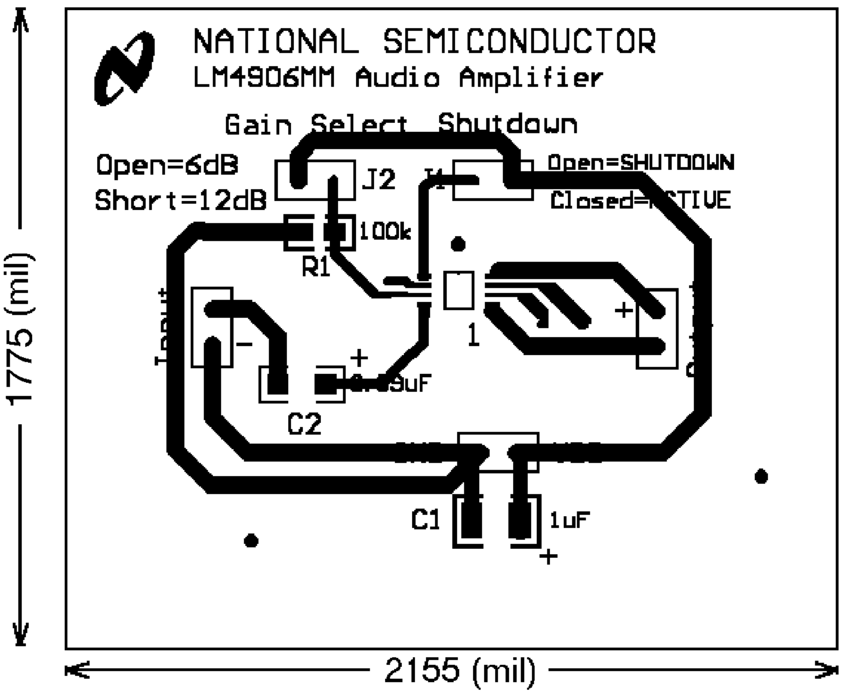


FIGURE 2. REFERENCE DESIGN BOARD SCHEMATIC

Application Information (Continued)

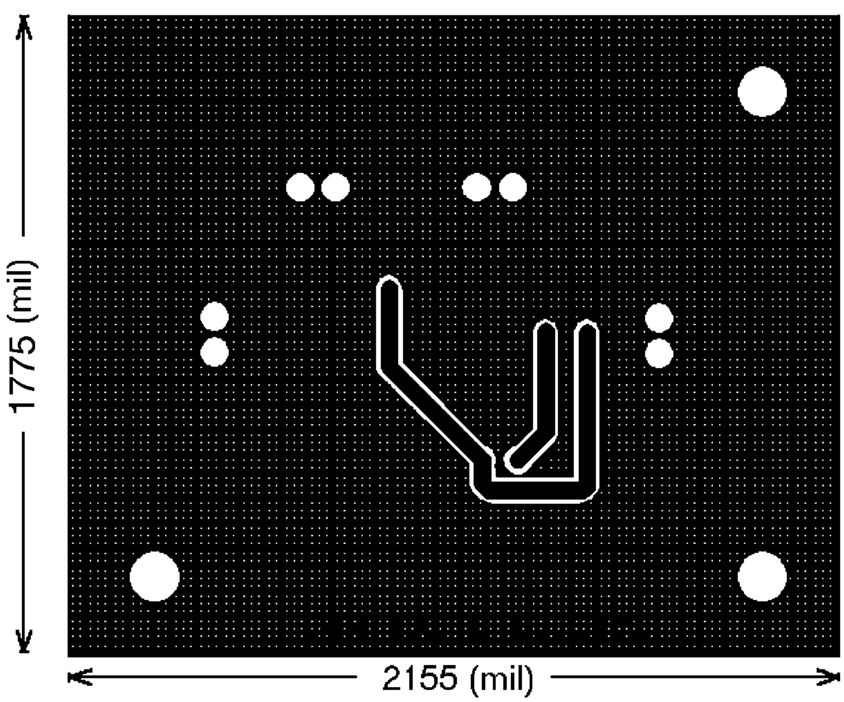
LM4906 MSOP DEMO BOARD ARTWORK

Top Layer



200571E6

Bottom Layer

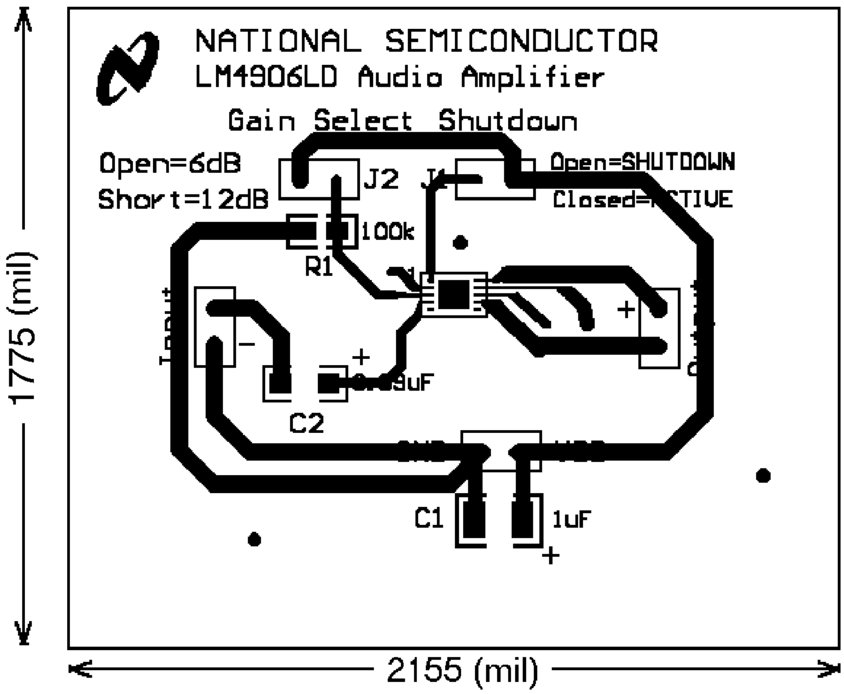


200571E7

Application Information (Continued)

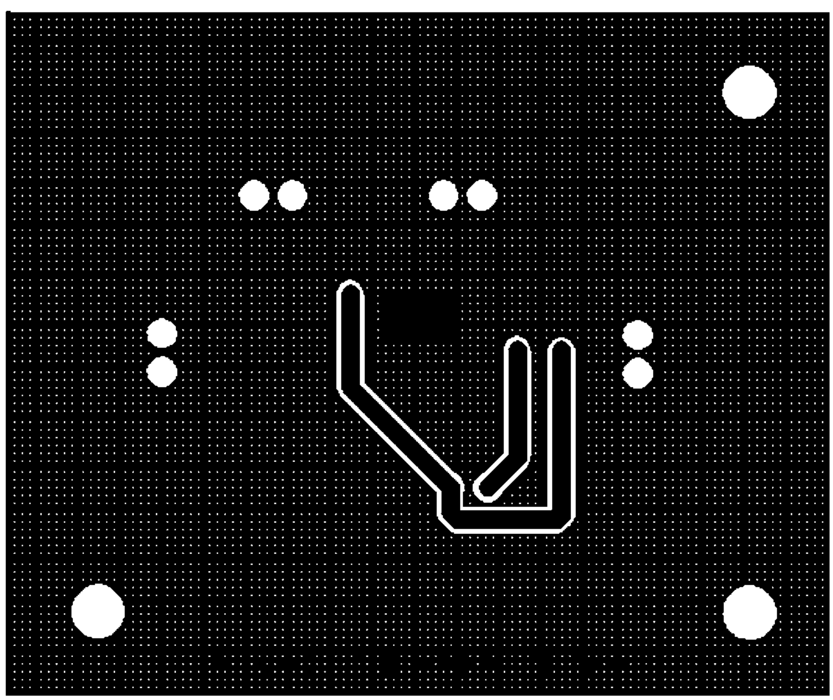
LM4906 LD DEMO BOARD ARTWORK

Top Layer



200571E8

Bottom Layer



200571E9

Application Information (Continued)

Mono LM4906 Reference Design Boards
Bill of Material

Part Description	Quantity	Reference Designator
LM4906 Audio Amplifier	1	U1
Tantalum Capcitor, 1µF	1	C1
Ceramic Capacitor, 0.39µF	1	C2
Jumper Header Vertical Mount 2X1 0.100“ spacing	5	J1, J2, Input, Output, V_{DD}

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

GENERAL MIXED SIGNAL LAYOUT RECOMMENDATION

Power and Ground Circuits

For 2 layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time but will not increase the final price of the board. The only extra parts required will be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing High Frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

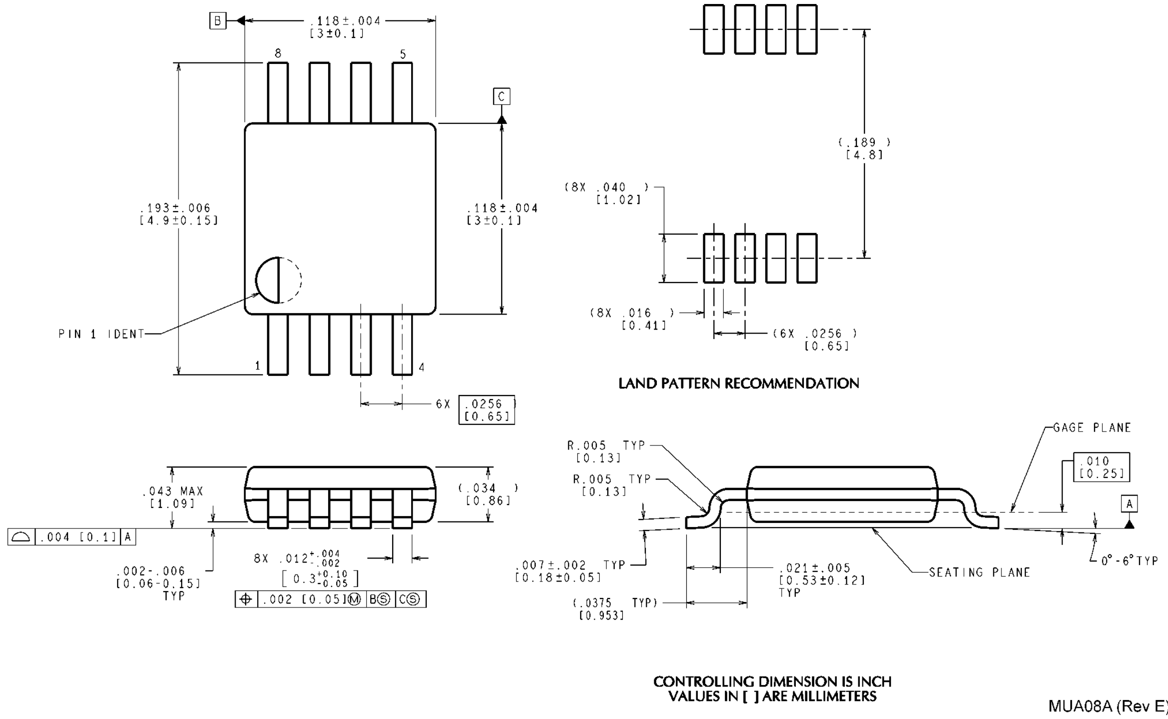
Placement of Digital and Analog Components

All digital components and high-speed digital signal traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

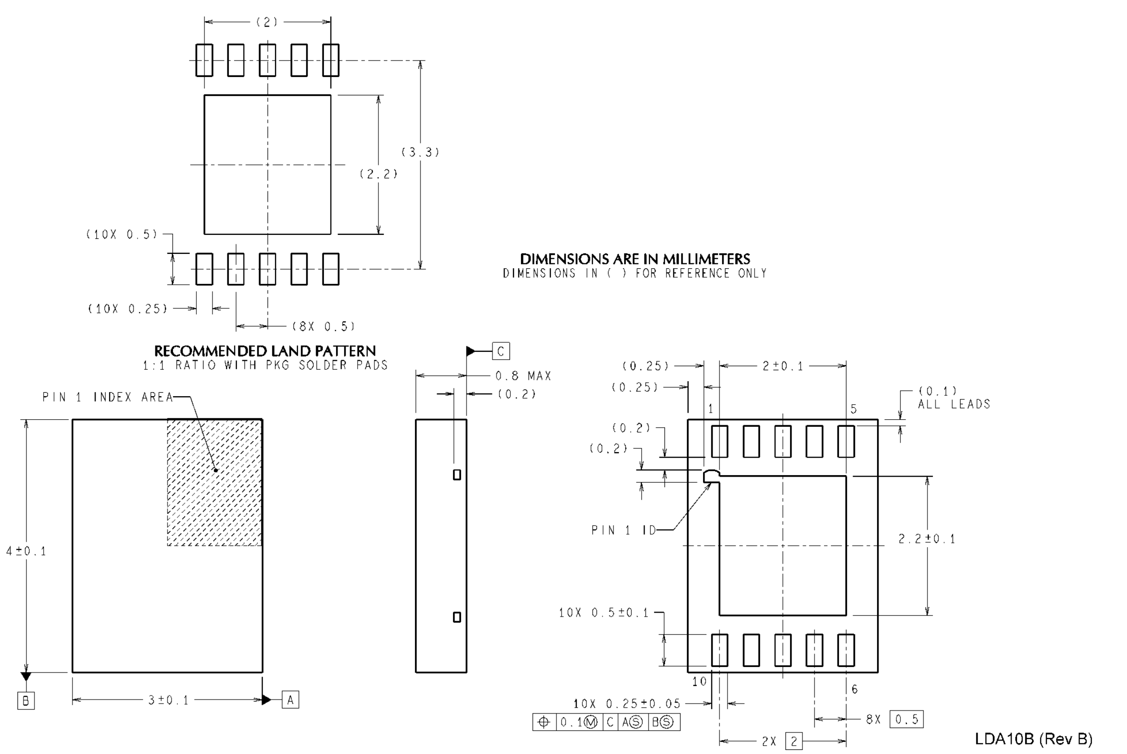
Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Physical Dimensions inches (millimeters) unless otherwise noted



MUA08A (Rev E)

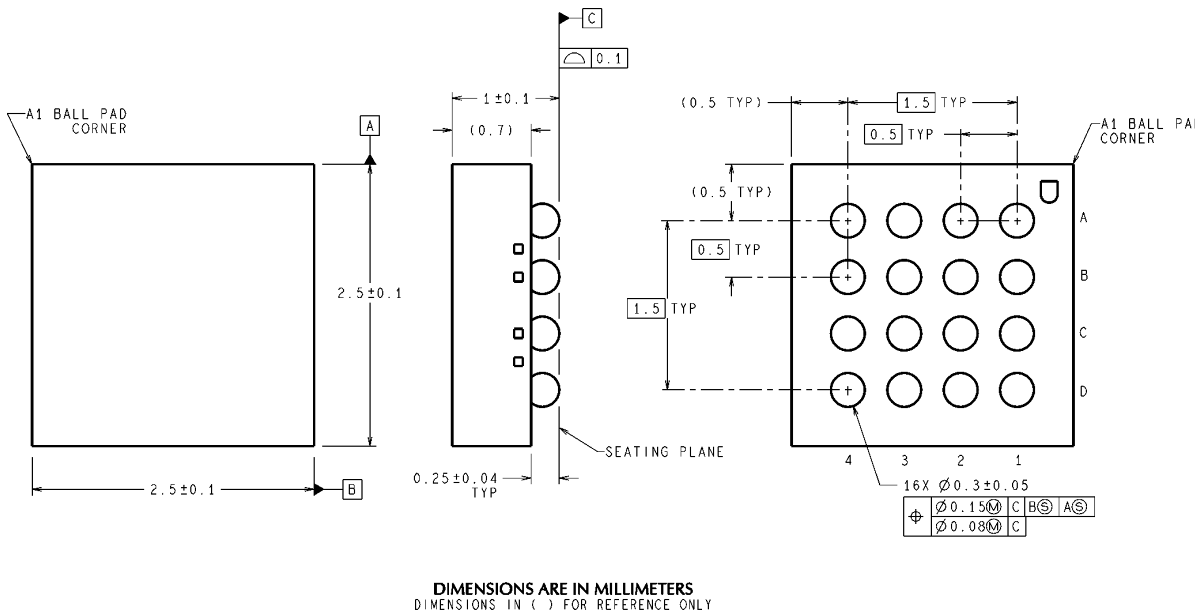
MSOP
Order Number LM4906MM
NS Package Number MUA08A



LDA10B (Rev B)

LLP
Order Number LM4906LD
NS Package Number LDA10B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



GRA16A (Rev A)

micro Array Pkg
Order Number LM4906GR
NS Package Number GRA16A

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