

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 2.7 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 8.5 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- All Outputs Have Equivalent 26- $\Omega$  Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

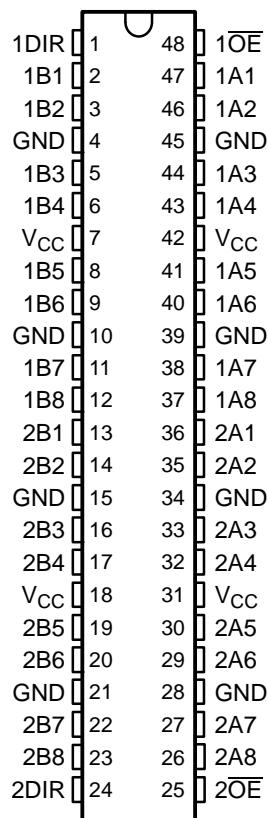
The SN74LVCR162245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses effectively are isolated.

All outputs, which are designed to sink up to 12 mA, include 26- $\Omega$  resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by  $\overline{OE}$  or DIR.

DGG OR DL PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVCR162245DL	LVCR162245
		Tape and reel	SN74LVCR162245DLR	
	TSSOP – DGG	Tape and reel	SN74LVCR162245DGGGR	LVCR162245
	VFBGA – GQL	Tape and reel	SN74LVCR162245KR	LEP245
	VFBGA – ZQL (Pb-free)		74LVCR162245ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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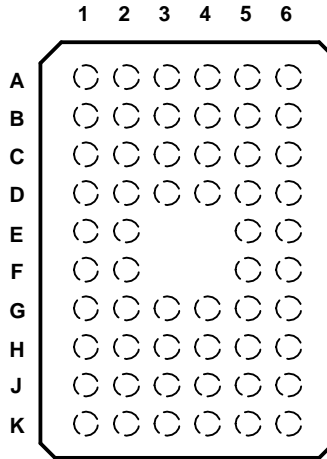
**SN74LVCR162245**  
**16-BIT BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES047E—AUGUST 1995—REVISED MARCH 2005

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**QQL OR ZQL PACKAGE**  
**(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>**

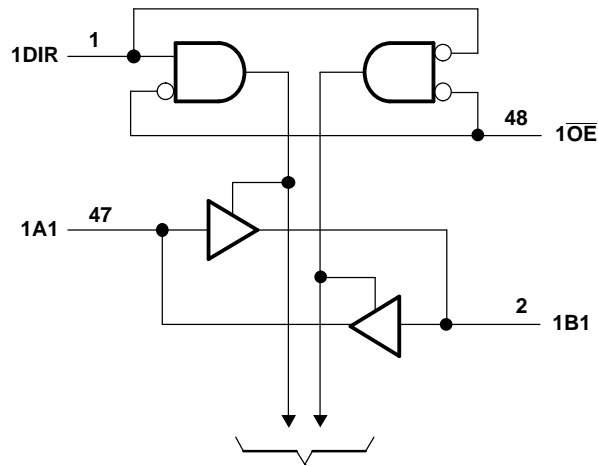
	1	2	3	4	5	6
<b>A</b>	1DIR	NC	NC	NC	NC	$1\overline{OE}$
<b>B</b>	1B2	1B1	GND	GND	1A1	1A2
<b>C</b>	1B4	1B3	$V_{CC}$	$V_{CC}$	1A3	1A4
<b>D</b>	1B6	1B5	GND	GND	1A5	1A6
<b>E</b>	1B8	1B7			1A7	1A8
<b>F</b>	2B1	2B2			2A2	2A1
<b>G</b>	2B3	2B4	GND	GND	2A4	2A3
<b>H</b>	2B5	2B6	$V_{CC}$	$V_{CC}$	2A6	2A5
<b>J</b>	2B7	2B8	GND	GND	2A8	2A7
<b>K</b>	2DIR	NC	NC	NC	NC	$2\overline{OE}$

(1) NC - No internal connection

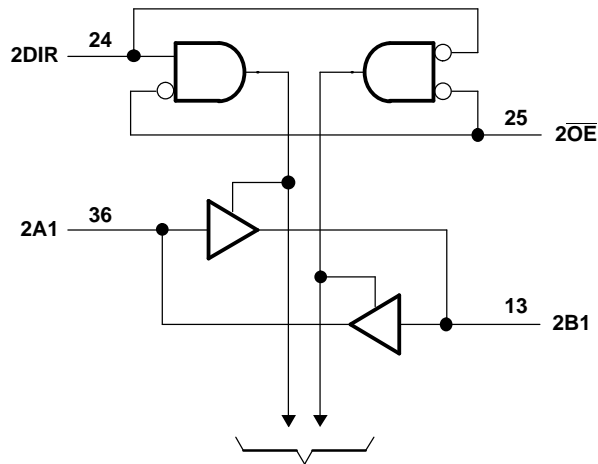
**FUNCTION TABLE**  
**(EACH 8-BIT SECTION)**

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**LOGIC DIAGRAM (POSITIVE LOGIC)**



To Seven Other Channels



Pin numbers shown are for the DGG and DL packages.

# SN74LVCR162245

## 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES047E–AUGUST 1995–REVISED MARCH 2005

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range	Except I/O ports <sup>(2)</sup>	$V_{CC} + 4.6$	V
		I/O ports <sup>(2)(3)</sup>	$V_{CC} + 0.5$	
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$	±50	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$	±50	mA
Continuous current through $V_{CC}$ or GND			±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	70	°C/W
		DL package	63	
		GQL/ZQL package	42	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7$ V to $3.6$ V		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7$ V to $3.6$ V		V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7$ V	-8	mA
		$V_{CC} = 3$ V	-12	
$I_{OL}$	Low-level output current	$V_{CC} = 2.7$ V	8	mA
		$V_{CC} = 3$ V	12	
$\Delta t/\Delta V$	Input transition rise or fall rate	10		ns/V
$T_A$	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at the associated  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>			I <sub>OH</sub> = -100 μA	MIN to MAX	V <sub>CC</sub> - 0.2			V
			I <sub>OH</sub> = -4 mA, V <sub>IH</sub> = 2 V	2.7 V	2.2			
			I <sub>OH</sub> = -8 mA, V <sub>IH</sub> = 2 V		2			
			I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 2 V	3 V	2.4			
			I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2 V		2			
V <sub>OL</sub>			I <sub>OL</sub> = 100 μA	MIN to MAX	0.2			V
			I <sub>OL</sub> = 4 mA, V <sub>IL</sub> = 0.8 V	2.7 V	0.4			
			I <sub>OL</sub> = 8 mA, V <sub>IL</sub> = 0.8 V		0.6			
			I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.8 V	3 V	0.55			
			I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V		0.8			
I <sub>I</sub>			V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5			μA
I <sub>I(hold)</sub>			V <sub>I</sub> = 0.8 V	3 V	75			μA
			V <sub>I</sub> = 2 V		-75			
			V <sub>I</sub> = 0 to 3.6 V	3.6 V	±500			μA
I <sub>OZ</sub> <sup>(3)</sup>			V <sub>O</sub> = 0 V or (V <sub>CC</sub> to 5.5 V)	3.6 V	±10			μA
I <sub>CC</sub>			V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	20			μA
			3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(4)</sup>		20			
ΔI <sub>CC</sub>			One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500			μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V	2.5			pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V	3.5			pF

(1) For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

(2) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(3) For the total leakage current in an I/O port, please consult the I<sub>I(hold)</sub> specification for the input voltage condition 0 V < V<sub>I</sub> < V<sub>CC</sub>, and the I<sub>OZ</sub> specification for the input voltage conditions V<sub>I</sub> = 0 V or V<sub>I</sub> = V<sub>CC</sub> to 5.5 V. The bus-hold current, at input voltage greater than V<sub>CC</sub>, is negligible.

(4) This applies in the disabled state only.

## Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

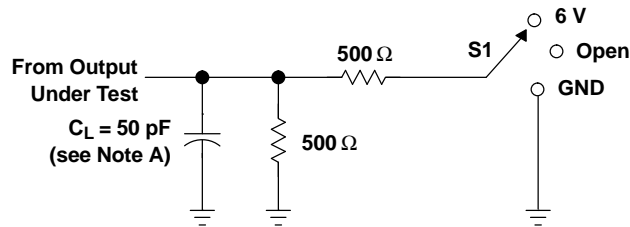
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	1.5	7.5	1.5	8.5	ns
t <sub>en</sub>	$\overline{\text{OE}}$	A or B	1.5	9	1.5	10	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	A or B	1.5	7.5	1.5	8.5	ns

## Operating Characteristics

V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C

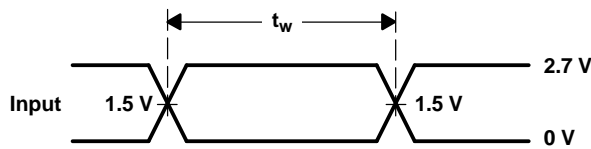
PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	Outputs enabled	20	pF
		Outputs disabled	2	

**PARAMETER MEASUREMENT INFORMATION**

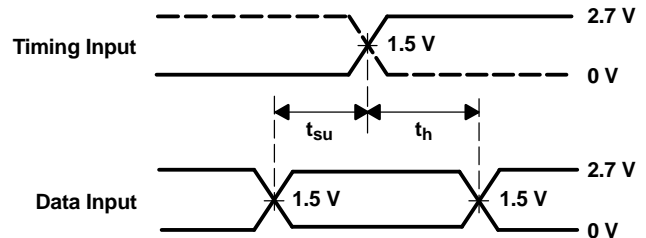


**LOAD CIRCUIT FOR OUTPUTS**

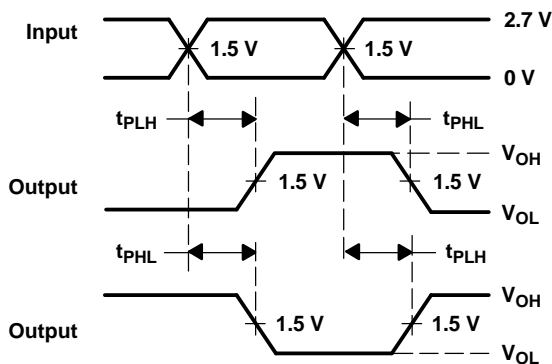
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



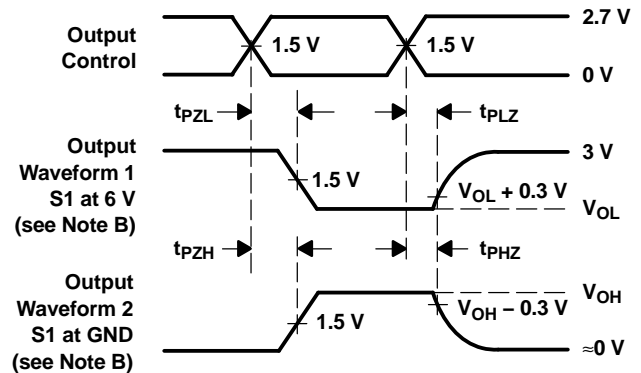
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCR162245DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCR162245	<a href="#">Samples</a>
SN74LVCR162245DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCR162245	<a href="#">Samples</a>
SN74LVCR162245DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCR162245	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCR162245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVCR162245DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

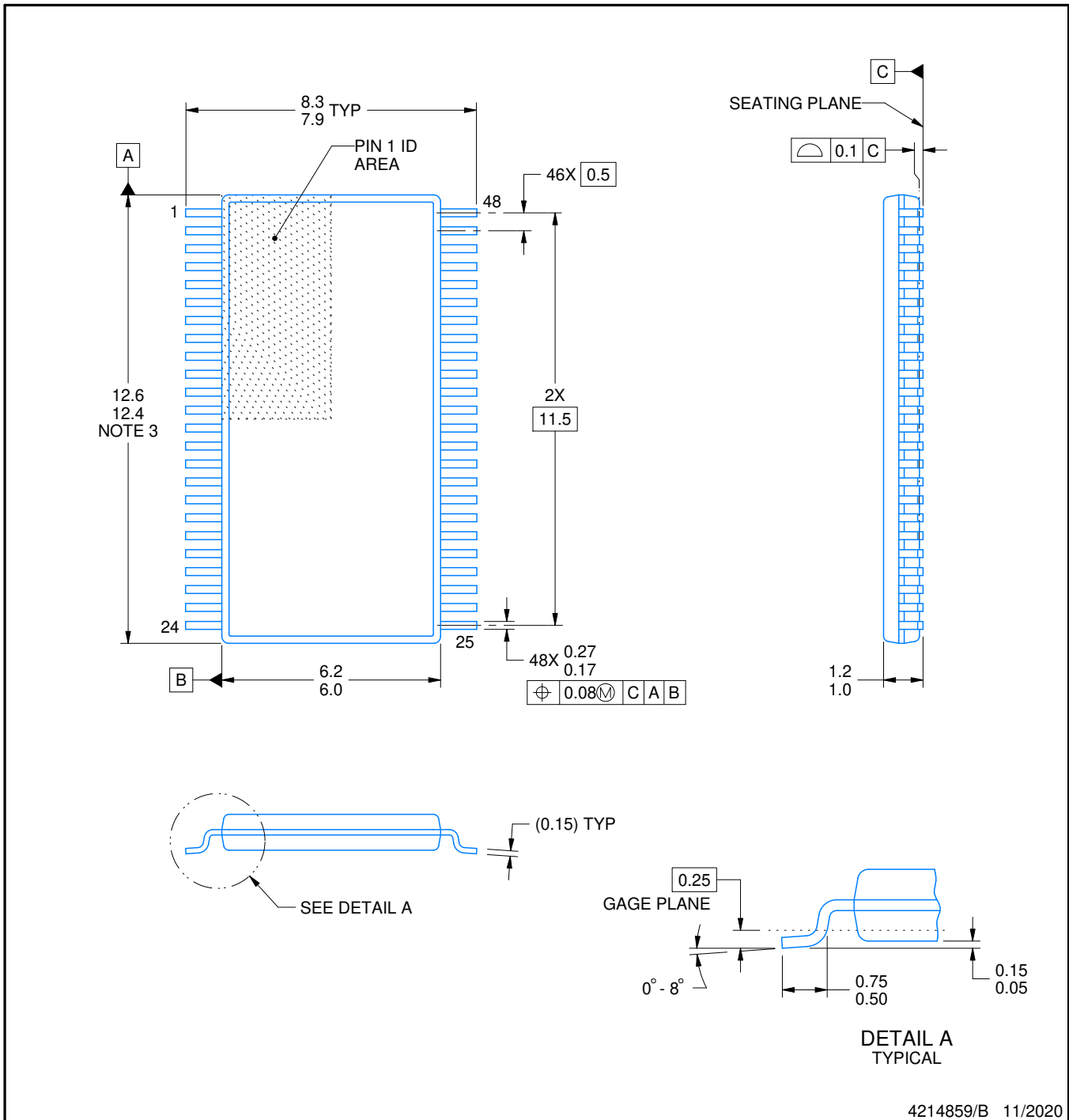

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCR162245DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVCR162245DLR	SSOP	DL	48	1000	367.0	367.0	55.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVCR162245DL	DL	SSOP	48	25	473.7	14.24	5110	7.87



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NOTES:

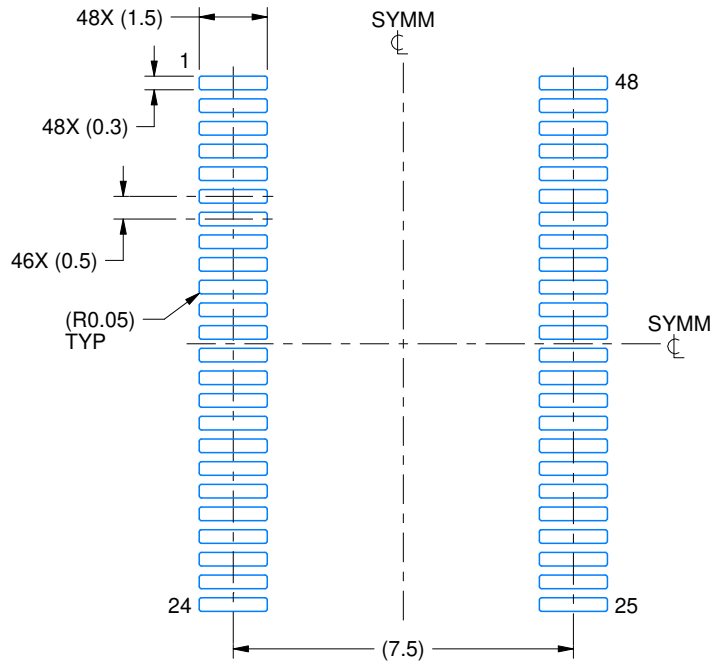
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

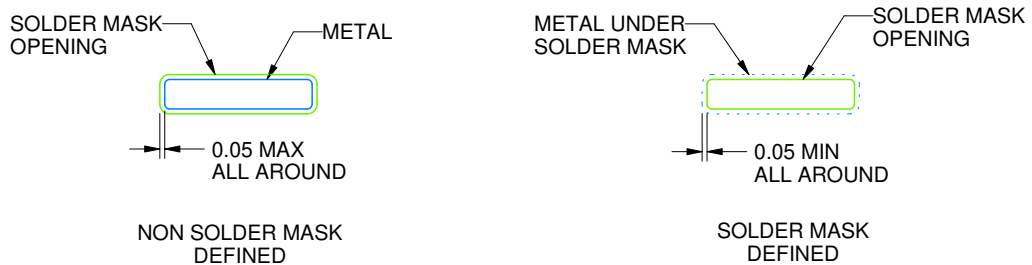
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

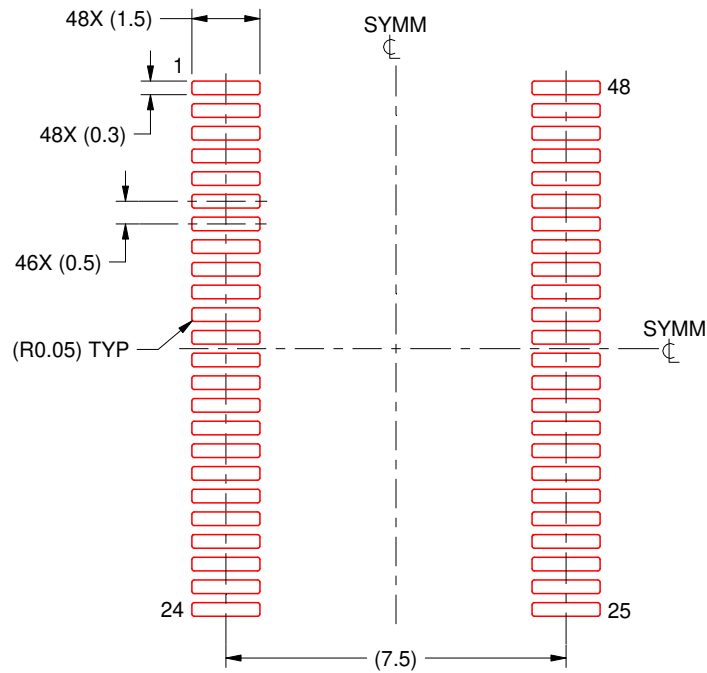
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

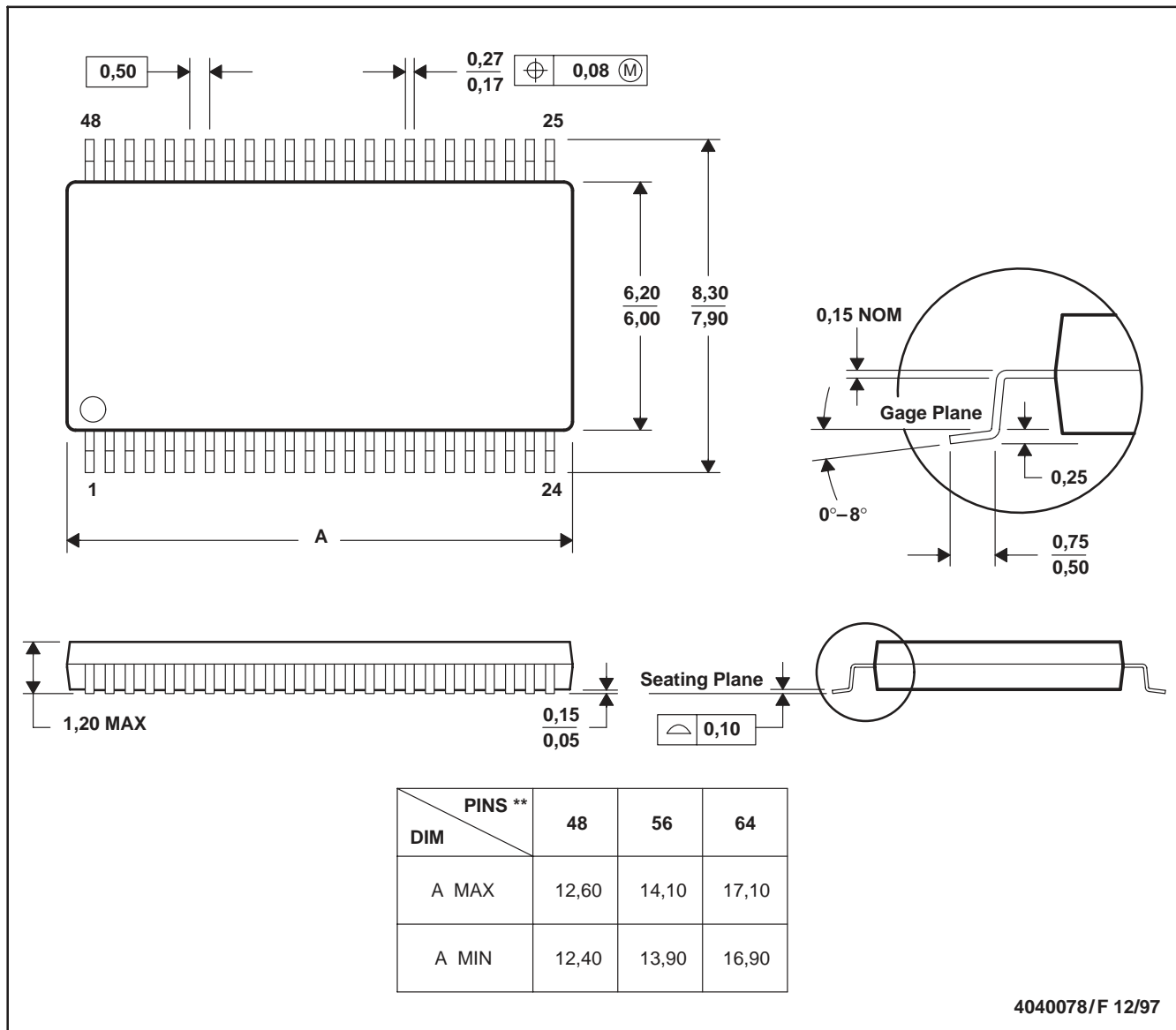
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

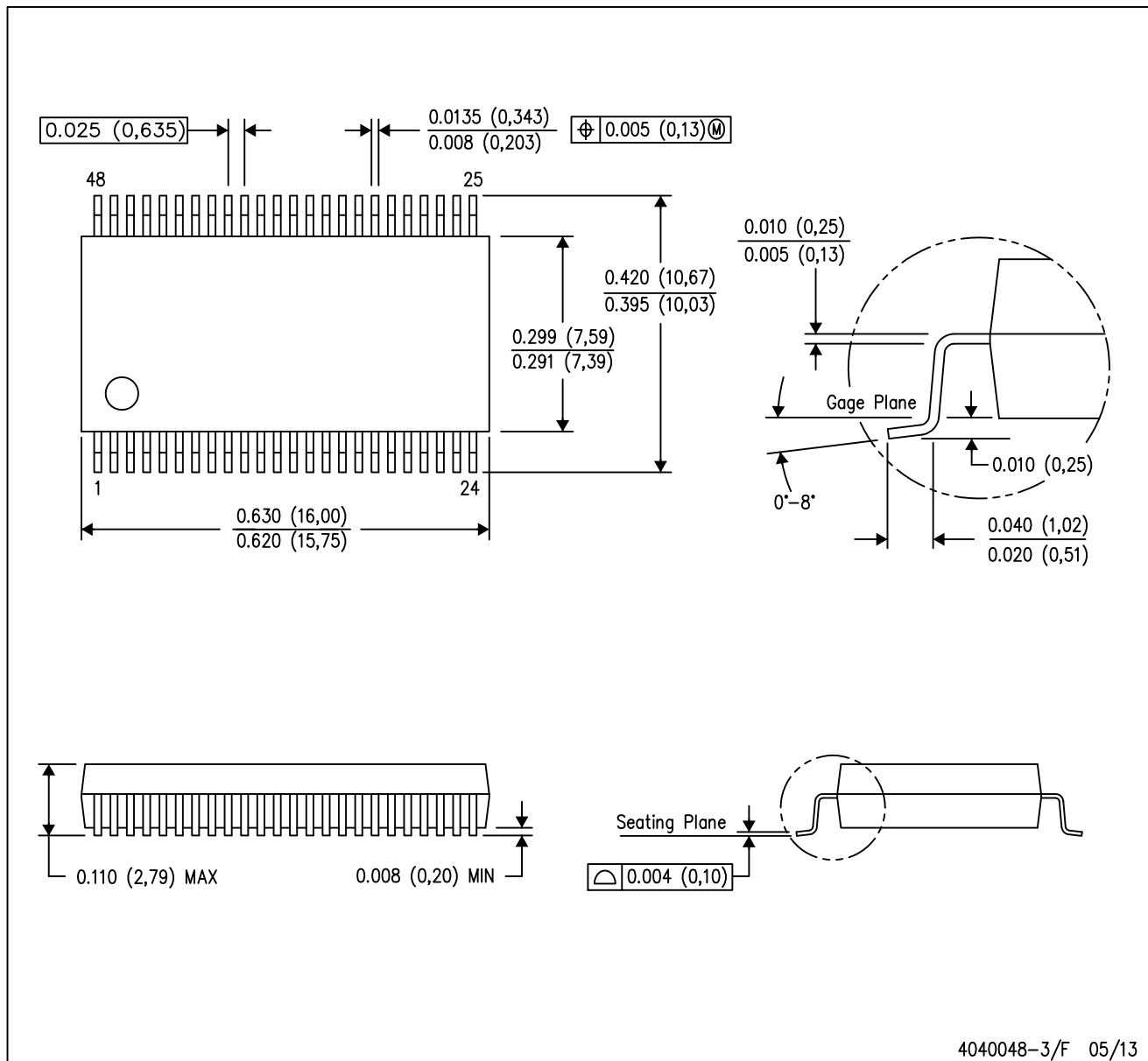


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

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