MMBT6517L, NSVMMBT6517L

High Voltage Transistor

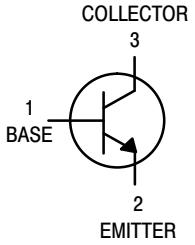
NPN Silicon

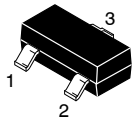
ON Semiconductor®

http://onsemi.com

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant





SOT−23 (TO−236AB)
CASE 318
STYLE 6

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	350	V
Collector −Base Voltage	V_{CBO}	350	V
Emitter − Base Voltage	V_{EBO}	5.0	V
Base Current	I_B	25	mA
Collector Current − Continuous	I_C	100	mA

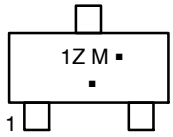
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board (Note 1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

MARKING DIAGRAM



1Z = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBT6517LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
MMBT6517LT3G	SOT−23 (Pb−Free)	10,000 / Tape & Reel
NSVMMBT6517LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage (I_C = 1.0 mA)	$V_{(BR)CEO}$	350	–	V
Collector – Base Breakdown Voltage (I_C = 100 μA)	$V_{(BR)CBO}$	350	–	V
Emitter – Base Breakdown Voltage (I_E = 10 μA)	$V_{(BR)EBO}$	6.0	–	V
Collector Cutoff Current (V_{CB} = 250 V)	I_{CBO}	–	50	nA
Emitter Cutoff Current (V_{EB} = 5.0 V)	I_{EBO}	–	50	nA
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 1.0 mA, V_{CE} = 10 V)		20	–	
(I_C = 10 mA, V_{CE} = 10 V)		30	–	
(I_C = 30 mA, V_{CE} = 10 V)		30	200	
(I_C = 50 mA, V_{CE} = 10 V)		20	200	
(I_C = 100 mA, V_{CE} = 10 V)		15	–	
Collector – Emitter Saturation Voltage (Note 3)	$V_{CE(sat)}$			V
(I_C = 10 mA, I_B = 1.0 mA)		–	0.30	
(I_C = 20 mA, I_B = 2.0 mA)		–	0.35	
(I_C = 30 mA, I_B = 3.0 mA)		–	0.50	
(I_C = 50 mA, I_B = 5.0 mA)		–	1.0	
Base – Emitter Saturation Voltage	$V_{BE(sat)}$			V
(I_C = 10 mA, I_B = 1.0 mA)		–	0.75	
(I_C = 20 mA, I_B = 2.0 mA)		–	0.85	
(I_C = 30 mA, I_B = 3.0 mA)		–	0.90	
Base – Emitter On Voltage (I_C = 100 mA, V_{CE} = 10 V)	$V_{BE(on)}$	–	2.0	V
SMALL– SIGNAL CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 10 mA, V_{CE} = 20 V, f = 20 MHz)	f_T	40	200	MHz
Collector–Base Capacitance (V_{CB} = 20 V, f = 1.0 MHz)	C_{cb}	–	6.0	pF
Emitter–Base Capacitance (V_{EB} = 0.5 V, f = 1.0 MHz)	C_{eb}	–	80	pF

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

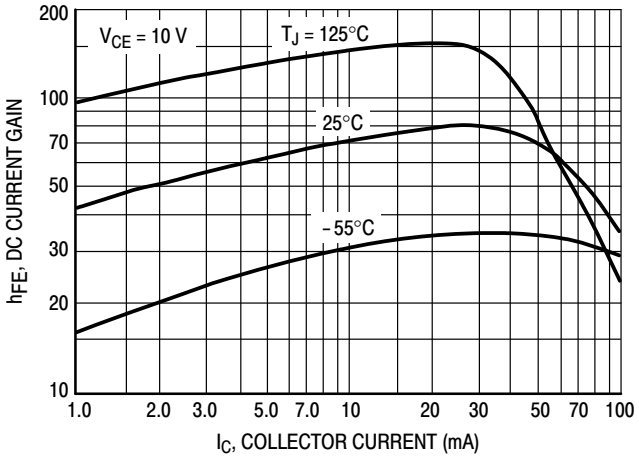


Figure 1. DC Current Gain

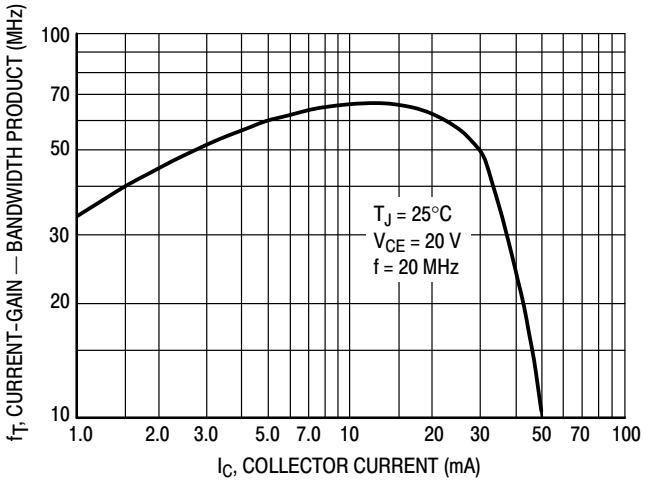


Figure 2. Current−Gain — Bandwidth Product

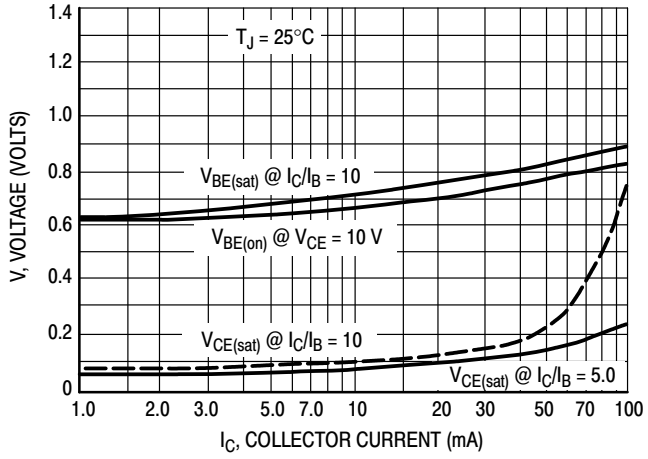


Figure 3. “On” Voltages

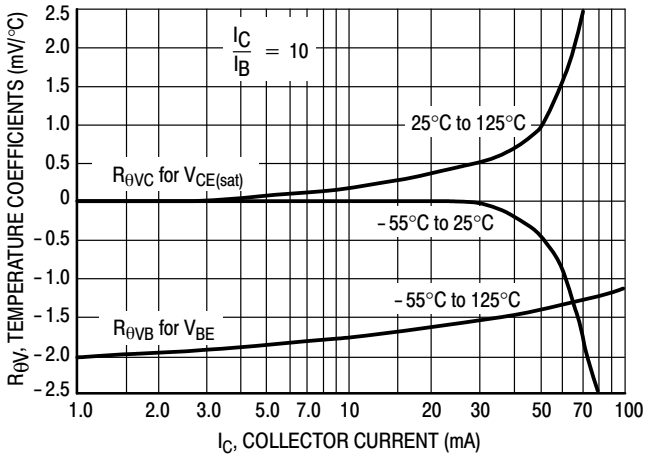


Figure 4. Temperature Coefficients

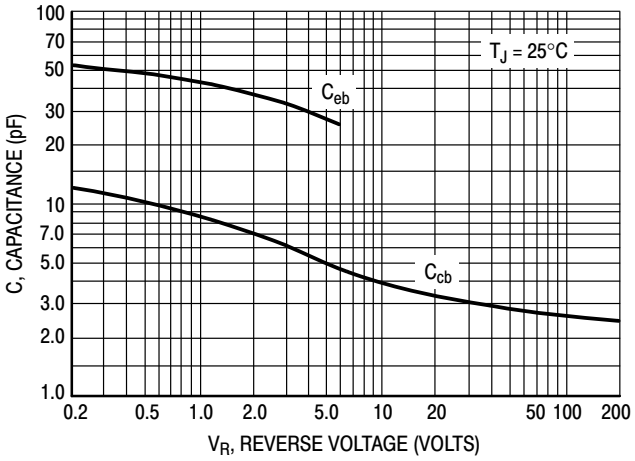


Figure 5. Capacitance

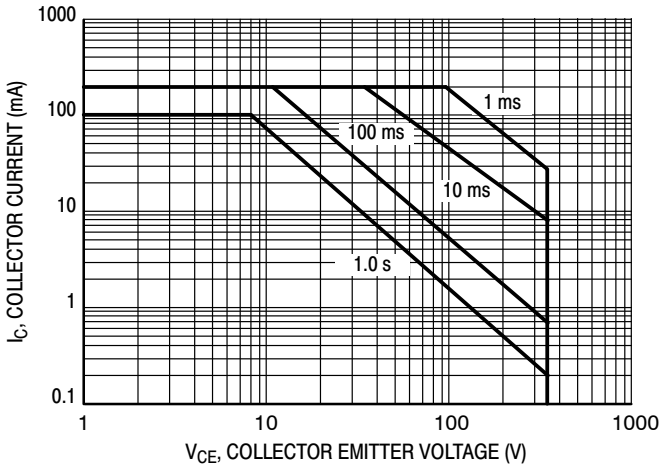


Figure 6. Safe Operating Area

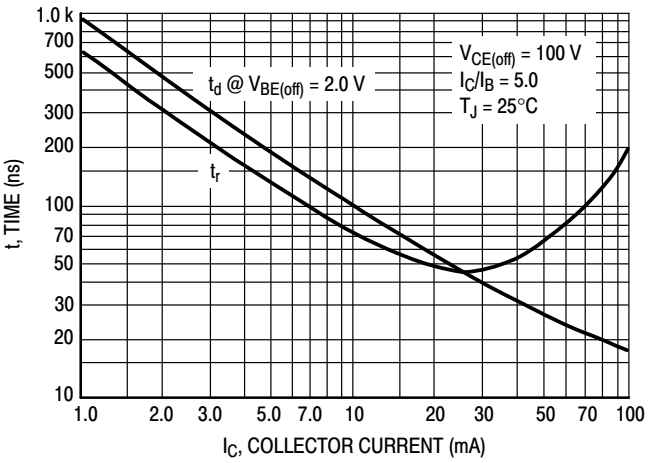


Figure 7. Turn−On Time

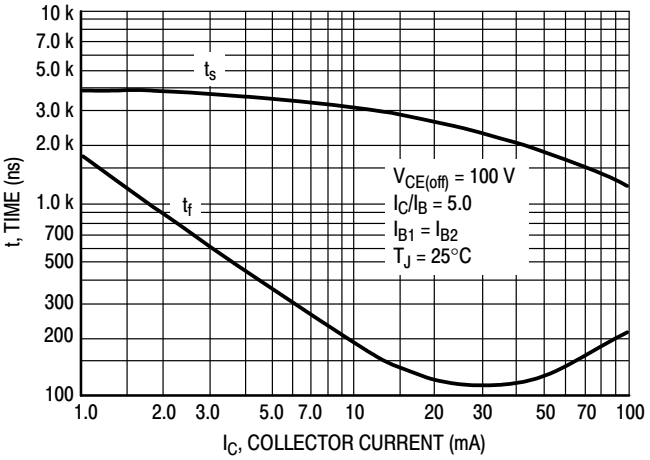


Figure 8. Turn−Off Time

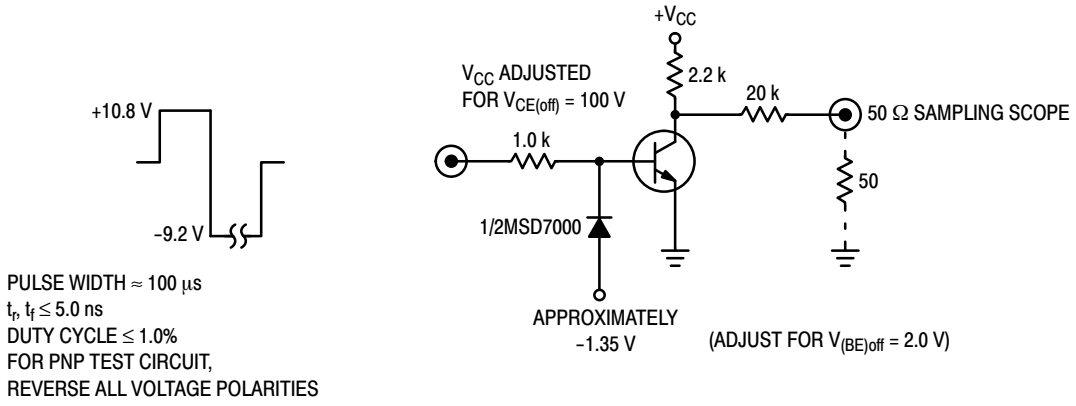


Figure 9. Switching Time Test Circuit

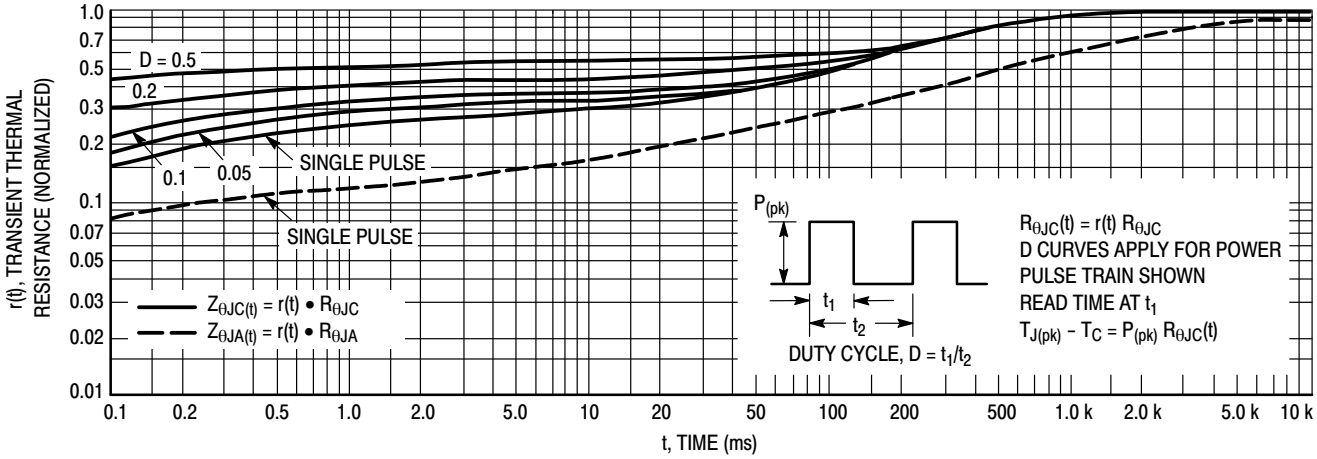
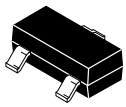


Figure 10. Thermal Response

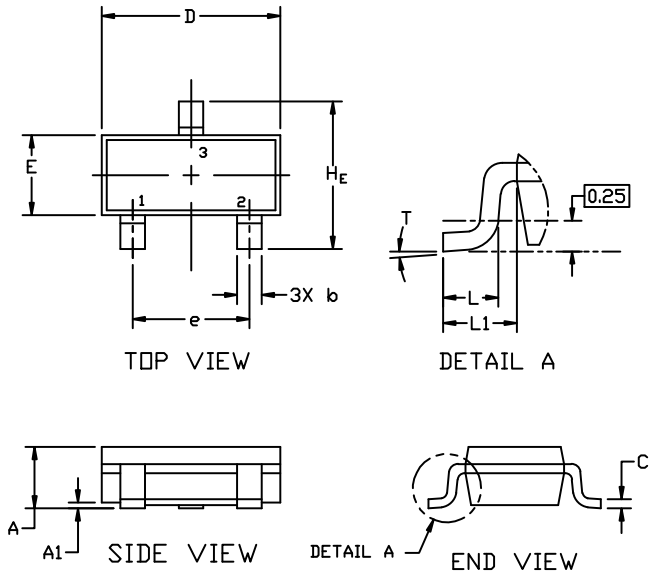
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

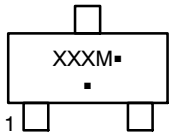


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

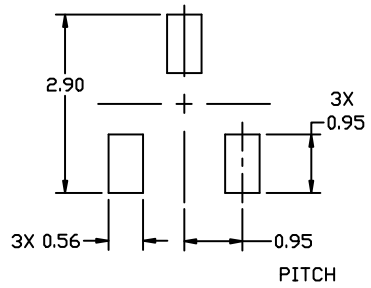
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

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