



PMZB670UPE

20 V, single P-channel Trench MOSFET

Rev. 3 — 23 March 2012

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Low threshold voltage
- Trench MOSFET technology
- ESD protection up to 2 kV
- Ultra thin package profile of 0.37 mm

1.3 Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

1.4 Quick reference data

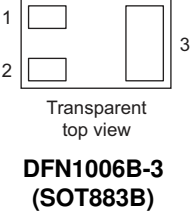
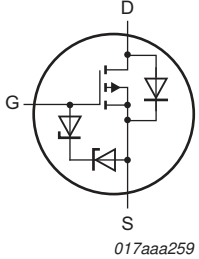
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-680	mA
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -400\text{ mA}; T_j = 25\text{ °C}$	-	0.67	0.85	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZB670UPE	DFN1006B-3	Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm	SOT883B

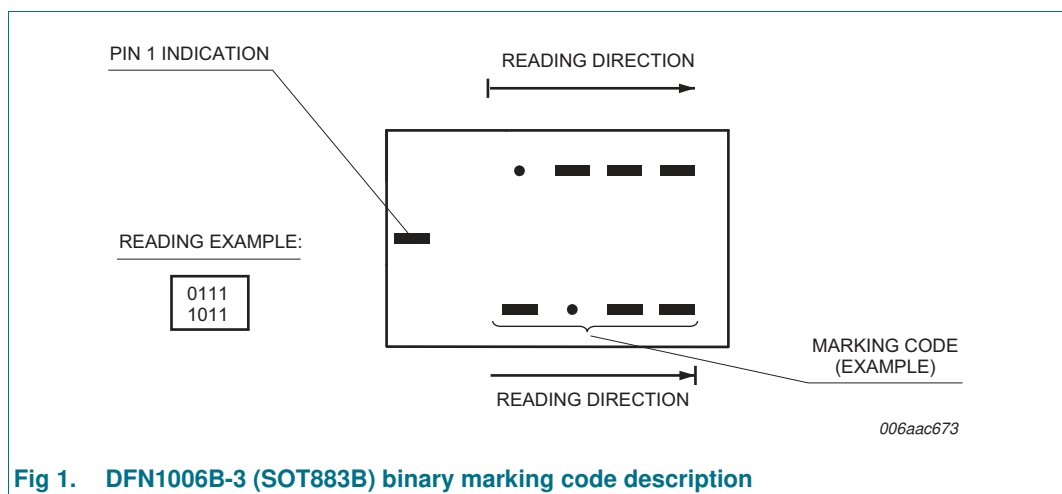
4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PMZB670UPE	0000 1011

[1] For DFN1006B-3 (SOT883B) binary marking code description see [Figure 1](#).

4.1 Binary marking code description



5. Limiting values

Table 5. Limiting values

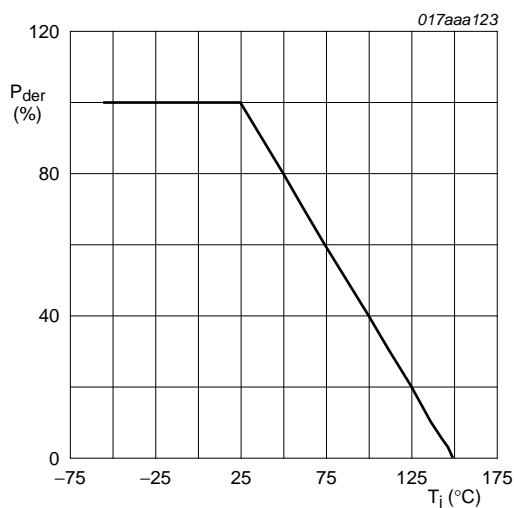
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-20	V	
V_{GS}	gate-source voltage		-8	8	V	
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-680	mA
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-425	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	-2.7	A	
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	360	mW
			[1]	-	715	mW
		$T_{sp} = 25\text{ °C}$		-	2700	mW
T_j	junction temperature		-55	150	°C	
T_{amb}	ambient temperature		-55	150	°C	
T_{stg}	storage temperature		-65	150	°C	
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-680	mA
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

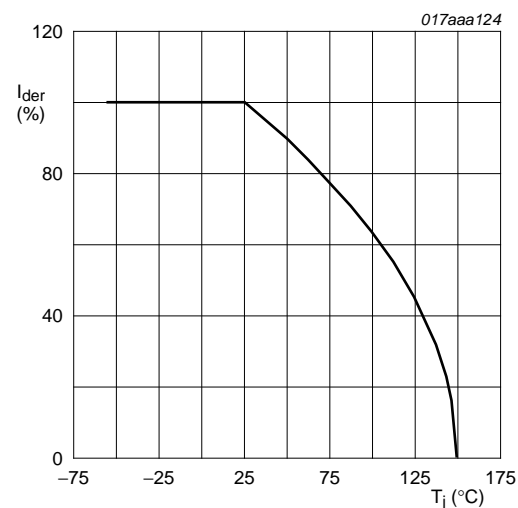
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



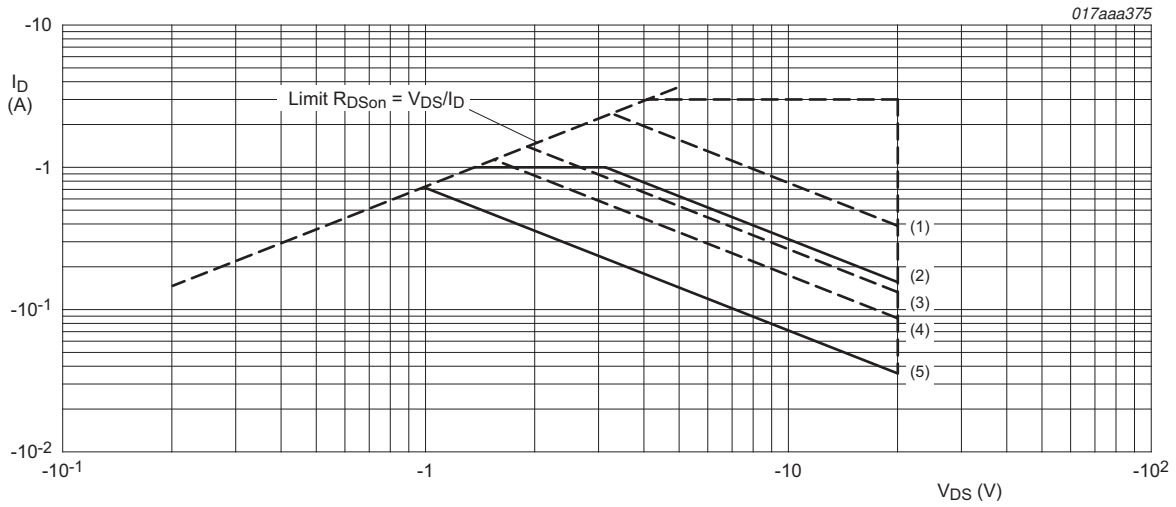
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 3. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

(1) $t_p = 1$ ms

(2) DC; $T_{sp} = 25$ °C

(3) $t_p = 10$ ms

(4) $t_p = 100$ ms

(5) DC; $T_{amb} = 25$ °C; drain mounting pad 1 cm²

Fig 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	305	360	K/W
			[2]	-	150	175	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

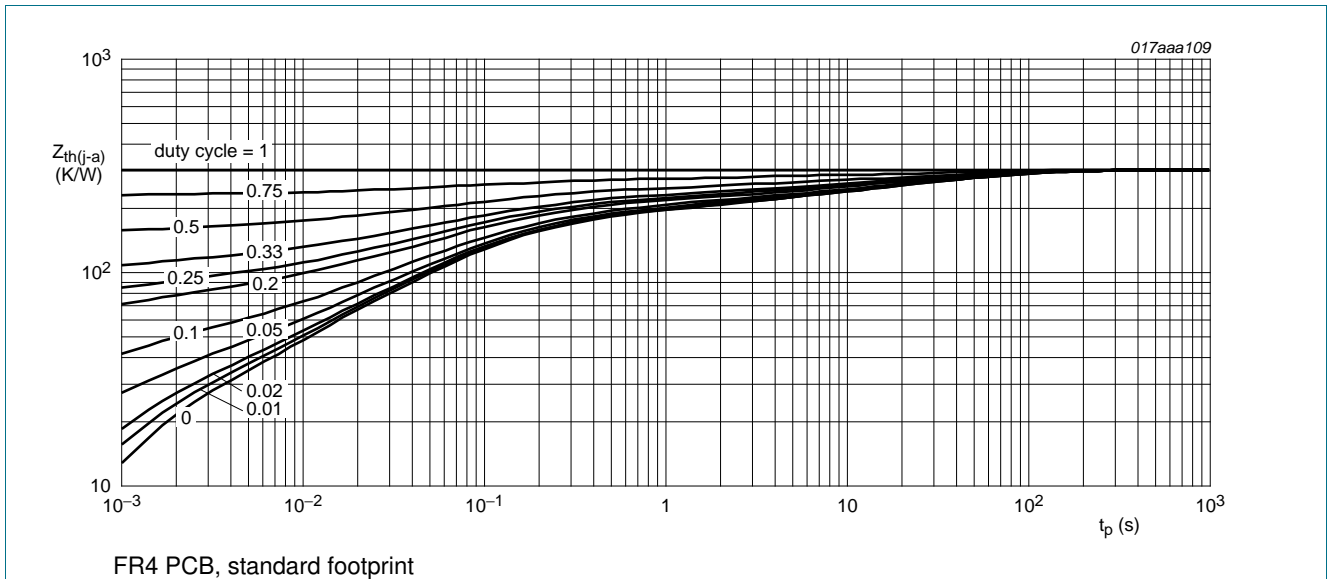


Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

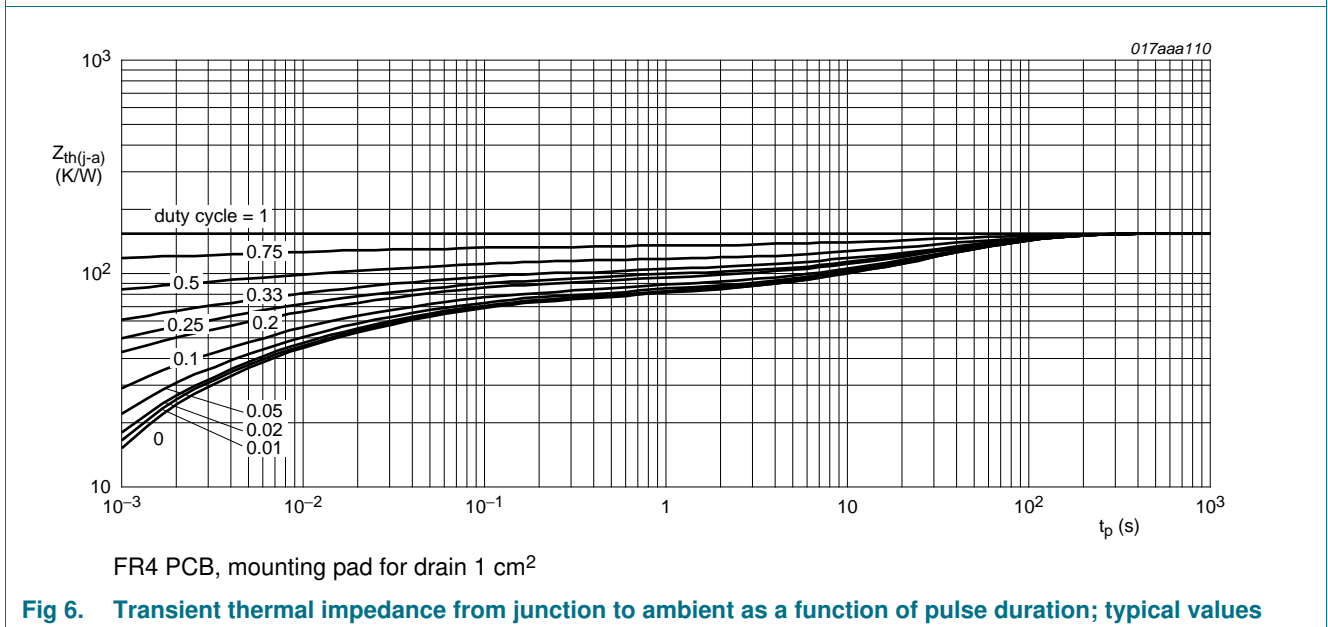


Fig 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	-0.5	-0.9	-1.3	V
I_{DSS}	drain leakage current	$V_{DS} = -20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
		$V_{DS} = -20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	-10	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-2	μA
		$V_{GS} = -8 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-2	μA
		$V_{GS} = 4.5 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-0.5	μA
		$V_{GS} = -4.5 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-0.5	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$; $I_D = -400 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.67	0.85	Ω
		$V_{GS} = -4.5 \text{ V}$; $I_D = -400 \text{ mA}$; $T_j = 150 \text{ }^\circ\text{C}$	-	1.1	1.4	Ω
		$V_{GS} = -2.5 \text{ V}$; $I_D = -200 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	1.2	1.5	Ω
		$V_{GS} = -1.8 \text{ V}$; $I_D = -10 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	1.8	2.8	Ω
g_{fs}	forward transconductance	$V_{DS} = -10 \text{ V}$; $I_D = -200 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	610	-	mS
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}$; $I_D = -400 \text{ mA}$; $V_{GS} = -4.5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.76	1.14	nC
Q_{GS}	gate-source charge		-	0.28	-	nC
Q_{GD}	gate-drain charge		-	0.18	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 \text{ V}$; $f = 1 \text{ MHz}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	58	87	pF
C_{oss}	output capacitance		-	21	-	pF
C_{rss}	reverse transfer capacitance		-	12	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}$; $R_L = 250 \Omega$; $V_{GS} = -4.5 \text{ V}$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 \text{ }^\circ\text{C}$	-	18	36	ns
t_r	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	80	160	ns
t_f	fall time		-	72	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -300 \text{ mA}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-0.48	-0.84	-1.2	V

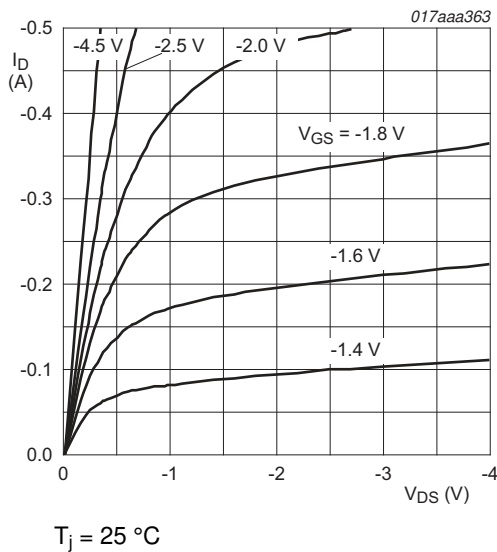


Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values

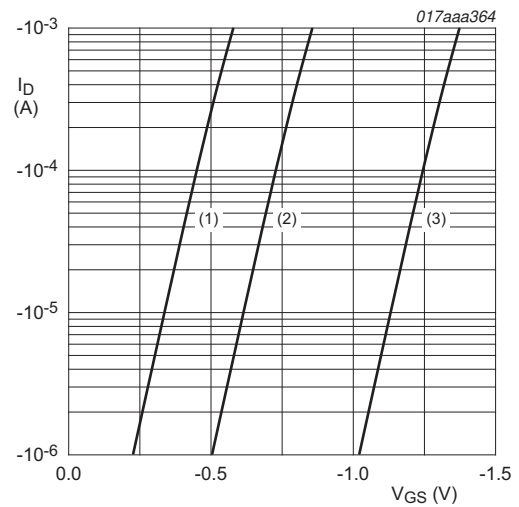


Fig 8. Sub-threshold drain current as a function of gate-source voltage

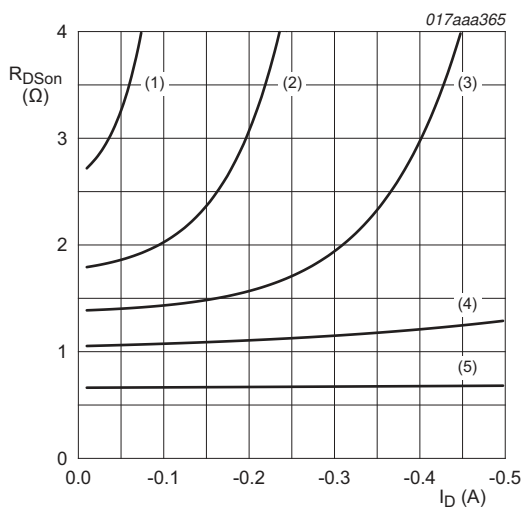


Fig 9. Drain-source on-state resistance as a function of drain current; typical values

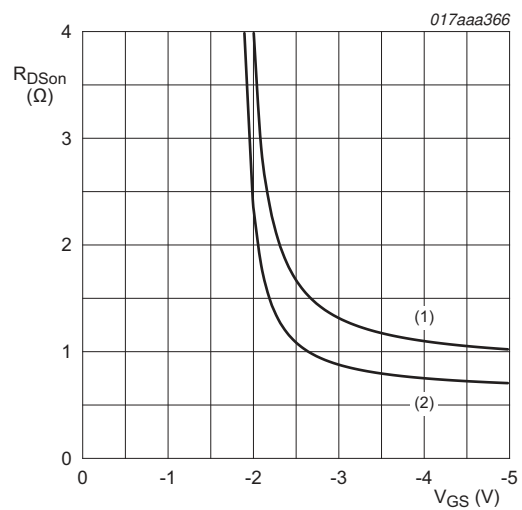
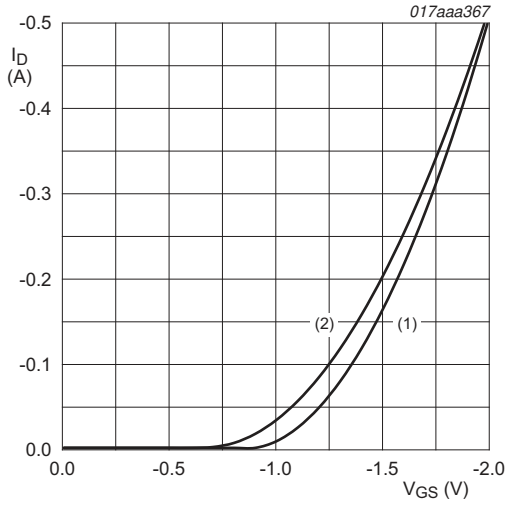
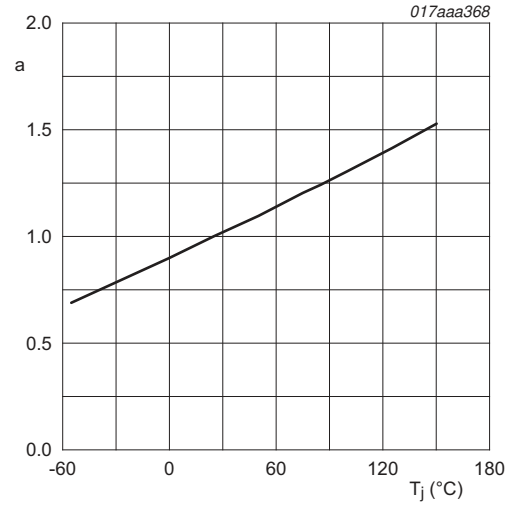


Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



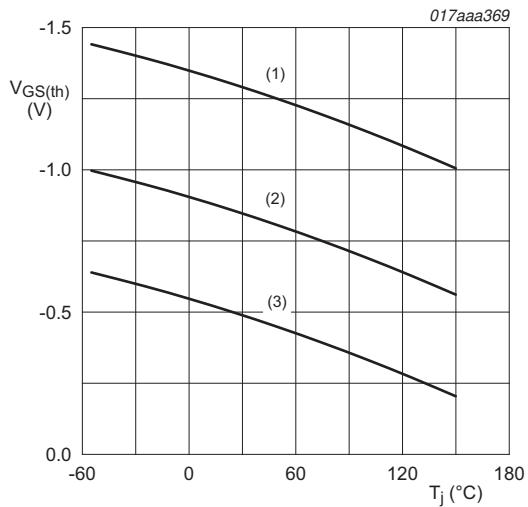
$V_{DS} > I_D \times R_{DS(on)}$
 (1) $T_j = 25\text{ °C}$
 (2) $T_j = 150\text{ °C}$

Fig 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values



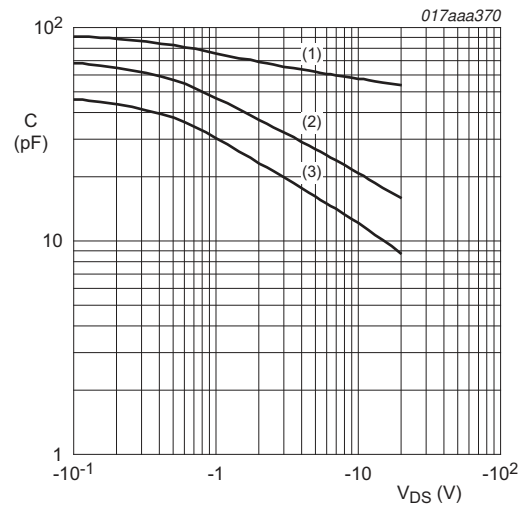
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

Fig 12. Normalized drain-source on-state resistance as a function of ambient temperature; typical values



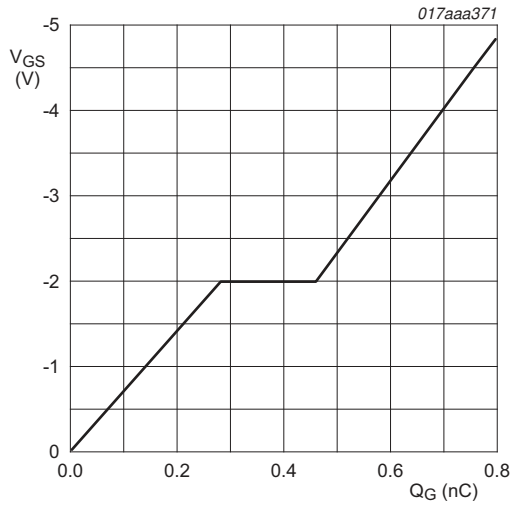
$I_D = -0.25\text{ mA}$; $V_{DS} = V_{GS}$
 (1) maximum values
 (2) typical values
 (3) minimum values

Fig 13. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}$; $V_{GS} = 0\text{ V}$
 (1) C_{iss}
 (2) C_{oss}
 (3) C_{rss}

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -0.4$ A; $V_{DD} = -10$ V; $T_{amb} = 25$ °C

Fig 15. Gate-source voltage as a function of gate charge; typical values

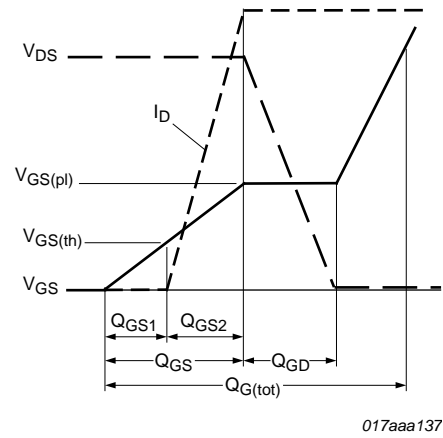
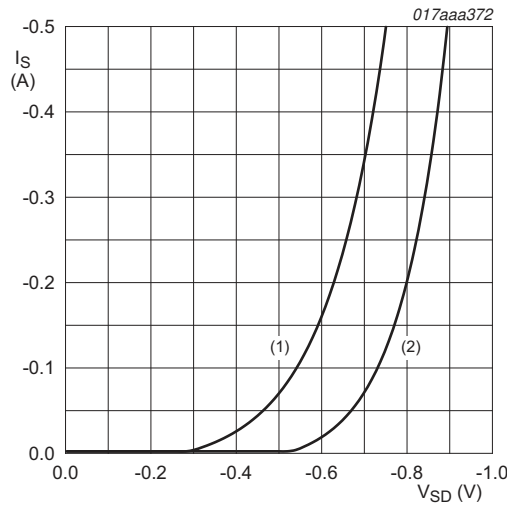


Fig 16. Gate charge waveform definitions



$V_{GS} = 0$ V
 (1) $T_{amb} = 150$ °C
 (2) $T_{amb} = 25$ °C

Fig 17. Source current as a function of source-drain voltage; typical values

8. Test information

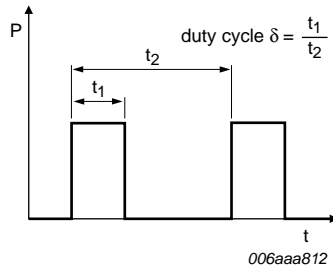


Fig 18. Duty cycle definition

9. Package outline

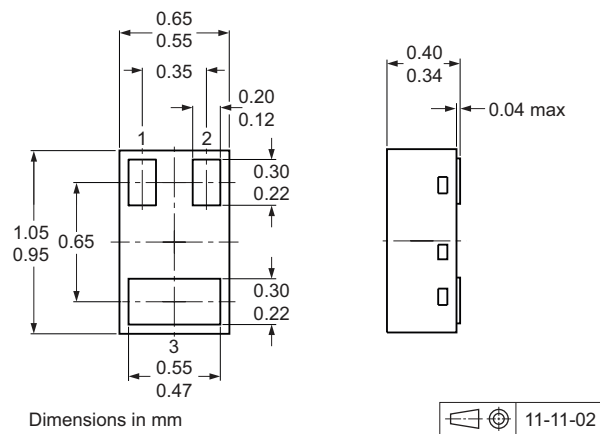


Fig 19. Package outline DFN1006B-3 (SOT883B)

10. Soldering

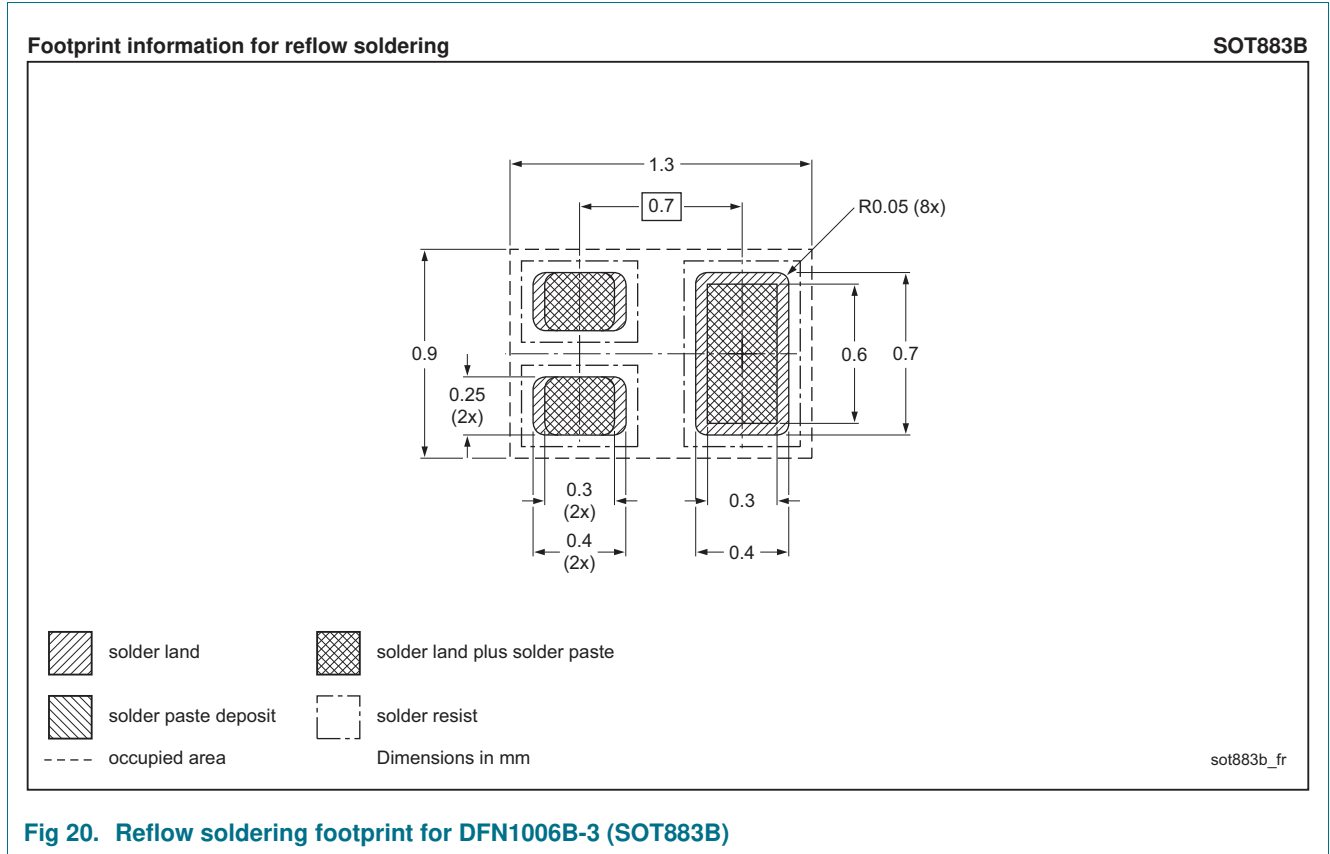


Fig 20. Reflow soldering footprint for DFN1006B-3 (SOT883B)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMZB670UPE v.3	20120323	Product data sheet	-	PMZB670UPE v.2
Modifications:	• 1.2 "Features and benefits" is corrected.			
PMZB670UPE v.2	20120207	Product data sheet	-	PMZB670UPE v.1
PMZB670UPE v.1	20120131	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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