

## **AN-1479 LP38856S-1.2 Evaluation Board**

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### **1 Introduction**

This board is designed to allow the evaluation of the LP38856S-1.2 voltage regulator. Each board is assembled and tested in the factory. This evaluation board has the TO-263 5-lead package mounted.

### **2 General Description**

The LP38856 is a dual-rail LDO linear regulator capable of supplying up to 3A of output current, and incorporates an enable function.

The device has been designed to work with 10  $\mu\text{F}$  input and output ceramic capacitors, and 1 $\mu\text{F}$  bias capacitors. Footprints areas for  $C_{\text{IN}}$  and  $C_{\text{OUT}}$  will allow for a variety of sizes.

### **3 Operation**

The input voltage, applied between  $V_{\text{IN}}$  and GND, should be at least 1.0 V greater than  $V_{\text{OUT}}$ , and no higher than the applied  $V_{\text{BIAS}}$  voltage.

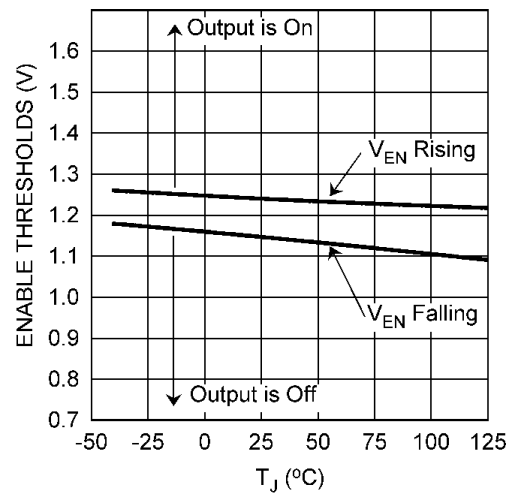
The bias voltage, applied between  $V_{\text{BIAS}}$  and GND should be above the minimum bias voltage of 3.0 V, and no higher than the maximum of 5.5 V.

Loads can be connected to  $V_{\text{OUT}}$  with reference to GND.

$V_{\text{OUT}}$  and  $V_{\text{IN}}$  test points are provided on the board to allow accurate measurements directly on the evaluation board, eliminating any voltage drop on the PCB traces or connecting wires to the load.

ON/OFF control is provided by supplying a logic level signal to the Enable pin. A minimum  $V_{\text{EN}}$  value of 1.3 V is required at this pin to enable the LDO output. The LDO output will be shutdown when the  $V_{\text{EN}}$  value is 1.0 V or less. The  $V_{\text{EN}}$  threshold incorporates approximately 100 mV of hysteresis.

In applications where the LP38856 is operated continuously, the Enable pin can be connected directly to  $V_{\text{BIAS}}$ , or left open. The Enable pin has a 200 k $\Omega$  internal resistor to  $V_{\text{BIAS}}$ . If the Enable pin is left open, care should be taken to minimize any capacitance on the Enable pin, as any capacitance will introduce an RC delay time on the Enable function.

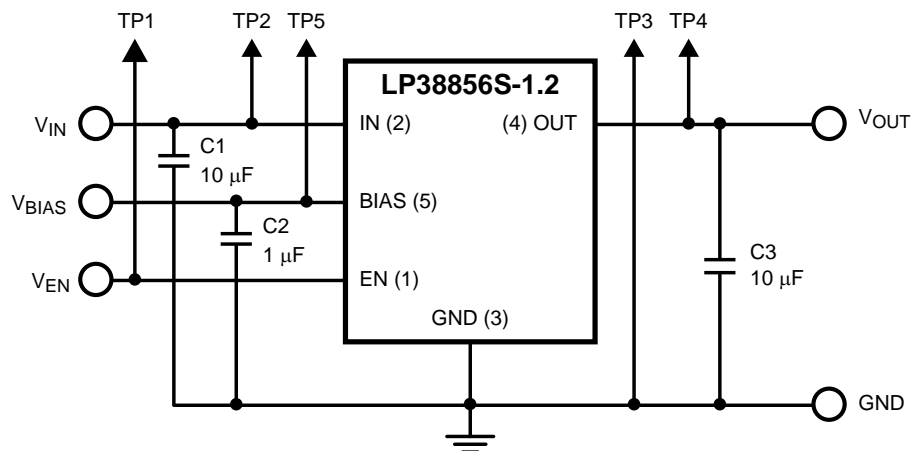


**Figure 1. Enable Thresholds**

#### 4 Hardware

The schematic is shown in [Figure 2](#) and the layout of the evaluation board is shown in [Figure 3](#).

#### 5 Schematic Diagram



**Figure 2. Evaluation Board Schematic**

## 6 PCB Layout

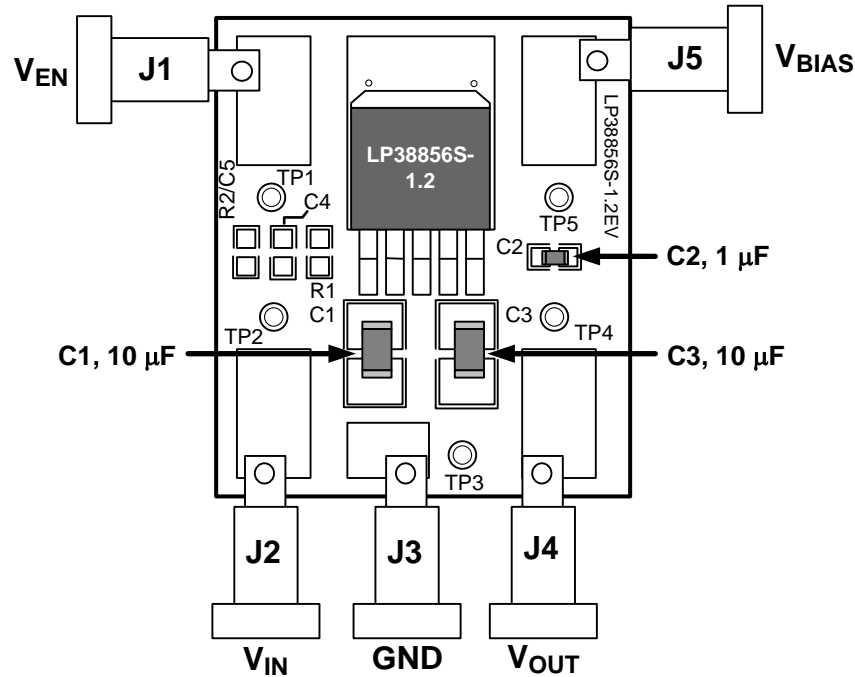


Figure 3. Evaluation Board Component and Pin Layout

## 7 Power Dissipation

The TO-263 package alone has a junction to ambient thermal resistance ( $\theta_{JA}$ ) rating of  $60^{\circ}\text{C}/\text{W}$ . When mounted on the LP38856S evaluation board, the  $\theta_{JA}$  rating is approximately  $37^{\circ}\text{C}/\text{W}$ .

Although there is only approximately 0.28 square inches of copper area immediately under the tab, the top copper surface area is extended to additional copper area on the bottom of the board by five thermal vias.

With the  $37^{\circ}\text{C}/\text{W}$  thermal rating, the LP38856S evaluation board will dissipate a maximum of 2.75W with  $T_A = 25^{\circ}\text{C}$ .

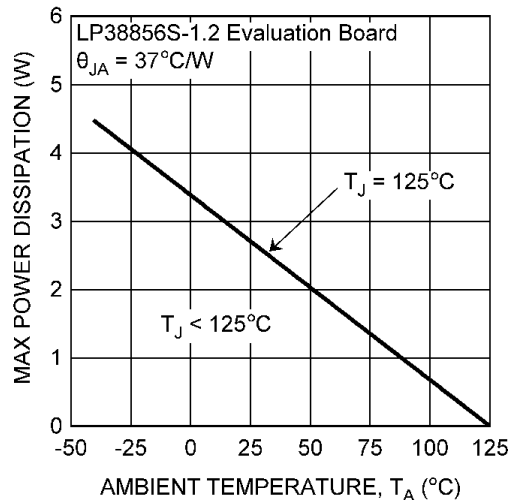


Figure 4. Maximum Power Dissipation vs Ambient Temperature

## 8 Bill of Materials

ID	Name	Description	Manufacturer	Part Number
U1	U1	LP38856	Texas Instruments	LP38856
C1	C <sub>IN</sub>	10 $\mu$ F, 10%, MLCC, 10 V, X7R, 1210	AVX	1210ZC106KAT2A
C2	C <sub>BIAS</sub>	1 $\mu$ F, 10%, MLCC, 10 V, X7R, 0805	AVX	0805ZC105KAT2A
C3	C <sub>OUT</sub>	10 $\mu$ F, 10%, MLCC, 10 V, X7R, 1210	AVX	1210ZC106KAT2A
C4	—	Not Installed	—	—
C5	—	Not Installed	—	—
J1	V <sub>EN</sub>	Banana Jack : Insulated Solder Terminal - WHITE	Johnson Components	108-0901-001
J2	V <sub>IN</sub>	Banana Jack : Insulated Solder Terminal - RED		108-0902-001
J3	GND	Banana Jack : Insulated Solder Terminal - BLACK		108-0903-001
J4	V <sub>OUT</sub>	Banana Jack : Insulated Solder Terminal - ORANGE		108-0906-001
J5	V <sub>BIAS</sub>	Banana Jack : Insulated Solder Terminal - BLUE		108-0910-001
R1	—	Not Installed	—	—
R2	—	Not Installed	—	—
TP1	TP <sub>EN</sub>	Turret Terminal : Mounting Hole Diameter = 0.062"	Keystone	1593-2
TP2	TP <sub>IN</sub>			
TP3	TP <sub>GND</sub>			
TP4	TP <sub>OUT</sub>			
TP5	TP <sub>BIAS</sub>			

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