8-Channel, I²C, 12-Bit SAR ADC with Temperature Sensor

Enhanced Product

AD7291-EP

FEATURES

- 12-bit SAR ADC
  - 8 single-ended analog input channels
  - Analog input range: 0 V to 2.5 V
- 12-bit temperature to digital converter
  - Temperature sensor accuracy of ±1°C typical
- Channel sequencer operation
- Specified for V_{DD} of 2.8 V to 3.6 V
- Logic voltage V_{DRIVE} = 1.65 V to 3.6 V
- Internal 2.5 V reference
- I²C-compatible serial interface supports standard and fast speed modes
- Out of range indicator/alert function
- Autocycle mode
- Power-down current: 13 µA maximum
- 20-lead LFCSP package

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended industrial temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available upon request

FUNCTIONAL BLOCK DIAGRAM

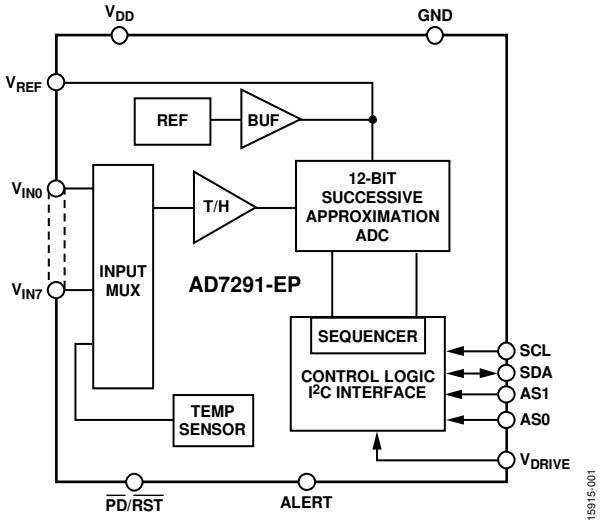

Figure 1.

GENERAL DESCRIPTION

The AD7291-EP is a 12-bit, low power, 8-channel, successive approximation analog-to-digital converter (ADC) with an internal temperature sensor.

The device operates from a single 3.3 V power supply and features an I²C-compatible interface. The device contains a 9-channel multiplexer and a track-and-hold amplifier with an input bandwidth of 30 MHz. The device has an on-chip 2.5 V reference that can be disabled to allow the use of an external reference.

The AD7291-EP provides a 2-wire serial interface compatible with I²C interfaces. The I²C interface supports standard and fast I²C interface modes. The AD7291-EP normally remains in a partial power-down state while not converting and powers up for conversions. The conversion process can be controlled by a command mode where conversions occur across I²C write operations or an autocycle mode selected through software control.

The AD7291-EP includes a high accuracy band gap temperature sensor, which is monitored and digitized by the 12-bit ADC to give a resolution of 0.25°C.

The AD7291-EP offers a programmable sequencer, which enables the selection of a preprogrammable sequence of channels for conversion.

On-chip limit registers can be programmed with high and low limits for the conversion results; an out-of-range indicator output (ALERT) becomes active when the programmed high or low limits are violated by the conversion result. This output can be used as an interrupt.

Additional application and technical information can be found in the AD7291 data sheet.

Rev. 0 Document Feedback

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REVISION HISTORY

7/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.8 V to 3.6 V; V_{DRIVE} = 1.65 V to 3.6 V; f_{SCL} = 400 kHz, fast SCLK mode; V_{REF} = 2.5 V internal/external; T_A = −55°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 1 kHz sine wave
Signal-to-Noise Ratio (SNR)	70	71		dB	
Signal-to-Noise + Distortion Ratio (SINAD)	70	71		dB	
Total Harmonic Distortion (THD)		−84	−78	dB	
Spurious-Free Dynamic Range (SFDR)		−85	−80	dB	
Intermodulation Distortion (IMD)					f_A = 5.4 kHz, f_B = 4.6 kHz
Second-Order Terms		−88		dB	
Third-Order Terms		−88		dB	
Channel-to-Channel Isolation		−100		dB	f_{IN} = 10 kHz
Full Power Bandwidth[2]		30		MHz	At 3 dB
		10		MHz	At 0.1 dB
DC ACCURACY					
Resolution	12			Bits	
Integral Nonlinearity (INL)		±0.5	±1	LSB	
Differential Nonlinearity (DNL)		±0.5	±0.99	LSB	Guaranteed no missing codes to 12 bits
Offset Error		±2	±4.5	LSB	
Offset Error Matching		±2.5	±4.5	LSB	
Offset Temperature Drift		4		ppm/°C	
Gain Error		±1	±4	LSB	
Gain Error Matching		±1	±2.5	LSB	
Gain Temperature Drift		0.5		ppm/°C	
ANALOG INPUT					
Input Voltage Ranges	0		V_{REF}	V	
DC Leakage Current		±0.01	±1	µA	
Input Capacitance[2]		34		pF	When in track
		8		pF	When in hold
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[3]	2.4925	2.5	2.5075	V	±0.3% maximum at 25°C
Long-Term Stability		150		ppm	For 1000 hours
Output Voltage Hysteresis		50		ppm	
Reference Input Voltage Range[4]	1		2.5	V	
DC Leakage Current		±0.01	±1	µA	External reference applied to Pin V_{REF}
V_{REF} Output Impedance		1		Ω	
Reference Temperature Coefficient		12	35	ppm/°C	
V_{REF} Noise[2]		60		µV rms	Bandwidth = 10 MHz
LOGIC INPUTS (SDA, SCL)					
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}			V	
Input Low Voltage, V_{INL}			0.3 × V_{DRIVE}	V	
Input Current, I_{IN}		±0.01	±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[2]		6		pF	
Input Hysteresis, V_{HYST}	0.1 × V_{DRIVE}			V	

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} − 0.3			V	V_{DRIVE} < 1.8
	V_{DRIVE} − 0.2			V	V_{DRIVE} ≥ 1.8
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Floating State Leakage Current		±0.01	±1	µA	
Floating State Output Capacitance[2]		8		pF	
INTERNAL TEMPERATURE SENSOR					
Operating Range	−55		+125	°C	
Accuracy		±1	±2	°C	T_A = −55°C to +85°C
		±1	±3	°C	T_A = 85°C to 125°C
Resolution		0.25		°C	LSB size
CONVERSION RATE					
Conversion Time		3.2		µs	
Autocycle Update Rate[5]		50		µs	
Throughput Rate			22.22	kSPS	f_{SCL} = 400 kHz
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
V_{DD}	2.8	3	3.6	V	
V_{DRIVE}	1.65	3	3.6	V	
I_{TOTAL}[6, 7]					
Normal Mode (Operational)		2.9	3.5	mA	
Normal Mode (Static)		2.9	3.4	mA	
Full Power-Down Mode		0.3	1.6	µA	T_A = −55°C to +25°C
		1.6	4.5	µA	T_A = >25°C to 85°C
		4.9	13	µA	T_A = >85°C to 125°C
Power Dissipation[7]					
Normal Mode (Operational)		8.7	10.5	mW	V_{DD} = 3 V, V_{DRIVE} = 3 V
		10.4	12.6	mW	
Normal Mode (Static)		10.4	12.2	mW	
Full Power-Down Mode		1.1	5.8	µW	T_A = −55°C to +25°C
		5.8	16.2	µW	T_A = >25°C to 85°C
		17.6	46.8	µW	T_A = >85°C to 125°C

[1] All specifications expressed in decibels are referred to full-scale range (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[2] Sample tested during initial product release to ensure compliance.
[3] Refers to Pin V_{REF} specified for 25°C.
[4] A correction factor can be required on the temperature sensor results when using an external V_{REF} (see the AD7291 data sheet).
[5] Sampled during initial product release to ensure compliance; not subject to production testing.
[6] I_{TOTAL} is the total current flowing in V_{DD} and V_{DRIVE}.
[7] I_{TOTAL} and power dissipation are specified with V_{DD} = V_{DRIVE} = 3.6 V, unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD} to GND1, GND	−0.3 V to +5 V
V_{DRIVE} to GND1, GND	−0.3 V to +5 V
Analog Input Voltage to GND1	−0.3 V to +3 V
Digital Input Voltage to GND1	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to GND1	−0.3 V to V_{DRIVE} + 0.3 V
V_{REF} to GND1	−0.3 V to +3 V
GND to GND1	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb-free Temperature, Soldering	
Reflow	260(+0)°C
ESD	2 kV

[1] Transient currents of up to 100 mA do not cause latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-20-8[1]	52	6.5	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 9 thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

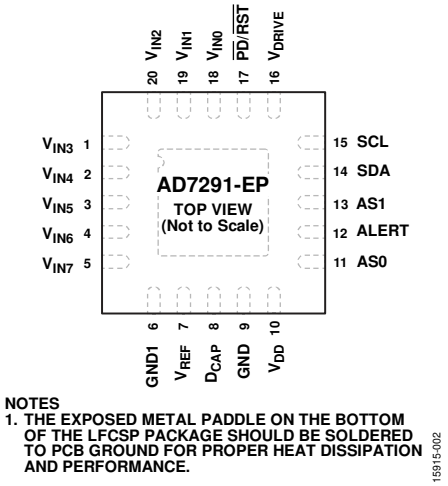


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 5, 18 to 20	V_{IN3}, V_{IN4}, V_{IN5}, V_{IN6}, V_{IN7}, V_{IN0}, V_{IN1}, V_{IN2}	Analog Inputs. The AD7291-EP has eight single-ended analog inputs that are multiplexed into the on-chip track-and-hold amplifier. Each input channel can accept analog inputs from 0 V to 2.5 V. Any unused input channels must be connected to GND1 to avoid noise pickup.
6	GND1	Ground. Ground reference point for the internal reference circuitry on the AD7291-EP. All analog input signals and the external reference signals must be referred to this GND1 voltage. The GND1 pin must be connected to the ground plane of a system. All ground pins must ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. The V_{REF} pin must be decoupled to this ground pin via a 10 µF decoupling capacitor.
7	V_{REF}	Internal Reference/External Reference Supply. The nominal internal reference voltage of 2.5 V appears at this pin. Provided the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system. Decoupling capacitors must be connected to this pin to decouple the reference buffer. For best performance, it is recommended to use a 10 µF decoupling capacitor on this pin to GND1. The internal reference can be disabled and an external reference supplied to this pin if required. The input voltage range for the external reference is 2.0 V to 2.5 V.
8	D_{CAP}	Decoupling Capacitor Pin. Decoupling capacitors (1 µF recommended) are connected to this pin to decouple the internal low dropout regulator (LDO).
9	GND	Ground. Ground reference point for all analog and digital circuitry on the AD7291-EP. The GND pin must be connected to the ground plane of the system. All ground pins must ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. Both D_{CAP} and V_{DD} pins must be decoupled to this GND pin.
10	V_{DD}	Supply Voltage, 2.8 V to 3.6 V. This supply must be decoupled to GND with 10 µF and 100 nF decoupling capacitors.
11, 13	AS0, AS1	Logic Inputs. Together, the logic state of these two inputs selects a unique I^2C address for the AD7291-EP. See the AD7291 data sheet for details. The device address depends on the voltage applied to these pins.
12	ALERT	Digital Output. This pin acts as an out-of-range indicator and, if enabled, becomes active when the conversion result violates the $DATA_{HIGH}$ or $DATA_{LOW}$ register values. See the AD7291 data sheet for further details.
14	SDA	Digital Input/Output. Serial bus bidirectional data. This open-drain output requires a pull-up resistor. The output coding is straight binary for the voltage channels and twos complement for the temperature sensor result.
15	SCL	Digital Inputs. Serial I^2C Bus Clock. This input requires a pull-up resistor. The data transfer rate in I^2C mode is compatible with both 100 kHz and 400 kHz operating modes.
16	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines the voltage at which the interface operates. This pin must be decoupled to GND. The voltage range on this pin is 1.65 V to 3.6 V and can be less than the voltage at V_{DD} but must never exceed it by more than 0.3 V.
17	$\overline{PD}/\overline{RST}$	Power-Down Pin. This pin places the device into a full power-down mode and enables power conservation when operation is not required. This pin can be used to reset the device by toggling the pin low for a minimum of 1 ns and a maximum of 100 ns. If the maximum time is exceeded, the device enters power-down mode. When placing the device in full power-down mode, the analog inputs must be returned to 0 V.
EPAD	EPAD	Exposed Pad. The exposed metal paddle on the bottom of the LFCSP package must be soldered to PCB ground for proper functionality and heat dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

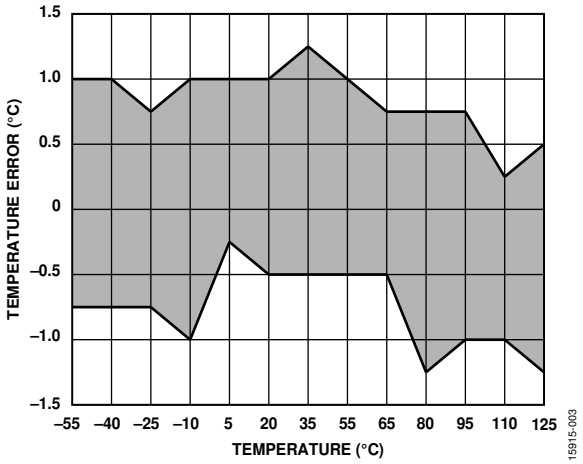


Figure 3. Temperature Accuracy at 3 V

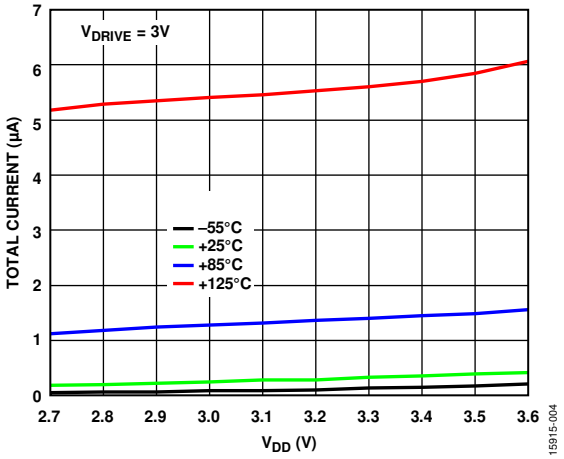
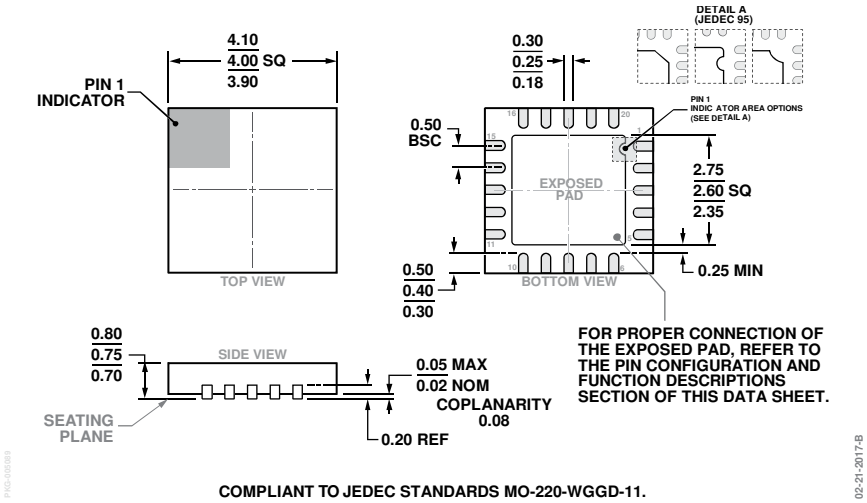


Figure 4. Full Shutdown Current vs. Supply Voltage for Various Temperatures

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.

Figure 5. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7291TCPZ-EP	−55°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
AD7291TCPZ-EP-RL7	−55°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).