



N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{(BR)DSS}	R _{DS(ON)} max	I _D max T _A = +25°C
30V	$23m\Omega$ @ V_{GS} = $10V$	10A
	$33m\Omega$ @ V_{GS} = $4.5V$	8A

Description

This MOSFET has been designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Backlighting
- Power Management Functions
- DC-DC Converters

Features and Benefits

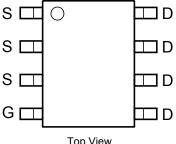
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Low Gate Resistance
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

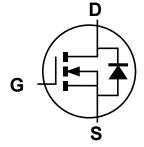
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish Matte Tin annealed over Copper leadframe.
 Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.074 grams (approximate)



Top View



Top View Internal Schematic



Equivalent circuit

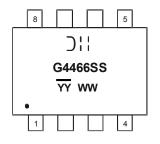
Ordering Information (Note 4)

Part Number	Case	Packaging
DMG4466SSS-13	SO-8	2500 / Tape & Reel

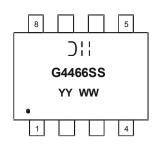
Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

□ : = Manufacturer's Marking G4466SS = Product Type Marking Code YYWW = Date Code Marking YY or YY = Year (ex: 13 = 2013) WW = Week (01 - 53)

YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)
YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)



Maximum Ratings (@ $T_A = +25^{\circ}C$, unless otherwise specified.)

Characte		Symbol	Value	Unit	
Drain-Source Voltage			V _{DSS}	30	V
Gate-Source Voltage			V _{GSS}	±25	V
Continuous Drain Current (Note 5)	Steady State	T _A = +25°C T _A = +85°C	I _D	10 6	А
Pulsed Drain Current (Note 5)			I _{DM}	60	A
Avalanche Current (Notes 6)			I _{AR}	16	А
Repetitive Avalanche Energy (Notes 6) L = 0.1mH			E _{AR}	12.8	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P _D	1.42	W
Thermal Resistance, Junction to Ambient @TA = +25°C (Note 5)	$R_{ heta JA}$	88.4	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	_	V	$V_{GS} = 0V$, $I_D = 250\mu A$	
Zero Gate Voltage Drain Current	I _{DSS}	1	_	1	μΑ	V _{DS} = 30V, V _{GS} = 0V	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 25V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V _{GS(th)}	1.0	1.45	2.4	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
Static Drain-Source On-Resistance	D	_	15	23	mΩ	$V_{GS} = 10V, I_D = 10A$	
Static Dialif-Source Off-Resistance	R _{DS} (ON)		25	33	11122	V _{GS} = 4.5V, I _D = 7.5A	
Forward Transfer Admittance	Y _{fs}		2.5	_	S	V _{DS} = 5V, I _D = 10A	
Diode Forward Voltage	V_{SD}	_	0.69	1	V	V _{GS} = 0V, I _S = 1A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}	1	478.9	_	pF	., .=., .,	
Output Capacitance	Coss		96.7	_	pF	$V_{DS} = 15V, V_{GS} = 0V,$ f = 1.0MHz	
Reverse Transfer Capacitance	C _{rss}		61.4	_	pF	11 - 1:0MHZ	
Gate Resistance	R_g	0.4	1.1	1.6	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	5.0	8	nC	V - 45V V - 40V L - 40A	
Total Gate Charge (V _{GS} = 10V)	Qg	_	10.5	17	IIC		
Gate-Source Charge	Q _{gs}	_	1.8	_	nC	V _{DS} = 15V, V _{GS} = 10V, I _D = 10A	
Gate-Drain Charge	Q_{gd}	_	1.6	_	nC		
Turn-On Delay Time	t _{D(on)}	_	2.9	_	ns	$V_{GS} = 10V, V_{DS} = 15V,$ $R_{G} = 3\Omega, R_{L} = 1.5\Omega$	
Turn-On Rise Time	t _r	_	7.9	_	ns		
Turn-Off Delay Time	t _{D(off)}	_	14.6	_	ns		
Turn-Off Fall Time	t _f	_	3.1	_	ns		

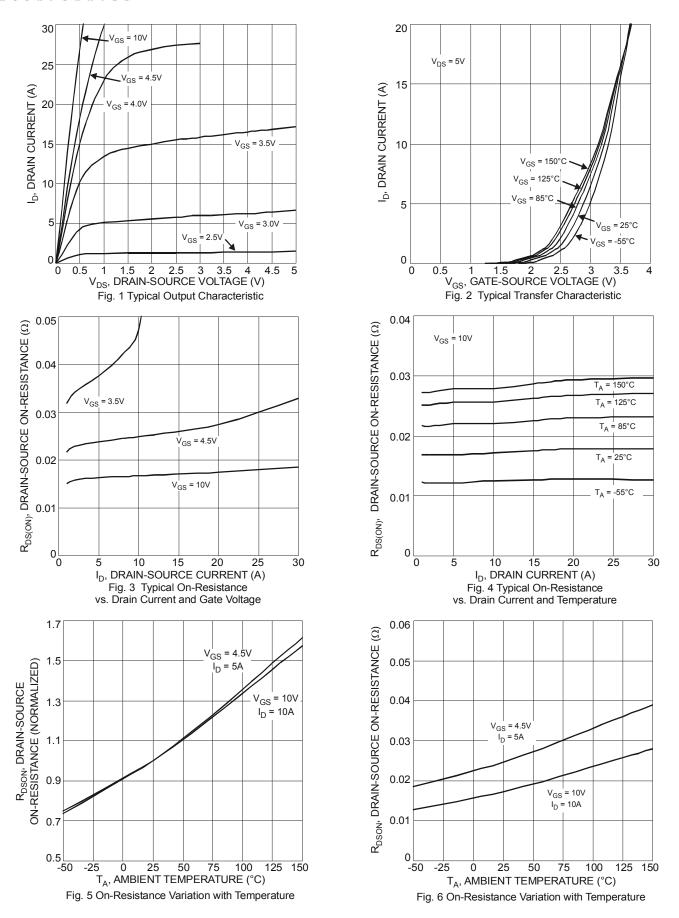
Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

6. I_{AR} and E_{AR} rating are based on low frequency and duty cycles to keep T_J = +25°C

7. Short duration pulse test used to minimize self-heating effect.

8. Guaranteed by design. Not subject to product testing.







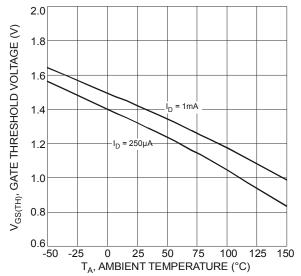
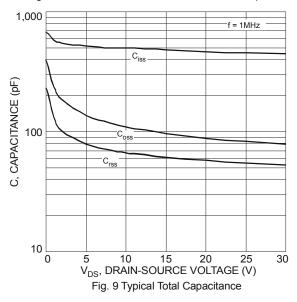
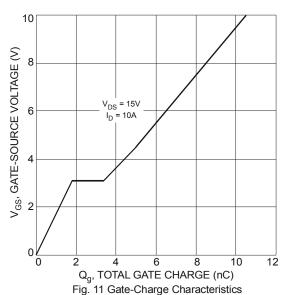
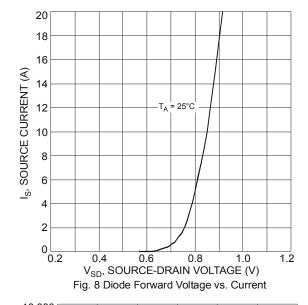
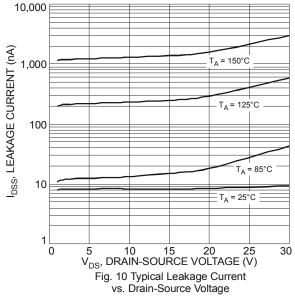


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

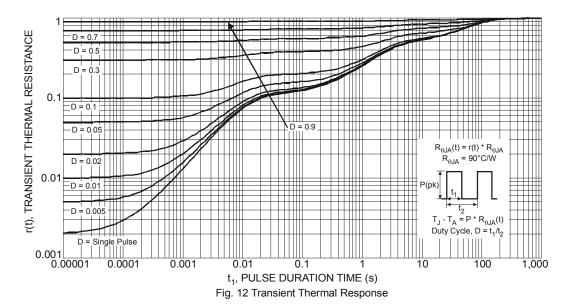






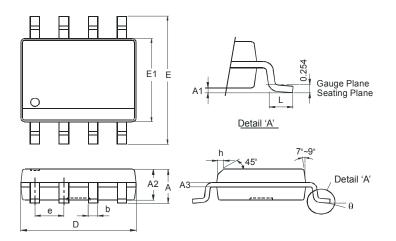






Package Outline Dimensions

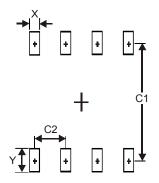
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SO-8					
Dim	Min	Max			
Α	-	1.75			
A1	0.10	0.20			
A2	1.30	1.50			
A3	0.15	0.25			
b	0.3	0.5			
D	4.85	4.95			
Е	5.90	6.10			
E1	3.85	3.95			
е	1.27 Typ				
h	-	0.35			
L	0.62	0.82			
θ	0°	8°			
All Dimensions in mm					

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for latest version.



Dimensions	Value (in mm)			
Х	0.60			
Υ	1.55			
C1	5.4			
C2	1.27			



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