Semiconductor Corporation

CS80600

High Speed Jitter Attenuator

Features

- Accepts Input Clock with Frequency of 4.5 MHz to 8.5 MHz
- Unique Clock-Tracking Circuitry
- Tolerates and Attenuates At Least 3 Unit Intervals of Jitter
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

General Description

The CS80600 from Crystal Semiconductor accepts 4.5 to 8.5 MHz clock and data inputs and removes up to ±3 data bits of jitter before outputting the data and clock. Jitter is removed using an internal clock tracking circuit and an 8-bit FIFO elastic store.

Applications

- **Token Ring:** The CS80600 can be used to eliminate the accumulation of data-pattern dependent jitter which is the primary factor limiting the size of token rings. The CS80600 is intended for application in station adaptor cards, in active wiring concentrators, and in repeators.
- **PCM:** TIC, T2, and CEPT2 and second order multiplexors.

ORDERING INFORMATION
CS80600-CP - 14 Pin Plastic DIP

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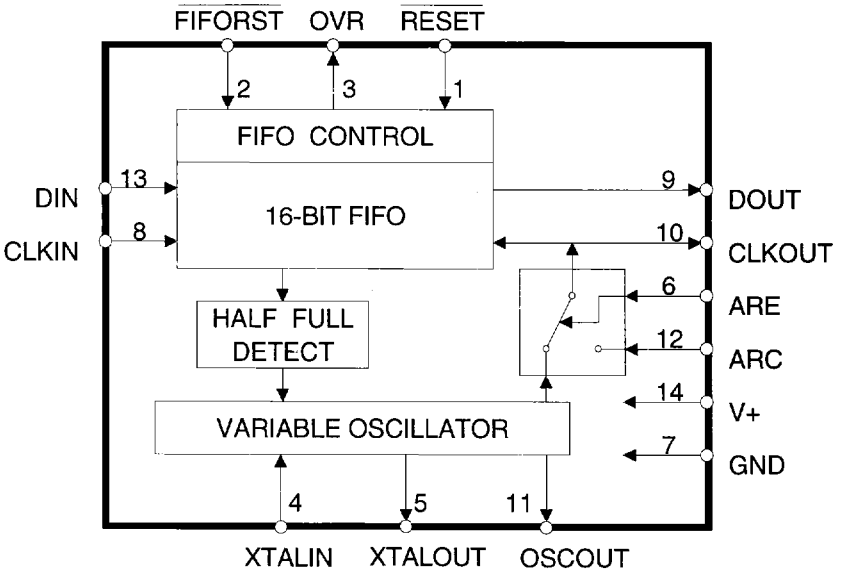

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	(V+)-GND	-	7.0	V
Input Voltage	V_{in}	GND - 0.3	(V+) + 0.3	V
Input Current, Any Pin (Note 1)	I_{in}	-100	100	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	125	°C

Note: 1. Device can tolerate transients of up to 100mA without latching up.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V+	4.5	5.0	5.5	V
Ambient Operating Temperature	T_A	0	25	70	°C
Power Dissipation	P_D	20	50	85	mW
Input Jitter Tolerance		3	-	7	U.I.

DIGITAL CHARACTERISTICS (T_A = 0° to 70° C; V+ = 5V ±10%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 2 and 3)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Notes 2 and 4)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	±10.0	µA

Notes: 2. Outputs will drive CMOS logic levels into a CMOS load.
3. I_{out} = -40 µA
4. I_{out} = 1.6 mA

Specifications subject to change without notice.

SWITCHING CHARACTERISTICS (T_A = 0° to 70° C; V+ = 5V ±10%; GND = 0V;

Inputs: Logic 0 = 0V, Logic 1 = V+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 5)	f_c	4.500	-	8.500	MHz
CLKIN Frequency	(Note 6)	f_{in}	-	f_c	-	MHz
CLKOUT Frequency	(Note 6)	f_{out}	-	f_c	-	MHz
Clock Pulse Width		t_{pwh}	-	$1/(2f_c)$	-	ns
	(Note 7)	t_{pwl}	-	$1/(2f_c)$	-	
Duty Cycle	(Note 8)		-	50	-	%
Rise Time, All Digital Outputs	(Note 9)	t_r	-	36	-	ns
Fall Time, All Digital Outputs	(Note 9)	t_f	-	17	-	ns
DIN to CLKIN Falling Setup Time		t_{su}	30	-	-	ns
CLKIN Falling to DIN Hold Time		t_h	50	-	-	ns
CLKOUT Falling to DOUT Propogation Delay		t_{phl}	-	-	60	ns
$\overline{\text{RESET}}$ Pulse Width			100	-	-	ns
$\overline{\text{FIFOREST}}$ Pulse Width			100	-	-	ns

Note:
5. Crystal must meet specifications described in *Applications* Section of this data sheet.
6. Although CLKIN and CLKOUT will vary in instantaneous frequency (jitter), over time CLKOUT will have the same average frequency as CLKIN.
7. The sum of the pulse widths must always meet the frequency specifications.
8. Duty cycle is (t_{PWH} / (t_{PWH} + t_{PWL})) x 100%.
9. At maximum load of 1.6mA and 50pF.

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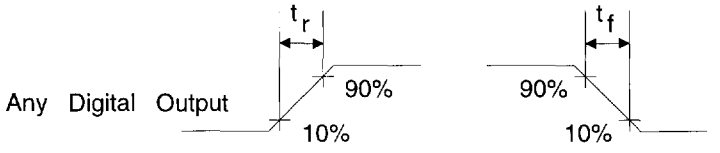

Figure 1. Signal Rise and Fall Characteristics

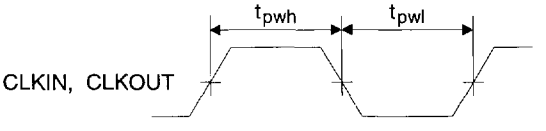

Figure 2. Clock Signal Quality

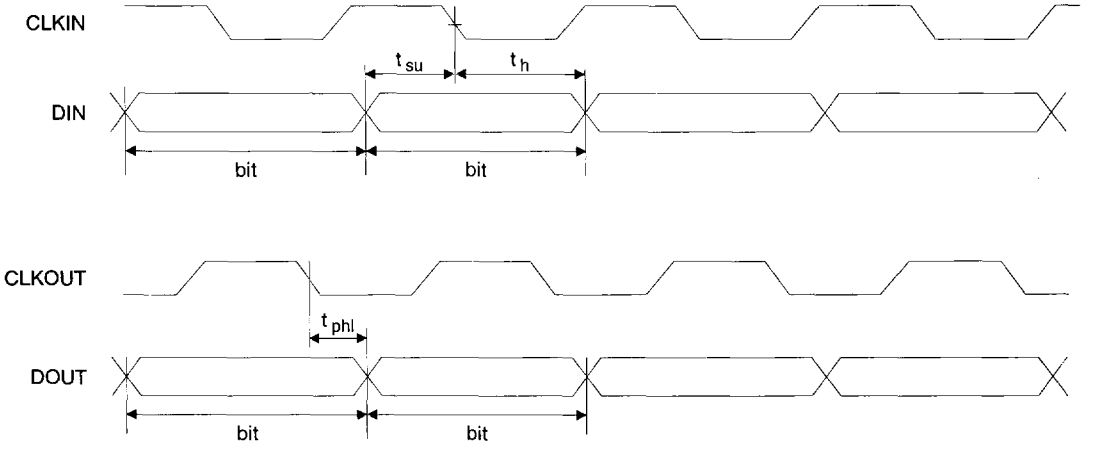

Figure 3. Switching Characteristics

CIRCUIT DESCRIPTION

Jitter Attenuation

The CS80600 will tolerate and attenuate at least three unit intervals of jitter from a 4.5MHz to 8.5MHz data and clock signal. An external clock divide circuit can be added for jitter attenuation for lower frequency signals. Jitter attenuation is accomplished by means of a FIFO and a variable oscillator. The frequency of the oscillator is controlled by logic in the CS80600 to be the same as the average of the input clock signal, CLKIN. Signal jitter is absorbed in the FIFO.

The FIFO's write pointer is controlled by the CLKIN signal. Data present on DIN is written into the memory location selected by the write pointer. The CLKOUT signal corresponds to the FIFO's read pointer and is controlled by the crystal oscillator. Internal logic determines the relationship of the read pointer and the write pointer, and adjusts the speed of the oscillator. For example, if the CLKIN signal is at a higher frequency than the CLKOUT signal, the write pointer will start to catch up with the read pointer. When this situation is detected, the capacitive loading the device presents to the crystal is reduced, resulting in an increase in oscillator frequency and read pointer (CLKOUT) frequency. The oscillator frequency is periodically updated and adjusted to maintain the FIFO at half full. High frequency variations in the phase of the CLKIN signal (jitter) are absorbed in the FIFO.

There are some advantages to this method of jitter attenuation. The device can tolerate large amplitude jitter at high frequencies. The device can track slow changes of the input clock frequency (wander) and tolerate input frequencies ranging over a specified frequency tolerance.

A by product of this method of jitter attenuation is that the greater the input jitter, the greater the jitter attenuation, and the lower the frequency at which the device starts to attenuate jitter. Conversely, low amplitude jitter recieves little attenuation. This performance characteristic is shown graphically in Figure 4.

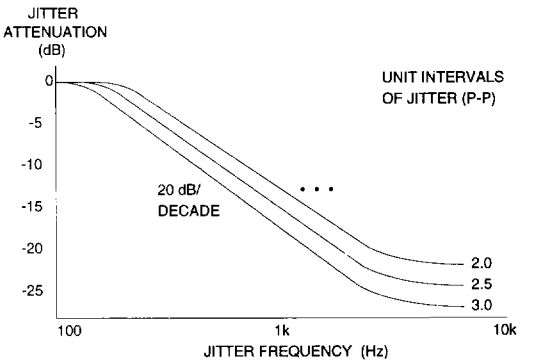

Figure 4 - Jitter Attenuation Characteristics for 8MHz Nominal Frequency

Clock Operation

The CS80600 requires an external crystal. Exacting crystal specifications must be met to ensure proper operation of the curcuit. Information on specifying crystals for the CS80600 is provided in the *Applications* section which appends this data sheet.

It is possible to use an externally generated clock signal to clock data out of the CS80600. The external clock is input to the Alternate Read Clock input, (ARC, pin 12). Holding the Alternate Read Enable pin high (ARE, pin 6), directs the CS80600 to clock data out of the FIFO at the rate determined by ARC. Unless the clock signal on ARC is at exactly the same average frequency as the clock signal on CLKIN, the CS80600 will be prone to underflow or overflow and data will be lost.

FIFO Overflow/Underflow

If underflow or overflow occurs, the buffer overflow/underflow flag, OVR (pin 3), goes high. A $\overline{\text{RESET}}$ (pin 1) resets the overflow flag. If an

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overflow occurs, the eight bits of data in the FIFO are lost. An underflow condition causes the next eight bits read from the FIFO to be invalid. In either case, the CS80600 will immediately attempt to relock on to the clock signal. Holding $\overline{\text{RESET}}$ low disables the OVR flag.

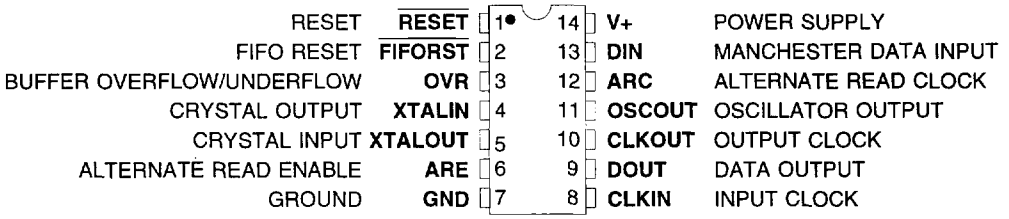
FIFO Reset

Taking the $\overline{\text{FIFORST}}$ pin low causes most of the subcircuits of the CS80600 to go into a reset state. These circuits will remain in a reset condition until $\overline{\text{FIFORST}}$ is returned to a logic 1 state. ***However, the outputs of the CS80600 are undefined if FIFORST is held low for more than 500 ms.*** The FIFO reset function will set the FIFO write and read pointers to the first and fourth locations respectively. The oscillator will continue to run and CLKOUT will continue to be output.

Power-Up Reset

Upon power up, the CS80600 goes through an initialization procedure which requires approximately 3 ms. During power-up reset, the overflow pin, OVR, is held high. When initialization is complete, the OVR pin goes low and the CS80600 is ready to lock on to an input clock signal on CLKIN.

PIN DESCRIPTIONS



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Power Supplies

V+ - Positive Power Supply, PIN 14.
Typically +5V volts.

GND - Ground, PIN 7.
Ground reference.

Oscillator

XTALIN; XTALOUT - Crystal Input; Crystal Output; PINS 4, 5.
A 20 kΩ resistor should be connected across these pins parallel with the crystal. There is no need for external capacitors. The crystal should be connected to XTALIN and XTALOUT with minimal length traces on the pc board.

Control

$\overline{\text{RESET}}$ - Reset, PIN 1.
When $\overline{\text{RESET}}$ is taken low, the OVR signal is reset.

$\overline{\text{FIFORST}}$ - FIFO Reset, PIN 2.
Taking $\overline{\text{FIFORST}}$ low resets the read and write pointers of the FIFO. Resetting the pointers will cause some data loss.

ARE - Alternate Read Enable, PIN 6.
For normal operation, ARE is held at logic 0. In this configuration the oscillator controls the read pointer of the FIFO. When ARE is at logic 1, the read pointer of the FIFO will be controlled by the clock signal on pin 12, ARC.

Inputs

CLKIN - Clock Input, PIN 8.

Clock for the data input. This clock contains the jitter to be removed.

DIN - Data Input, PIN 13.

Data input is sampled on the falling edge of CLKIN.

ARC - Alternate Read Clock, PIN 12.

When ARE, Pin 6, is at logic 1, a clock signal on ARC will control the FIFO's read pointer. CLKOUT, pin 10, will be at the same frequency and phase as ARC. Setting ARE to logic 0 results in the device using its oscillator to generate CLKOUT.

Outputs

OVR - Buffer Overflow/Underflow, PIN 3.

Goes high if the FIFO overflows or underflows, and is cleared by $\overline{\text{RESET}}$.

DOUT - Data Output, PIN 9.

Data output with jitter removed. DOUT is stable and valid on the rising edge of CLKOUT.

CLKOUT - Output Clock, PIN 10.

Jitter free clock output corresponding to the data on DOUT.

OSCOUT - Oscillator Output, Pin 11.

Output of the crystal oscillator.

APPLICATIONS

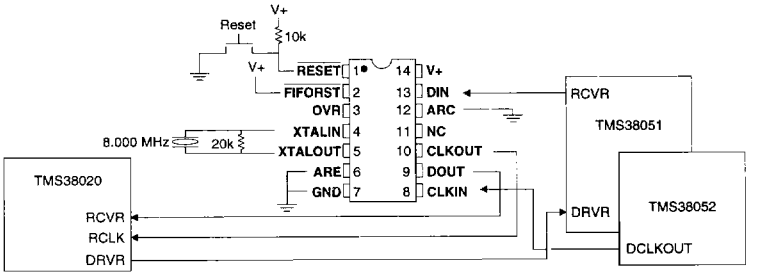

Figure A1. Basic LAN Application suggested for TMS380 Chip Set

Token Ring Operation

The CS80600 can be used, as shown in Figure A1 with the TMS380 Token Ring adaptor chipset in station adaptors, active wiring concentrators and/or repeaters to attenuate jitter that accumulates in a ring. Figure A1 has the effect of masking frequency deviations from the TMS38020 and preventing the "Hardware Error Process" from triggering. In this case, error recovery occurs as the result of higher level procedures.

Figure A2 allows the "Hardware Error Process" to occur. When the CS80600 overflows or underflows, a MUX is used to pass the out-of-frequency clock data around the CS80600 for a fixed number of bits. After those number of bits are passed, the CS80600 is switched back into the circuit. This allows the TMS38020 to observe a wide frequency variation.

Figure A3 shows how the CS80600 can be used to generate a FRAQ signal, thereby allowing the TMS38051/52 PLL to be controlled in a repeater without the use of the TMS38020.

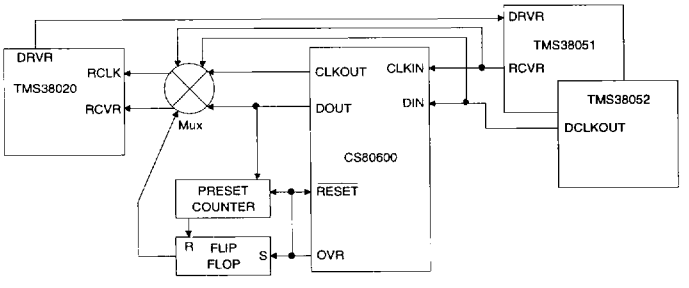

Figure A2. Passing of Frequency Errors

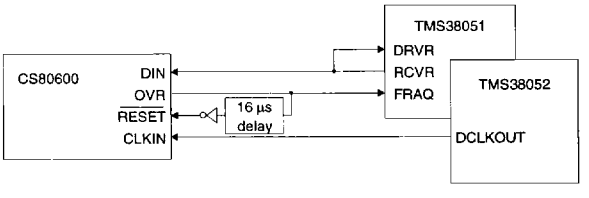

Figure A3. Eliminating TMS38010/20/30 in Repeaters

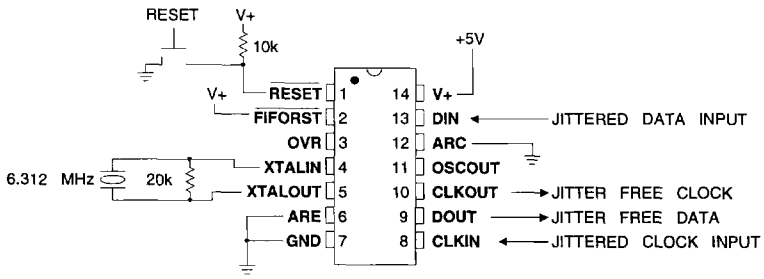

Figure A4. Typical Jitter Attenuation Curcuit

T2 Operation

The CS80600 may be connected as shown in Figure A4 for jitter attenuation in T2 applications.

Selecting an Oscillator Crystal

Figure A5 shows an equivalent representation of the oscillator circuit. The variable load capacitor is internal to the CS80600. The value of this capacitor is controlled by logic internal to the CS80600. Based on this model, equations 1 and 2 have been developed to help calculate the required crystal parameters necessary to meet system requirements.

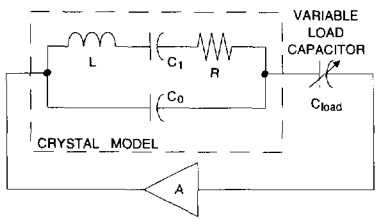

Figure A5. Equivalent Circuit of Oscillator

The important parameters in this model are the upper and lower bounds of C_{load} (the variable load capacitor) and the value of C_0 and C_1. C_1 can be used to control the series resonant frequency of the crystal. The minimum values of C_{load} and C_0 set the parallel resonant frequency. Together, C_1, C_0 and C_{load} can be used to set the pull range of the oscillator and its maximum and minimum frequencies.

Determining Required Pull Range

Four factors contribute to the required pull range of the crystal:

1) The frequency range required for the application.
2) The frequency drift of the crystal over the operating temperature range.
3) The variability in load capacitance from IC to IC.
4) The accuracy to which the crystal can be manufactured.

All of these factors have been measured or can be controlled.

For a given crystal geometry, the series resonant frequency of the crystal is inversely proportional to C_1. The relationship of the crystal's series resonant frequency to its parallel resonant frequency in the oscillator circuit determines the pull range of the oscillator. The further away the series resonant frequency is from the parallel resonant frequency (which is set by the load condition in the oscillator circuit) the greater the pull range of the crystal. That is: a smaller C_1 (greater series resonant frequency) results in less pull range, while the larger the C_1 (lower series resonant frequency), the larger the pull range.

The series resonant frequency of the crystal is calculated by Equation 1.

$$f_S = f_N - \frac{\Delta f}{2(C_L - C_H)} (C_L + C_H + 2C_0) \quad \text{(C's in pF)} \qquad (1)$$

f_S = series resonant frequency of crystal
f_N = Nominal Signal Frequency
- should be 8.000000 MHz for LAN
- should be 6.312000 MHz for T2
- should be 8.448000 MHz for CEPT2

Δf = required pull range of crystal in Hz (Δppm x f_N)
C_L = load capacitance for low frequency oscillation (average is ~44.0 pF)
C_H = load capacitance for high frequency oscillation (average is ~9.5 pF)

The parallel resonant frequency is calculated by Equation 2.

$$f_{load} = f_S \left(\frac{C_1 + C_{load} + C_0}{C_{load} + C_0}\right)^{1/2}$$

Table A1 shows the crystal frequency as a function of load capacitance. The deviation in frequency from the nominal is shown in ppm. Temperature drift has been accounted for as shown. *The accuracy to which C_0 and C_1 can be controlled, and the accuracy to which a crystal can be trained or calibrated should be factored in to guarantee that the required frequency range will be met.*

The setup shown in Figure A6 can be used to test crystals. When no CLKIN signal is applied to the device, the oscillator will tend to pull to one extreme of its pull range. Momentarily pressing the push button moves the relative positions of the FIFO pointers and if the write pointer stops (when the push button opens) in the right relationship to the read pointer, the oscillator will pull to the other end of its range. It may take a few tries.

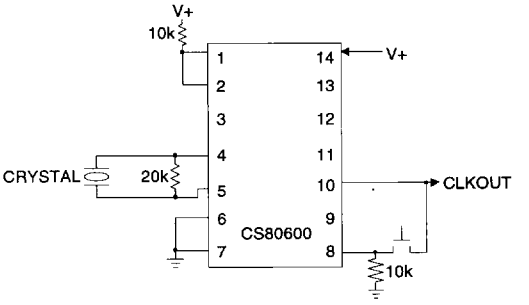

Figure A6. Crystal Pull Range Test

General Applications

The CS80600 will tolerate and attenuate at least three unit intervals of jitter over the specified range of input clock and oscillator frequencies. If the oscillator crystal is chosen so that the center frequency of its pull range is close to the input frequency, CLKIN, the CS80600 will tolerate more jitter; up to seven unit intervals will be tolerated under optimal conditions.

NOMINAL INPUT SIGNAL FREQUENCY
8.000000 MHz

C_L in pf	FREQUENCY TOLERANCE OF INPUT SIGNAL ±100 ppm			
$C_{low\ freq}$ min 41.0	-170 ppm 7998640	$C_{high\ freq}$ max 10.7	+170 ppm 8001360	CRYSTAL FREQUENCY FOR CORRESPONDING LOAD CAPACITANCE
ASSUMING ±50 ppm TEMPERATURE DRIFT FROM 0° - 70° C				
MAXIMUM ALLOWABLE PULL RANGE: 400 ppm				

Table A1. LAN Crystal Requirements

Consider the case where the average clock frequency at CLKIN approaches the slow end of the range, 8.000 MHz - 100 ppm. In this case, the oscillator will be near the bottom of its pull range, restricting its ability to achieve frequencies well below the CLKIN frequency. The result is that the read pointer of the FIFO will begin to catch up to the write pointer. If enough jitter is introduced, the read pointer will overtake the write pointer resulting in an error (i.e. the device will try to read out data before it is written in). A similar situation occurs when the CLKIN signal approaches the fast end of its range, 8.000 MHz + 100 ppm. In either case, the CS80600 will tolerate at least 3 unit intervals of jitter.

Taking care in selecting the proper crystal can result in improved jitter tolerance without degrading the performance of the CS80600. If the center frequency of the oscillator is precisely the CLKIN frequency, and the crystal has at least the specified pull range, the CS80600 will tolerate 7 unit intervals of jitter. In this case, the read and write pointers of the FIFO will maintain optimal separation when the signal is jitter free, allowing the device to tolerate maximum jitter input.

Master/Slave Configuration

Some applications require separate representations of the positive and negative going pulses for an AMI signal. Two CS80600s can be used to remove jitter from a set of signals consisting of POS, NEG and CLK. Figure A7 shows the master/slave configuration.

This configuration requires one crystal (on the master). The CLKOUT signal from the master controls the FIFO read pointer of the slave CS80600. Setting ARE, pin 6, of the slave to logic 1 directs the device to use the clock input to ARC, pin 12, to control the FIFO read pointer. For this configuration to function properly, the positions of the FIFO the read and write pointers in both devices must correspond. The FIFO pointer reset, $\overline{\text{FIFORST}}$, of both devices must be tied together. After the power supplies have stabilized, and the clock has been input at CLKIN, $\overline{\text{FIFORST}}$ should be momentarily pulled low to reset the pointers of both devices. The overflow flags should then be reset by momentarily pulling $\overline{\text{RESET}}$, pin 1, low.

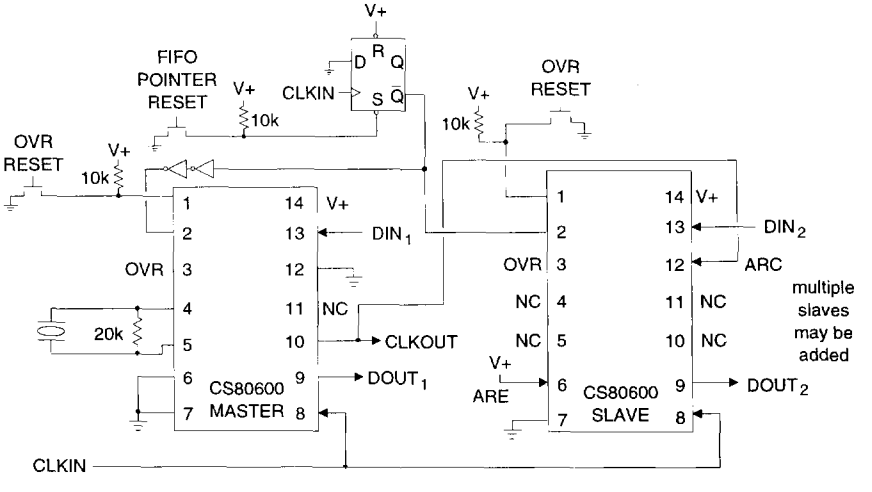

Figure A7. Master/Slave Configuration

Additional slaves may be added. The ARC input may be derived from either the CLKOUT pin on the master, or the CLKOUT pin on a preceding slave. When using the master's CLKOUT pin, the fan out must be considered. Attaching several inputs to the CLKOUT pin increases the load that the output must drive. The added capacitance will reduce the switching speed of the output driver. Similarly, a configuration which uses the CLKOUT signal of each CS80600 to drive the subsequent CS80600 will induce some propagation delay. These potential timing problems should be considered when cascading CS80600s.

Creating Phase Coherent Clocks From Two Clock/Data Streams

The master/slave configuration can be used to align two independent clock/data streams as long as the clocks of both signals are at exactly the same average frequency. The schematic shown in Figure A7 is used to implement this application, but CLKIN signals are independent, not tied together. This application will attenuate jitter as long as the jitter input to either device plus the difference in unit intervals between the clock signals does not exceed seven unit intervals. Note that more jitter can be tolerated if the guidelines described at the beginning of this section are followed.

Maintaining Clock

Many applications require that the clock signal from CLKOUT be maintained within some specified range of frequencies when the clock signal on CLKIN (often generated from a recovered T2 or CEPT2 signal clock) goes away. Figure A8 shows one method for maintaining the CLKOUT signal. The reference clock is a locally generated clock whose frequency lies within the tolerance of the applicable specifications which govern the system's design. When the CLKIN signal goes away, the multiplexor should switch in the reference clock. Since this clock goes through the jitter attenuator, phase and frequency integrity at CLKOUT is maintained.

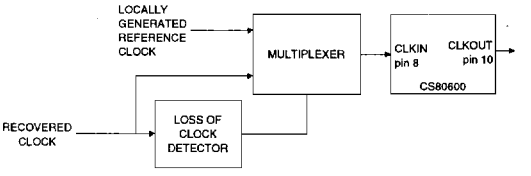

Figure A8. Maintaining Clock Integrity

Jitter Attenuation at Different Clock Rates

The CS80600 can be used to attenuate jitter at frequencies below 4.5 MHz. For signal frequencies above about 4.5 MHz, selection of the appropriate crystal will suffice. For jitter attenuation of lower frequency signals, an external divider is required. Figure A9 shows how the CS80600 can be configured for low frequency jitter attenuation.

Frequency tolerance of the input signal is still based on the pull range of the crystal in ppm. For example, a 64 kbps jitter attenuator which uses an external divide by 128, and a 8.192 MHz crystal with ± 200 ppm pull range will have ± 200 ppm tolerance at 64 kbps or ± 12.8 Hz.

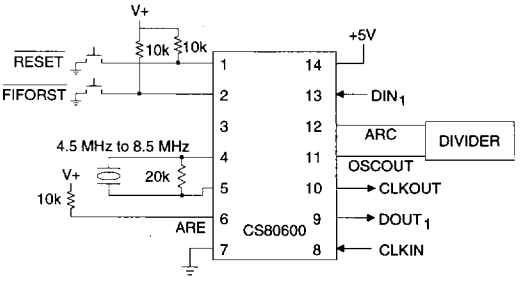

Figure A9. Low Frequency Jitter Attenuation