TEXAS INSTRUMENTS

ADS5410 EVM

User's Guide

June 2002 *AAP High-Speed Data Converter (Dallas)*

SLAU082

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 40°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide is to assist the user with the operation of the EVM using the ADS5410 devices.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1—Overview
- ❏ Chapter 2—Physical Description
- ❏ Chapter 3—Circuit Description

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

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Notes, Cautions, and Warnings

Chapter 1

Overview

This user's guide gives a general overview of the ADS5410 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module.

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1.1 Purpose

The ADS5410 EVM provides a platform for evaluating the ADS5410 analog-to-digital converter (ADC) under various signal, reference, and supply conditions. Use this document in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Analog input to the ADC is provided via two external SMA connectors. The single-ended input the user provides is converted into a differential signal at the input of the device. One input uses a differential amplifier, while the other input is transformer coupled.

The EVM provides an external SMA connection for input of the ADC clock. The user can send this clock to the output connector with the digital data or provide a second clock source to be sent in place of the ADC clock. This allows the user to provide the required setup and hold times of the output data with respect to the output clock. See the *Clock Inputs* section for the proper configuration and operation.

Digital output from the EVM is via a 40-pin connector. The digital lines from the ADC are buffered before going to this connector. More information on this connector can be found in the ADC output section.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the analog and digital supply.

1.3 Power Requirements

The EVM can be powered directly with only a 1.8-V and 3.3-V supply if using the module with a transformer coupled input and an internal reference source.

A voltage of ±5 V is required if using the differential amplifier input. Provision has also been made to allow the EVM to be powered with independent analog, digital, and I/O supplies to provide higher performance.

Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

1.4 ADS5410 EVM Operational Procedure

The ADS5410 EVM provides a flexible means of evaluating the ADS5410 in a number of modes of operation. A basic setup procedure that can be used as a board confidence check is as follows:

1) Verify all jumper settings against the schematic jumper list in Table 1–1 and Table 1–2:

Table 1–1. Two Pin Jumper List

Jumper	Function	Installed	Removed	Default
W10	N/A			Removed
W11	N/A			Removed
R37	Positive analog input	Transformer coupled	No connection	Installed
R39	Negative analog input	Transformer coupled	No connection	Installed
R36	Positive analog input	Differential amplifier	No connection	Removed
R38	Negative analog input	Differential amplifier	No connection	Removed
R43, R44	Output clock option	ADC clock at output connector	Buff clock at output connector	Removed
R62	Optional output clock parallel termination	Provides pullup termination	No pullup termination	Removed
R40	Single-ended clock option	Single-ended clock to ADC	Differential clock input to ADC	Removed

Table 1–2. Three Pin Jumper List

Jumper	Function	Location: Pins 1–2	Location: Pins 2–3	Default
W3	Transformer and diff amp common mode select	ADC output common mode voltage	N/A	1–2
W6	Power-down select	Power-down mode	Operate mode	2–3
W1	Reference select	N/A	Internal reference	2–3

2) Connect supplies to the EVM as follows:
   - 1.8-V digital supply to J9 and return to J10
   - 3.3-V driver supply to J13 and return to J14
   - 3.3-V analog supply to J6 and return to J5
3) Switch power supplies on.
4) Use a function generator with 50-Ω output to input a 80-MHz differential sine wave, 0-V offset, 1 $V_{(p-p)}$ to 6 $V_{(p-p)}$. To provide the ADC clock, connect the positve output into J3 and the negative output into J16.

Note:

The frequency of the clock must be within the specification for the device speed grade.

5) Use a function generator with 50-Ω output to input a 1.5-V offset, 3-$V_{(p-p)}$ amplitude square wave signal into J4 to be used as the buffered output clock.

Note:

This signal must be the same frequency and synchronized with the ADC clock.

6) Use a frequency generator with 50-Ω output to input a 17-MHz, 0-V offset, 1.5-$V_{(p-p)}$ amplitude sine wave signal into J2. This provides a transformer coupled differential signal to the ADC.

7) The digital pattern on the output connector J15 now represents a sine wave and can be monitored using a logic analyzer.

Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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2.1 PCB Layout

The EVM is constructed on a 4-layer, 104 mm (4.1 inch) x 114 mm (4.5 inch) x 1,57 mm (0.062 inch) thick PCB using FR–4 material. Figure 2–1 through Figure 2–4 show the individual layers.

Figure 2–1. Top Layer

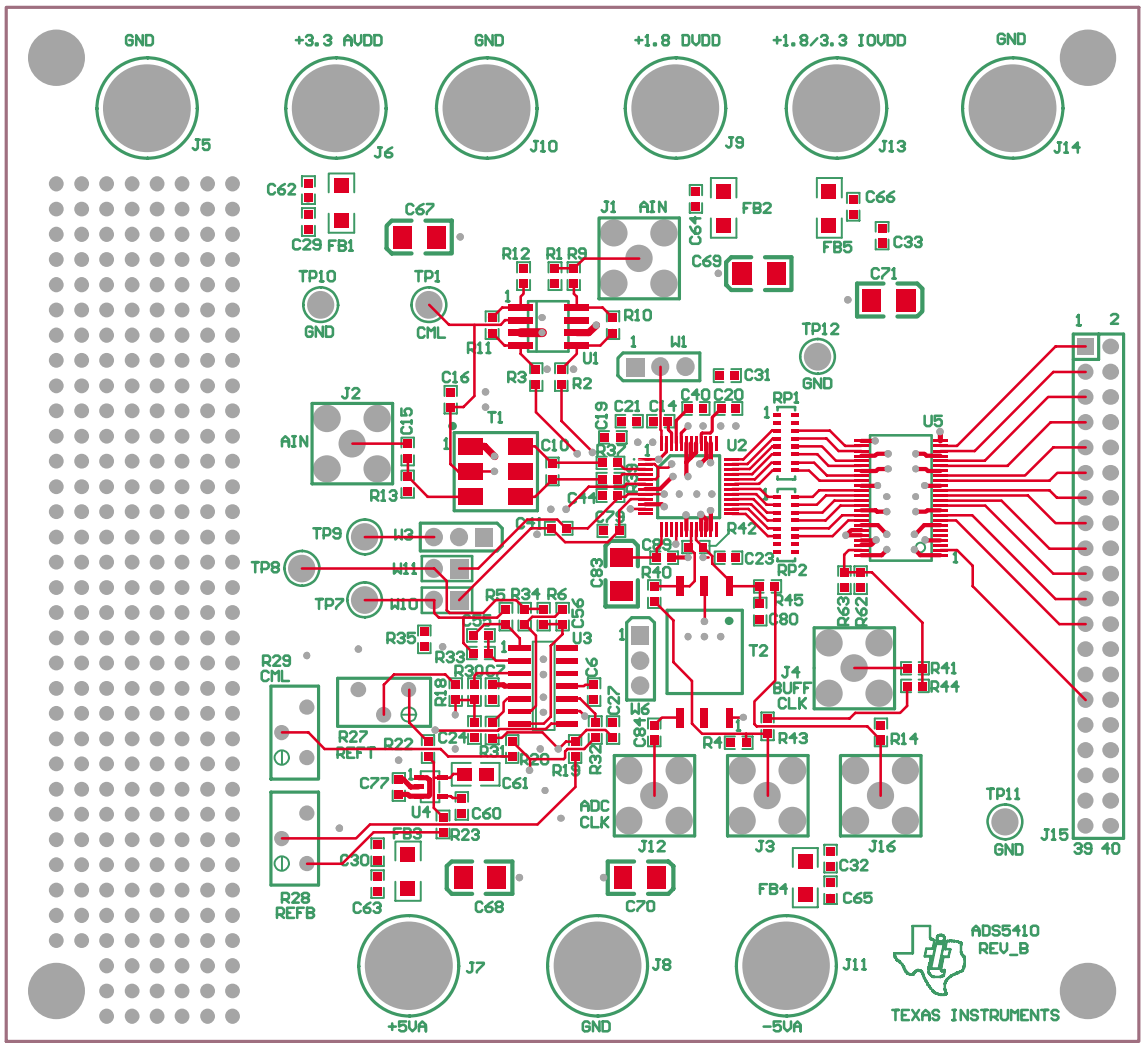


Figure 2–2. Inner Layer 1, Ground Plane

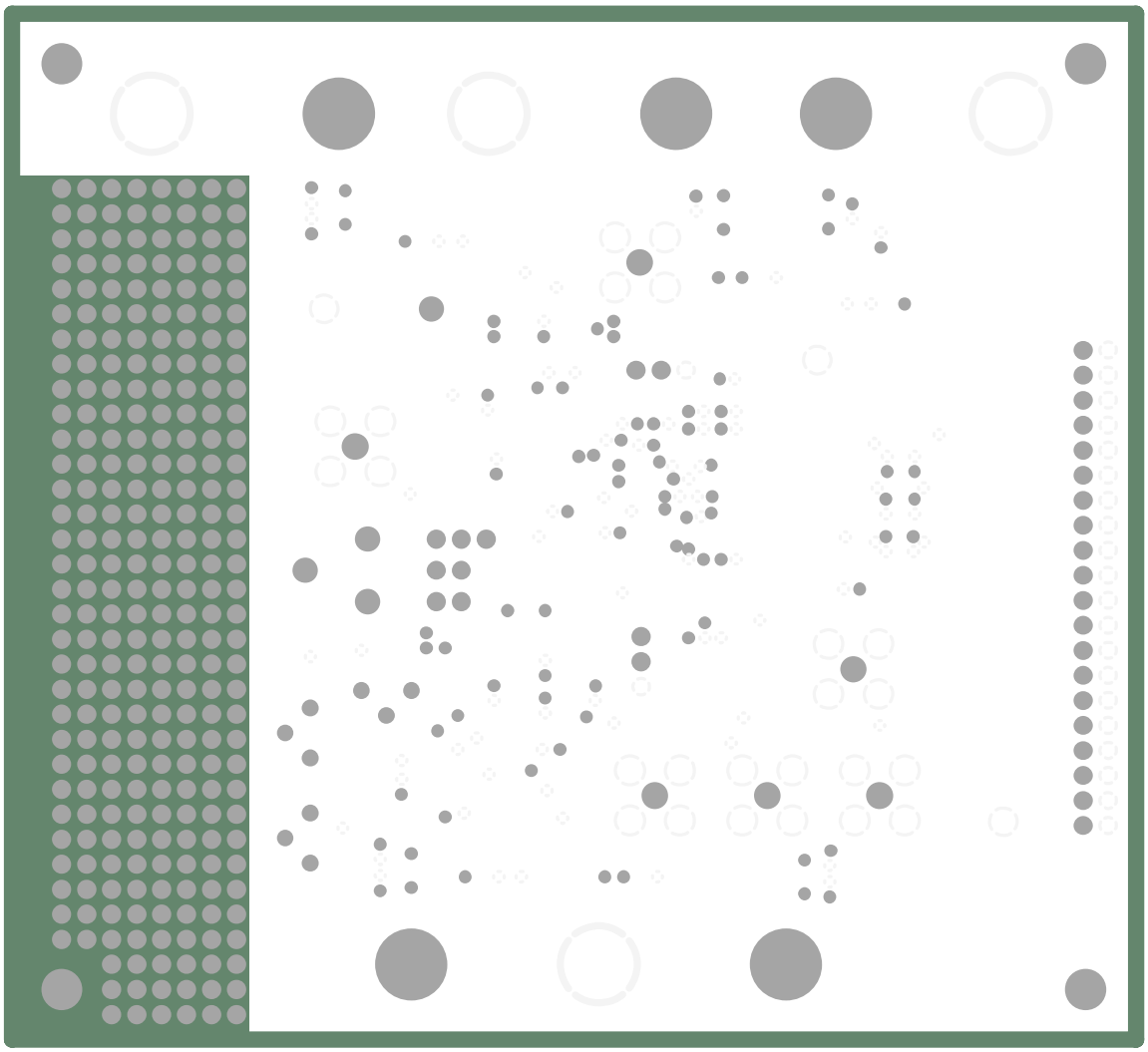


Figure 2–3. Inner Layer 2, Power Plane

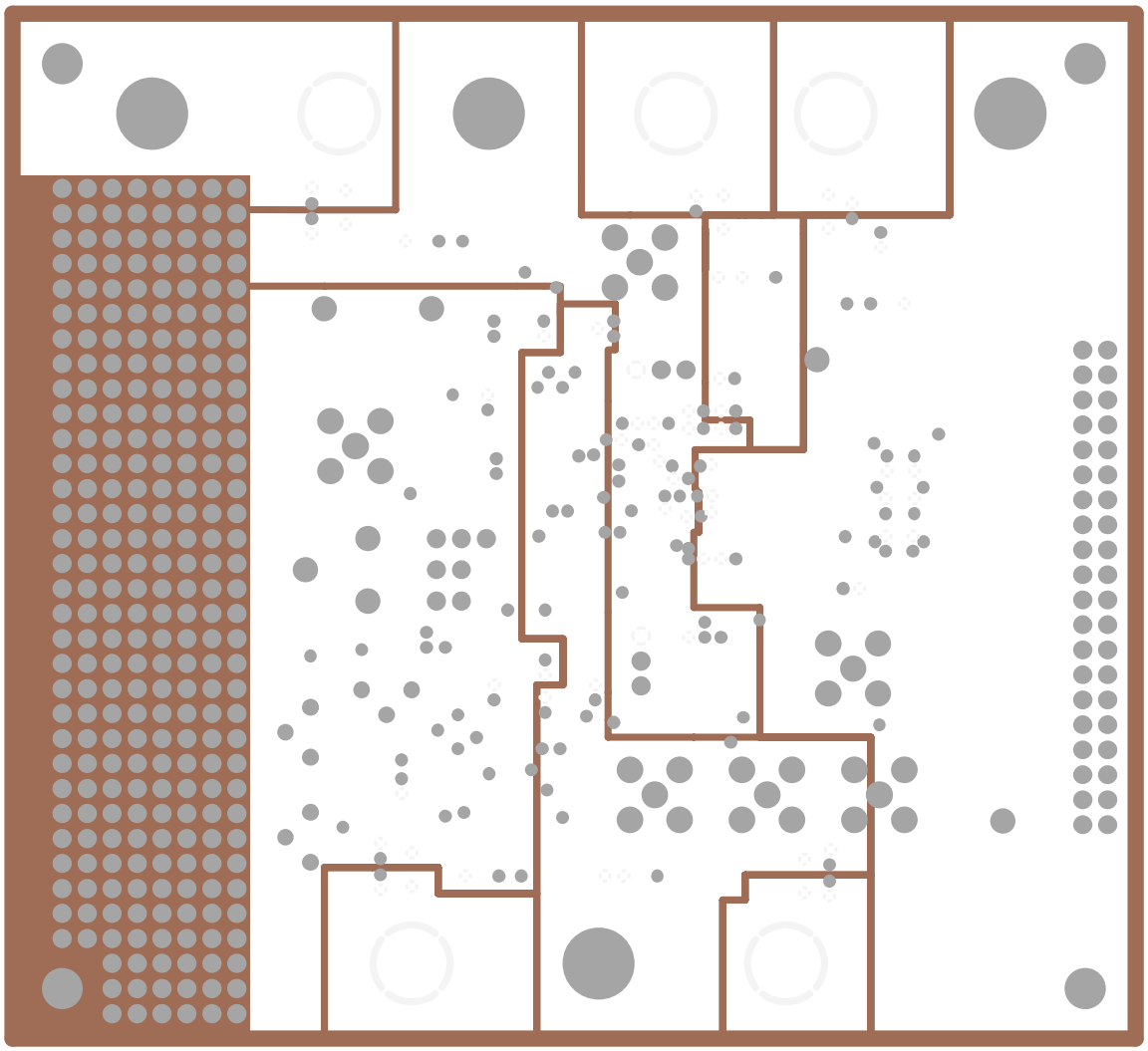
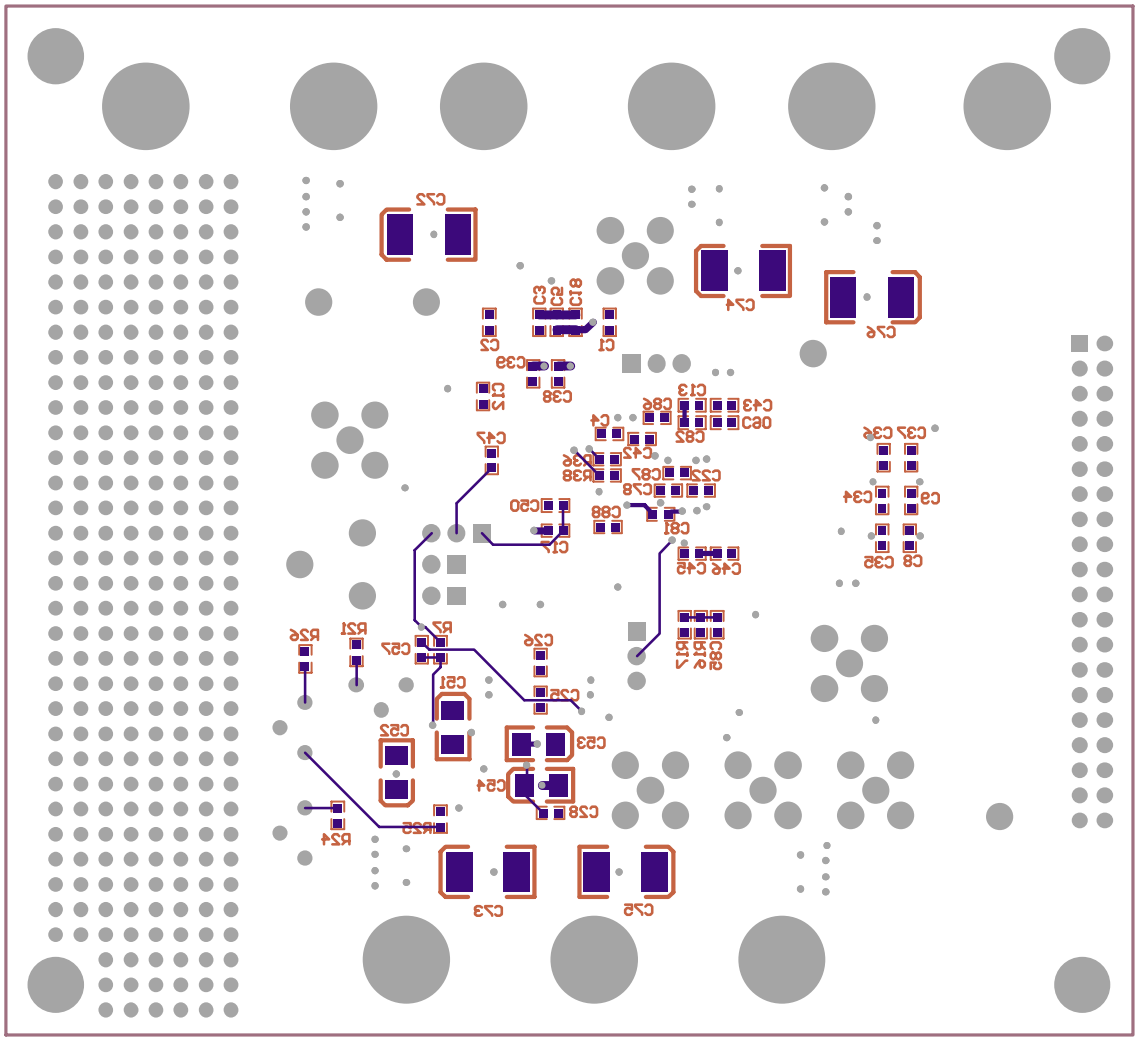


Figure 2–4. Bottom Layer



2.2 Bill of Materials

Table 2–1 lists the parts used in constructing the EVM.

Table 2–1. Bill of Materials

Description	QTY	Part Number	MFG	REF DES	Not Installed
47 μF, 10 V, 10% tantalum capacitor	5	10TPA47M	Sanyo	C72–C76	
0.1 μF, 16 V, 10% capacitor	36	ECJ–1VB1C104K	Panasonic	C4, C8, C9, C12, C14–C20, C22, C23, C29–C37, C41, C44, C47, C62–C66, C81, C85, C86–C89	C24–C28,C80
10 μF, 10 V, 10% capacitor	6	GRM42X5R106K10	Murata	C67–C71, C83	C51–C54
0.01 μF, 50 V, 10% capacitor	13	06035A103KATZA	AVX	C13, C21, C40, C42, C43, C45, C46 C50, C78, C79, C82, C84, C90	C60
1 μF, 10 V, 10% capacitor	0	ECJ-1VF1A105Z	Panasonic		C77
22 pF, 50 V, 5%, capacitor	2	PCC220ACVCT	AVX	C38, C39	
0.047 μF, 50 V, 10% capacitor	0	PCC1758CT	Panasonic		C55, C56, C57
12 pF, 50 V, 10%	1	PCC12ACVCT	Panasonic	C10	
2 pF, 16 V, 10% capacitor	2	ECU-V1H020CCV	Panasonic	C1, C2	
470 pF, 50 V, 10% capacitor	2	PCC471BVCT	Panasonic	C3, C5	C6, C7
2.2 μF, 16 V, 10% capacitor	0	PCC1851CT	Panasonic		C61
Ferrite bead	5	D01608C-472	Coil Craft	FB1–FB5	
100-Ω resistor, 1/16 W, 1%	0	ERJ-3EKF1000V	Panasonic		R30, R31, R32
392-Ω resistor, 1/16 W, 1%	2	ERJ–3EKF392R0V	Panasonic	R10, R11	
374-Ω resistor, 1/16 W, 1%	1	ERJ–3EKF374R0V	Panasonic	R9	
402-Ω resistor, 1/16 W, 1%	1	ERJ–3EKF402R0V	Panasonic	R12	
499-Ω resistor, 1/16 W, 1%	0	ERJ–3EKF499R0V	Panasonic		R22
2.87-kΩ resistor, 1/16 W, 1%	0	ERJ–3EKF2871V	Panasonic		R23
2.55-kΩ resistor, 1/16 w, 1%	0	ERJ-3EKF2551V	Panasonic		R24
4.99-kΩ resistor, 1/16 w, 1%	0	ERJ-3EKF4991V	Panasonic		R26
56.2-Ω resistor, 1/16 W, 1%	1	ERJ–3EKF56R2V	Panasonic	R1	
49.9-Ω resistor, 1/16 W, 1%	6	ERJ–3EKF49R9V	Panasonic	R2–R4, R13, R14, R63	R5, R6, R7, R42
5.62-kΩ resistor, 1/16 w, 1%	0	ERJ-3EKF5621V	Panasonic		R21
10-Ω resistor, 1/16 W, 10%	2	ERJ-3EKF10R0V	Panasonic	R37, R39	
10-kΩ resistor, 1/16 W, 1%	0	ERJ-3EKF1002V	Panasonic		R18, R19, R20
1-kΩ resistor, 1/16 W, 1%	0	ERJ-3EKF1001V	Panasonic		R16, R17
2-kΩ resistor, 1/16 W, 1%	0	ERJ-3EKF2001V	Panasonic		R25, R33, R34, R35

Description	QTY	Part Number	MFG	REF DES	Not Installed
0-Ω resistor, 1/16 W, 1%	1	ERJ–3EKF0R00V	Panasonic	R41	R36, R38, R40, R43, R44, R45, R62
1K Pot	0	3296Y–102	Bourns		R27, R28, R29
Transformer	1	ADT1–1WT		T1	
Transformer	0	T1–6T–KK81	Mini-Circuits		T2
SMA connectors	6	713–4339 (901–144–8RFX)	Allied	J1, J2, J3, J4, J12, J16	
Black test point	3	5011K	Keystone	TP10, TP11, TP12	
Red test point	1	5000K	Keystone	TP1	TP7, TP8, TP9
2POS header	0	TSW–150–07–L–S	Samtec		W10, W11
3POS header	3	TSW–150–07–L–S	Samtec	W1, W3, W6	
2-circuit jumpers	3	863–3285	Allied (molex)		
40-pin header	1	TSW–120–07–L–D	Samtec	J15	
Red banana jacks	5	ST–351A	Allied	J6, J7, J9, J11, J13	
Black banana jacks	4	ST351B	Allied	J5, J8, J10, J14	
ADS5410	1	ADS5410PFB	TI	U2	
TPS79225	0	TPS79225DBVR	TI		U4
100-Ω R-pack	2	742C163101JCT	Bourns	RP1, RP2	
SN74AVC16244DGG	1	SN74AVC16244DGG	TI	U5	
THS4503	1	THS4503ID	TI	U1	
OPA4227UA	0	OPA4227UA	TI		U3
Stand off hex (1/4” x 1”)	4	219–2063	Allied		

Chapter 3

Circuit Description

This chapter describes the circuit function and shows the schematic for the EVM.

Topic **Page**

3.1 Circuit Function

The following paragraphs describe the function of the individual circuits. See data sheet for device operating characteristics.

3.1.1 Analog Inputs

The ADC has either transformer-coupled inputs or differential-amplifier inputs from a single-ended source. The inputs are provided via the SMA connectors J1 and J2 on the EVM, which must be configured as follows:

- For a 1:1 transformer coupled input to the ADC, a single ended source is connected to J2. R36 and R38 must be removed, and R37 and R39 must be installed. The input is ac-coupled and has a 50-Ω terminator. This is the EVM initial configuration.
- For a differential amplifier input to the ADC, a single ended source is connected to J1. R36 and R38 must be installed, and R37 and R39 must be removed. The input has a 50-Ω terminator.

3.1.2 Clock Inputs

The EVM provides separate inputs for the ADC clock and output buffer clock. This allows the user to send a modified version of the ADC clock (inverted, delayed, etc.) with the output data to generate the required setup and hold times for the user interface.

3.1.2.1 Differential ADC Clock

The initial configuration of this EVM converts a single-ended input clock into a differential clock using transformer T2. To provide a true differential ADC clock, configure the board as follows:

1) Install J3, J16, R40, and R45.
2) Remove T2 and R42.
3) Connect the positive clock input to J3 and the negative clock input to J16.

3.1.2.2 Single-Ended ADC Clock

To provide a single-ended ADC clock, configure the EVM as follows:

1) Install J3, R40, and C80.
2) Remove T2, R42, and R45.
3) Apply the clock input to the SMA connector J3.

3.1.2.3 Buffer Clock

To provide a clock to the output buffer, apply a clock input to J4. To provided the single-ended ADC clock to the output buffer do the following:

1) Insert R43 and R44.

2) Remove R41.

3) Install R62 if a pull-up resistor is desired.

Since the input clock will now be terminated at both loads, the clock signal amplitude should be adjusted to provide the appropriate levels at the loads.

3.1.3 Control Inputs

The ADC has one discrete input to control the operation of the device.

3.1.3.1 Power Down

With jumper W6 installed between pins 1 and 2, the ADC is in power-down mode. The device is in operate mode with jumper W6 installed between pin 2 and pin32.

3.1.4 Power

Power is supplied to the EVM via banana jack sockets. A separate connection is provided for a 3.3-V analog supply (J6 and J5), a 1.8-V digital supply (J9 and J10), a 1.8/3.3-V digital driver supply (J13 and J14), and a ±5-V analog supply (J7, J8, and J11).

3.1.5 Outputs

The data outputs from the ADC are buffered using a SN74AVC16244 before going to header J15. The ADC and output buffer can provide 1.8-V or 3.3-V output levels. The voltage placed at the driver power inputs (J13 and J14) selects this. J15 is a standard 40-pin header on a 100-mil grid, and allows easy connection to a logic analyzer. The connector pin out is listed in Table 3–1.

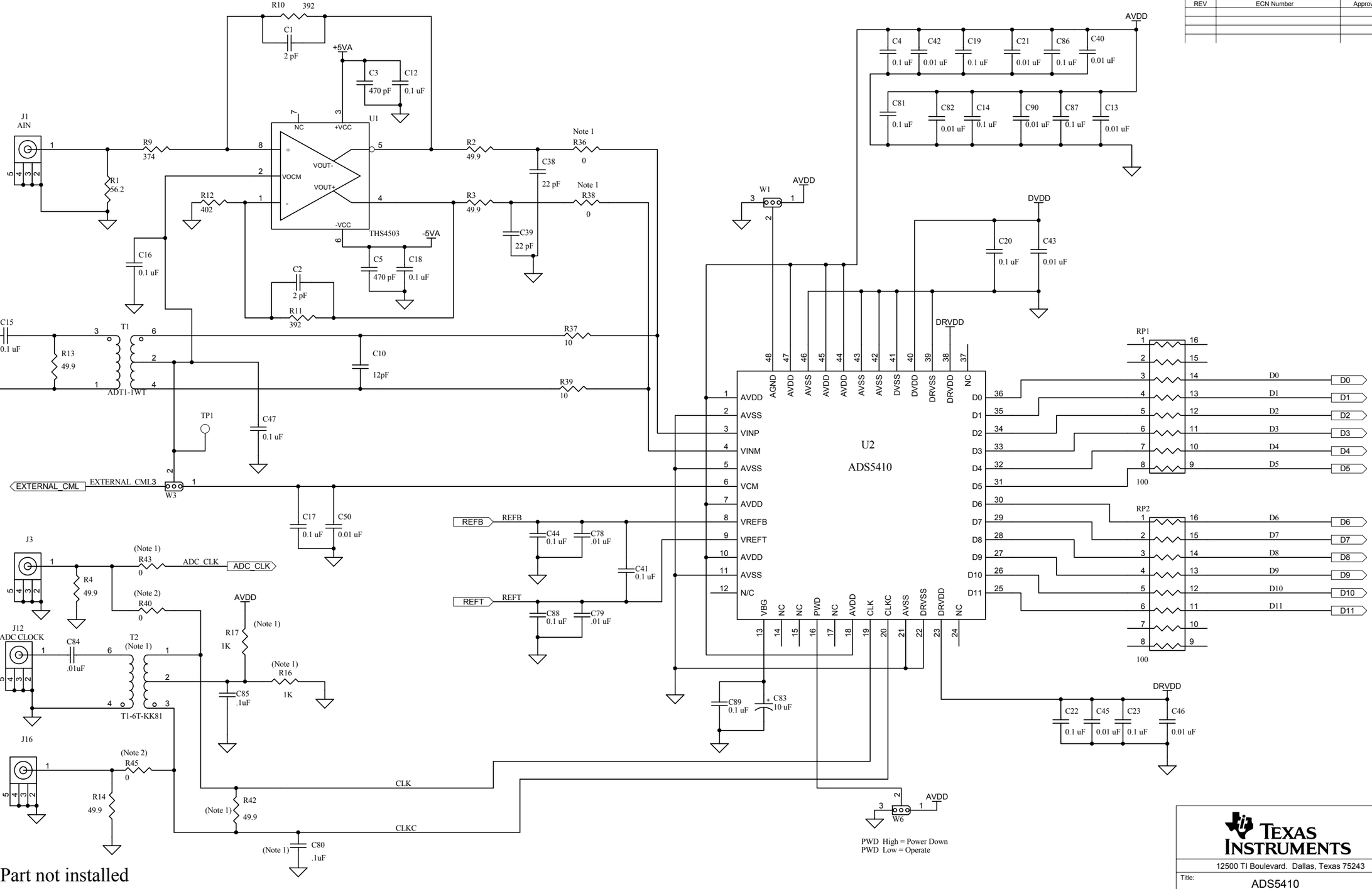
Table 3–1. Output Connector J15

J15 Pin	Description	J15 Pin	Description
1	Data bit 0 (LSB)	21	Data bit 10
2	GND	22	GND
3	Data bit 1	23	Data bit 11
4	GND	24	GND
5	Data bit 2	25	NC
6	GND	26	GND
7	Data bit 3	27	NC
8	GND	28	GND
9	Data bit 4	29	Output clock
10	GND	30	GND
11	Data bit 5	31	NC
12	GND	32	GND
13	Data bit 6	33	NC
14	GND	34	GND
15	Data bit 7	35	NC
16	GND	36	GND
17	Data bit 8	37	NC
18	GND	38	GND
19	Data bit 9	39	NC
20	GND	40	GND

3.2 Schematic Diagram

The following figures show the schematic diagram for the EVM.

Revision History		
REV	ECN Number	Approved



Note 1. Part not installed

Note 2. Part replaced with 0.1 uF capacitor for true differential clock option

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Drawn By: Y. DEWONCK	DOCUMENTCONTROL# 6435809		REV: A
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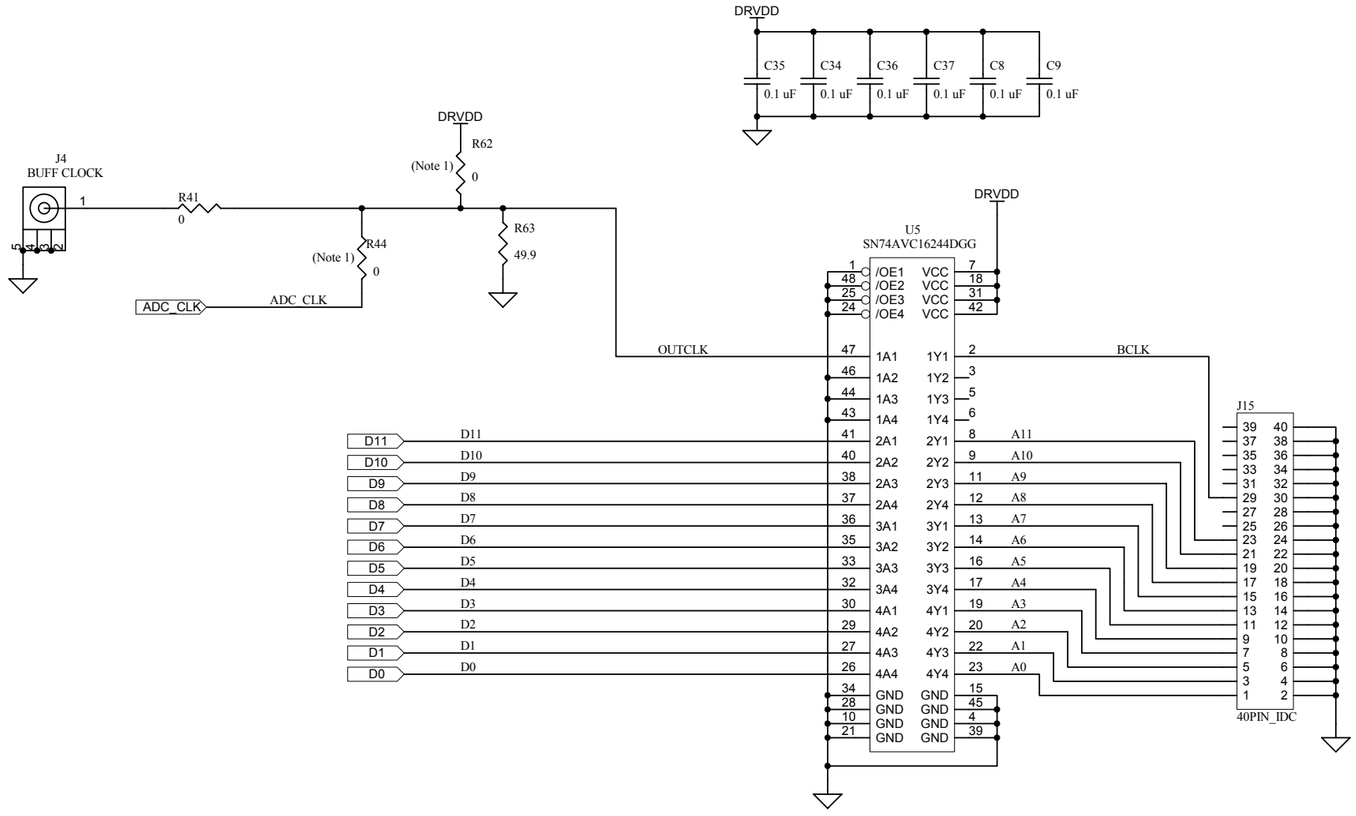

Note 1. Part not Installed

Engineer: J. SETON	
Drawn By: Y. DEWONCK	
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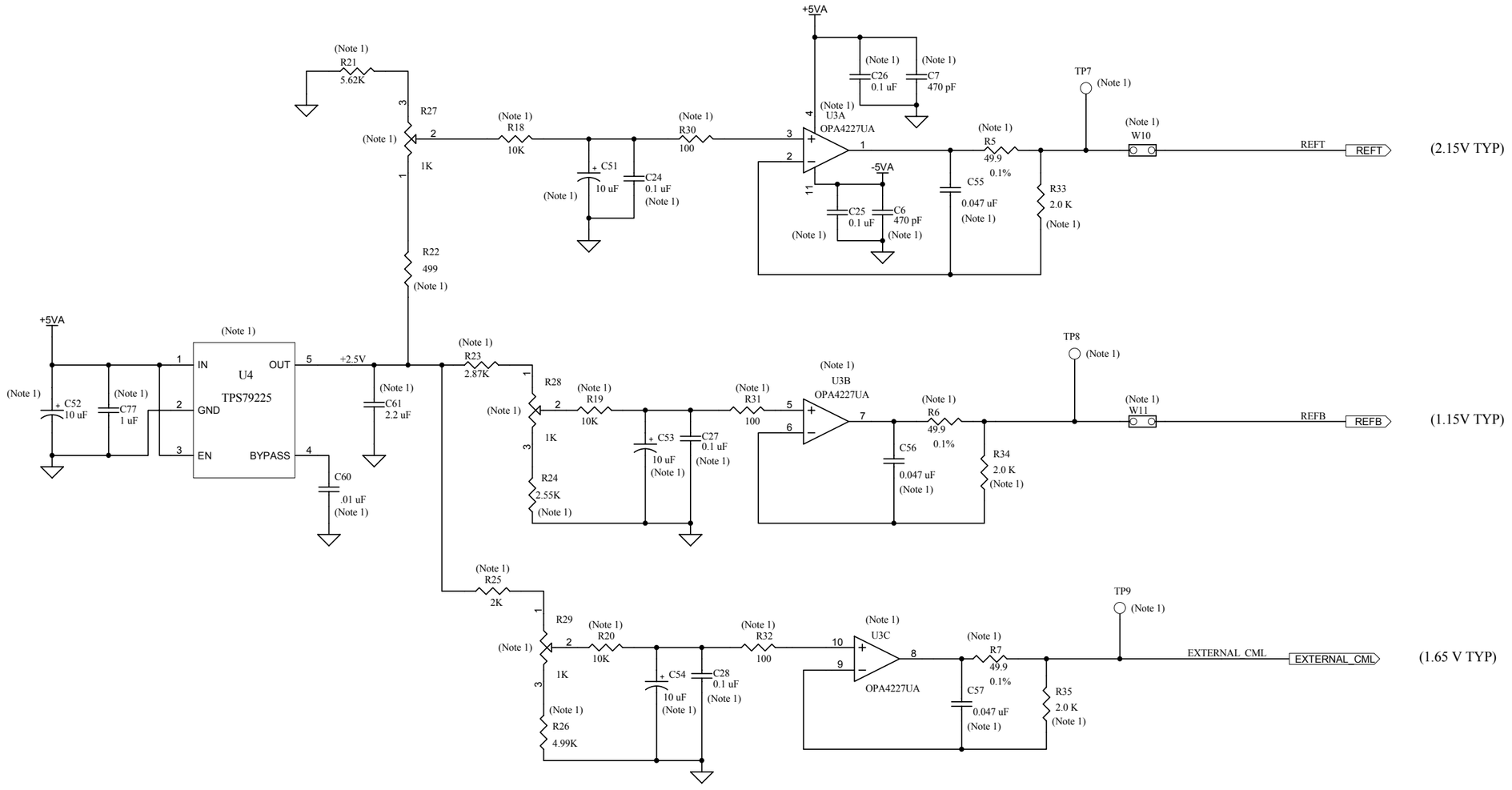

Note 1. Part not installed

Engineer:	J. SETON
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FILE:	

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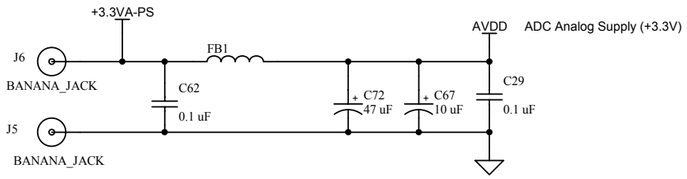

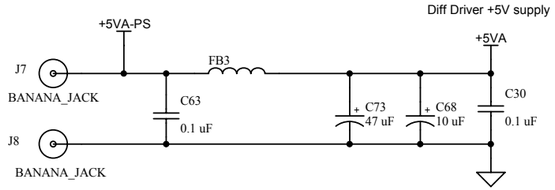

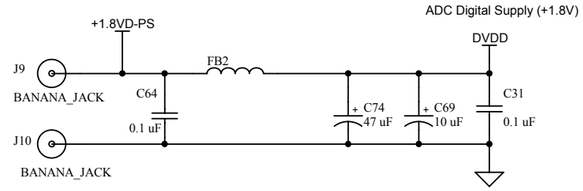

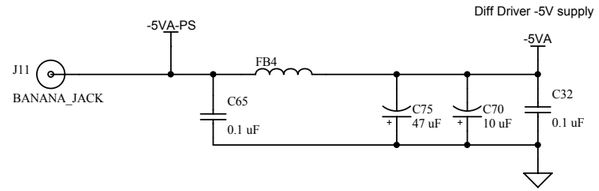

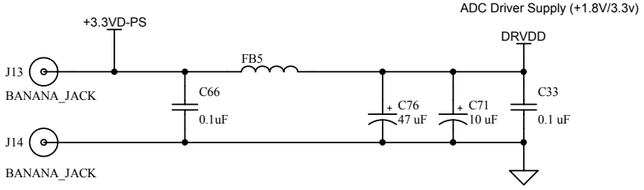

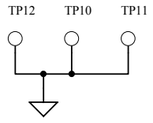

Engineer: J. SETON			
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