TPS4334xEVM Evaluation Module

The Texas Instruments TPS4334xEVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS4334x Switch-Mode Power Supply, Multiple-Output Voltage Regulator. This document describes the setup and the input/output connections of the EVM. Included are the board layout, bill of materials, and schematic.

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1 Introduction

The Texas Instruments TPS4334xEVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS4334x Switch-Mode Power Supply, Multiple-Output Voltage Regulator (see Table 1). The EVM contains one dc/dc converter/controller.

Table 1. Device and Package Configurations

CONVERTER	IC	PACKAGE
U1	TPS43340QPHPQ1	PHP-48
	TPS43341QPHPQ1	

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS43340EVM.

2.1 Input/Output Connector Description

J1 – **Output** is the output terminal for the TPS43340x linear regulator. The terminal block provides a power (VOUT4) and ground (GND) connection.

J2 – **Input** is the power input terminal for the device. The terminal block provides a power (Vbat) and ground (GND) connection that allows the user to attach the EVM to a cable harness.

J3 – **Output** is the output terminal for the TPS4334x switch-mode regulator 3. The terminal block provides a power (VOUT3) and ground (GND) connection.

J4 – **Output** is the output terminal for the TPS4334x switch-mode regulator 1. The terminal block provides a power (VOUT1) and ground (GND) connection.

J5 – **Output** is the output terminal for the TPS4334x switch-mode regulator 2. The terminal block provides a power (VOUT2) and ground (GND) connection.

J6 – **Input** is the power input terminal for switch-mode regulator 3. The terminal block provides a power (Vsup) and ground (GND) connection that allows the user to attach the EVM to a cable harness. Vsup must not exceed 10 V.

JP1 – **PGATE** is the jumper used to enable PMOS FET in the power path. The jumper allows the FET to be forced off or controlled by the GPULL output of the device

Figure 1. PGATE Jumper Setting

JP2 – **EXTSUP** is the jumper used to select the optional power supply for the source and sink circuitry that control the gate drives to the FETs. The jumper selects the output of the switch-mode regulator 1 or switch-mode regulator 2. If the jumper is removed and EXTSUP is tied to GND, the gate driver is supplied from VIN.

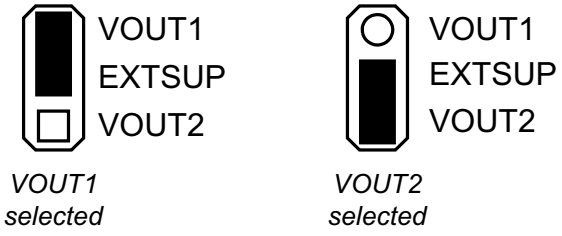

Figure 2. EXTSUP Jumper Setting

JP3 – **VINLR1** is the jumper used to select the power supply source for the linear regulator. The jumper selects the output of the switch-mode regulator 1 or the protected battery input (VIN). The user can leave the jumper open and use an external supply via the VINLR1 test point.

Figure 3. VINLR1 Jumper Setting

JP4 – **VIN2** is the jumper used to select the power supply source for the switch-mode regulator 2. The jumper selects the output of the switch-mode regulator 1 or the protected battery input (VIN).

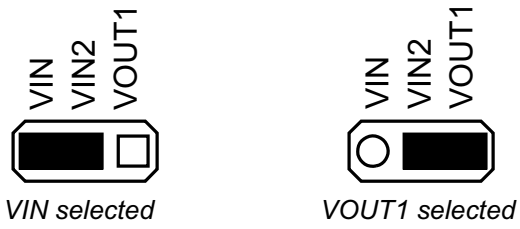

Figure 4. VIN2 Jumper Setting

JP5 – **VSUP** is the jumper used to select the power supply source for the switch-mode regulator 3. The jumper selects the output of the switch-mode regulator 1 or the VSUP input (J6).

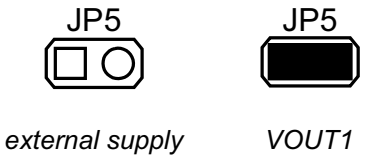

Figure 5. VSUP Jumper Setting

JP6 – **ROSC** is the jumper used to select the operating switching frequency for the switch-mode regulators. The jumper places a pulldown resistor in the circuit to set the frequency to approximately 240 kHz, 400 kHz, or 600 kHz.

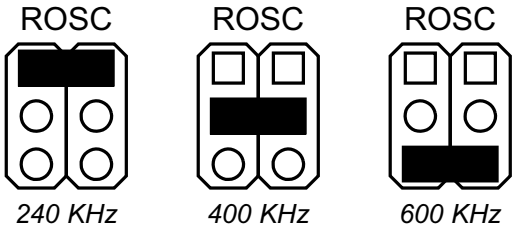

Figure 6. ROSC Jumper Settings

JP7 – **DELAY** is the jumper used to set power-on reset delay. The jumper places a capacitor in the circuit to set the delay to approximately 1 ms, 10 ms, or 100 ms.

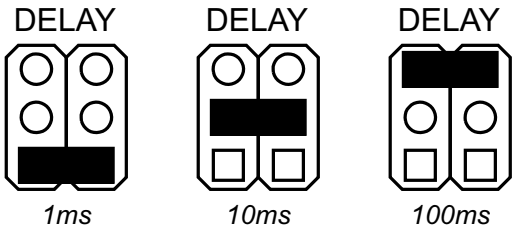

Figure 7. Delay Jumper Settings

JP8 – **EN1** is the jumper used to enable the switch-mode converter 1. The converter is enabled when the EN1 is high and disabled when low.

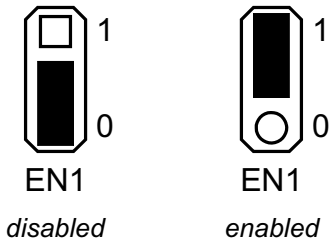

Figure 8. EN1 Jumper Setting

JP9 – **EN2** is the jumper used to enable the switch-mode converter 2. The converter is enabled when the EN2 is high and disabled when low.

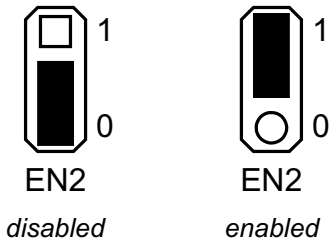

Figure 9. EN2 Jumper Setting

JP10 – **EN3** is the jumper used to enable the switch-mode converter 3. The converter is enabled when the EN3 is high and disabled when low.

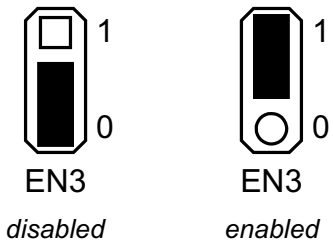

Figure 10. EN3 Jumper Setting

JP11 – **EN4** is the jumper used to enable the linear regulator. The regulator is enabled when the EN4 is high and disabled when low.

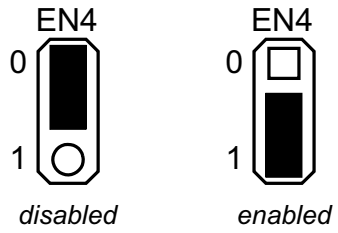

Figure 11. EN4 Jumper Setting

JP12 – **SLEW** is the jumper used to set the slew rate for the integrated high-side power MOSFET of switch-mode converter 3. The slew rate can be set to slow, medium, or fast.

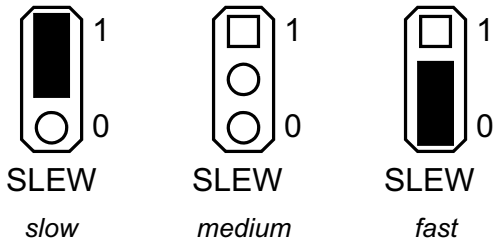

Figure 12. SLEW Jumper Setting

JP13 – **SYNC** is the external clock input for switching frequency synchronization of the buck converters and to enable Low Power Mode (LPM). The external clock source can be attached to the center pin of JP13. A high logic level on this pin ensures forced continuous mode operation of the buck controllers and inhibits transition to low power mode. An open or low allows discontinuous mode operation, and entry into low power mode at light loads. On the TPS43341, a high level enables frequency-hopping spread spectrum while an open or a low level disables the spectrum.

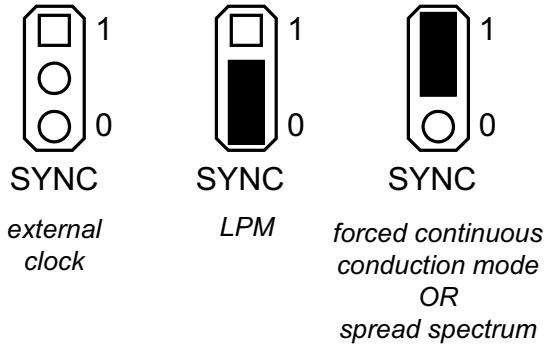

Figure 13. SYNC Jumper Setting

The following listing describes the functions of the various test points.

Test Points

- EN1 Enable for switcher 1
- EN2 Enable for switcher 2
- EN3 Enable for switcher 3
- EN4 Enable for the linear regulator
- EXTSUP External power source for the MOSFETs
- GND (x9) Ground
- PH1 Switcher 1 phase pin
- PH2 Switcher 2 phase pin
- PH3 Switcher 3 phase pin
- RST1 Reset output for switcher 1
- RST2 Reset output for switcher 2
- RST3 Reset output for switcher 3
- RST4 Reset output for the linear regulator
- VBAT Power Input
- VIN Power Input after the reverse battery protection diode
- VINLR1 Linear regulator input
- VOUT1 Switcher 1 output
- VOUT2 Switcher 2 output
- VOUT3 Switcher 3 output
- VOUT4 Linear regulator output
- VSUP Power input for switcher 3

2.2 Setup

The input voltage range for the converter is 4 V to 40 V. The minimum input voltage is 6.5 V at start-up. The input voltage range is 4 V to 10 V for switcher 3.

2.3 Operation

For the correct operation of the TPS4334xEVM, Delay, EN1, EN2, EN3, EN4, EXTSUP, JP1, JP5, JP6, PGATE, and VIN2, must be properly configured. The recommended setting, using the switch and shorting blocks, follow.

Delay	1 ms
EN1	Disabled
EN2	Disabled
EN3	Disabled
EN4	Disabled
EXTSUP	VOUT1
JP1	Auto
JP5	External supply
ROSC	400 kHz
SLEW	Fast
SYNC	Forced continuous conduction mode
VIN2	VIN
VINLR1	VIN

In this configuration, the regulators do not turn on when power is applied. You enable the regulators by using the enable jumpers after power has been applied to the EVM.

Delay sets the power-on reset delay – slow, medium or fast. EN1, EN2, EN3, and EN4 turn the regulators on or off, disabled or enabled. EXTSUP selects the power supply source for the MOSFETs. JP1 controls the PGATE FET. The FET can be turned off or set to be controlled automatically by the TPS4334x. JP5 sets the power source for switcher 3, external supply VSUP, or VOUT1. JP6 sets the switching frequency for the regulators to approximately 250 kHz, 400 kHz, or 600 kHz. SLEW sets the slew rate for the high-side FETs on switcher 3 – slow, medium, or fast. SYNC enables LPM or forced continuous conduction mode and is the external clock input for switching frequency synchronization of the buck converters. SYNC disables spread spectrum operation on the TPS43341 when set low or left open. VIN2 selects the power source for switcher 2, VIN, or VOUT1. VINLR1 selects the power source for the linear regulator – VIN or VOUT1.

The device can be set up to run in low-power mode, to reduce the quiescent operating current, by setting the Sync jumper to 0. Low-power mode allows the device to switch into a PFM mode of operation, if the load current demand is low. It automatically switches back to PWM mode as the load current increases.

Regulator Configuration:

Regulator	Output Voltage (V)	Maximum Output Current (A)
Switcher 1:	5	4.5
Switcher 2:	3.3	4.5
Switcher 3:	1.8	2.2
VLR:	3.3	0.3

3 Board Layout

Figure 14, Figure 15, and Figure 16 show the board layout for the TPS4334xEVM printed-circuit board (PCB).

The TPS4334x converter offers high efficiency, but does dissipate power. The PowerPAD™ package offers an exposed thermal pad to enhance thermal performance. This must be soldered to the copper landing on the PCB for optimal performance. The PCB provides 2-oz copper planes on the top and bottom to dissipate heat.

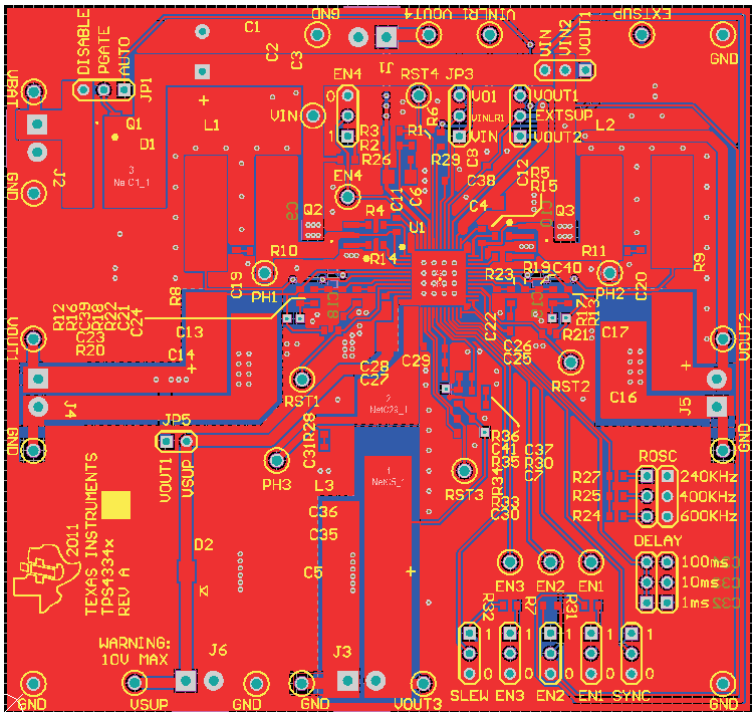

Figure 14. Top Assembly Layer

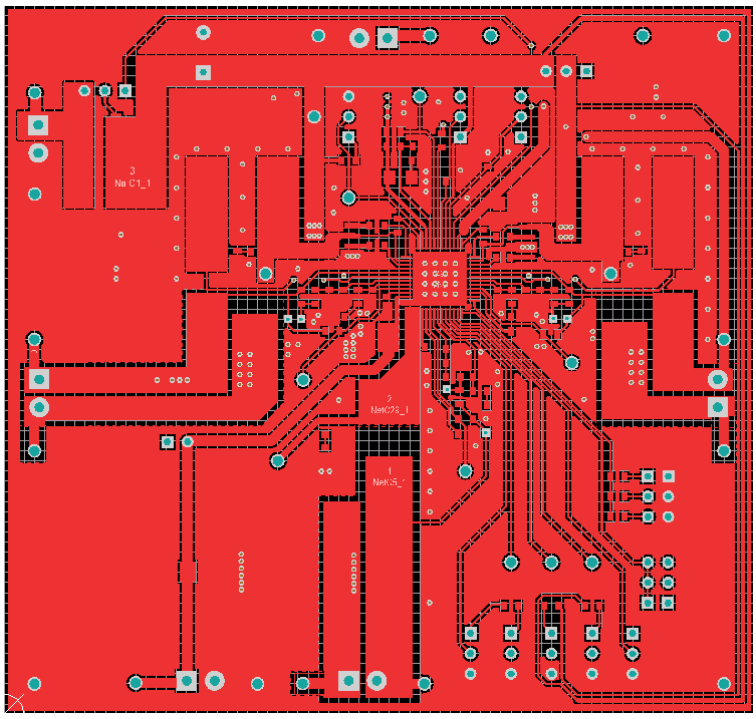

Figure 15. Top Layer Routing

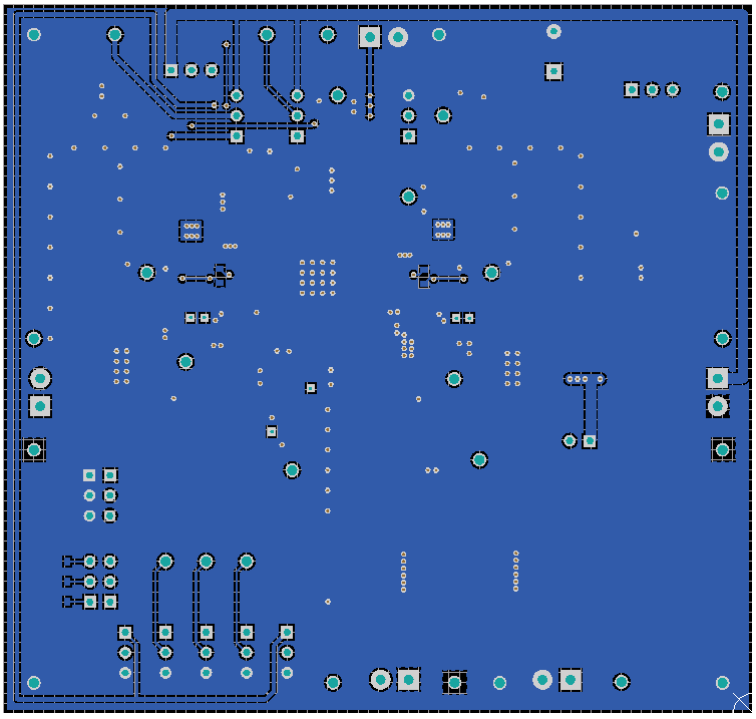

Figure 16. Bottom Layer Routing

4 Schematic and Bill of Materials

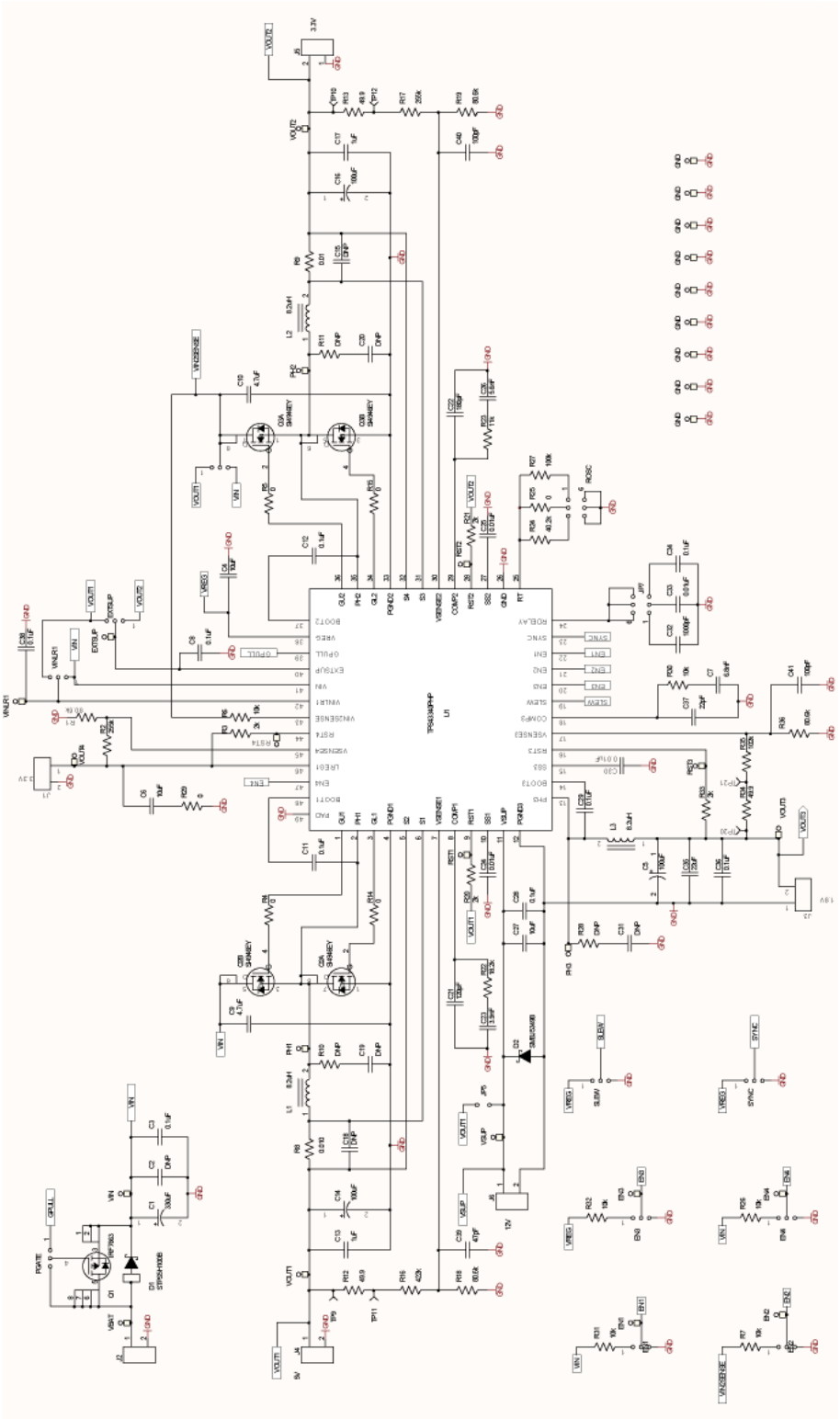

Figure 17. TPS4334xEVM Schematic

Table 2. TPS4334xEVM Bill of Materials

Count	REF DES	Description	Size	MFR	Part Number
1	C1	Capacitor, electrolytic, 330 µF, 50V	10mm x 20mm	Nichicon	UPW1H331MPD
7	C2, C15, C18, C19, C20, C31, C35	Do not populate			
9	C3, C8, C11, C12, C28, C29, C34, C36, C38	Capacitor, ceramic, 0.1 µF, 50V, 10%	603	STD	STD
3	C4, C6, C27	Capacitor, ceramic, 10 µF, 16V, 10%	1206	STD	STD
3	C5, C14, C16	Capacitor, tantalum, 100 µF, 16V, 10%	7343-31	AVX	TPSD107K016R0060
1	C7	Capacitor, ceramic, 6.8 nF, 50V, 10%	603	STD	STD
2	C9, C10	Capacitor, ceramic, 4.7 µF, 50V, +80%/–20%	1206	STD	STD
2	C13, C17	Capacitor, ceramic, 1 µF, 50V, 10%	1206	STD	STD
1	C21	Capacitor, ceramic, 120 pF, 50V, 5%	603	STD	STD
1	C22	Capacitor, ceramic, 180 pF, 50V, 5%	603	STD	STD
1	C23	Capacitor, ceramic, 3.9 nF, 50V, 10%	603	STD	STD
4	C24, C25, C30, C33	Capacitor, ceramic, 0.01 µF, 50V, 10%	603	STD	STD
1	C26	Capacitor, ceramic, 5.6 nF, 50V, 10%	603	STD	STD
1	C32	Capacitor, ceramic, 1000 pF, 50V, 10%	603	STD	STD
1	C37	Capacitor, ceramic, 22 pF, 50V, 5%	603	STD	STD
1	C39	Capacitor, ceramic, 47 pF, 50V, 10%	603	STD	STD
2	C40, C41	Capacitor, ceramic, 100 pF, 50V, 10%	603	STD	STD
1	D1	Diode, Schottky, 10A, 45V	DPAK	STM	STPS1045B
1	D2	Diode, Zener, 12V, 3W	SMB	MMC	3SMBJ5927B-TP
6	J1, J2, J3, J4, J5, J6	Terminal block, 2-pin, 6A, 3.5mm	0.25 x 0.27	OST	ED1514
29	EN1, EN2, EN3, EN4, EXTSUP, GND (9), PH1, PH2, PH3, RST1, RST2, RST3, RST4, SYNC, VBAT, VIN, VINLR1, VOUT1, VOUT2, VSUP, VOUT4	Test point, 52-mil	0.052	Kobiconn	151-103-RC
1	JP5	Header, 2-pin, 100-mil spacing	0.100 x 2	Sullins	PEC02SAAN
10	EN1, EN2, EN3, EN4, EXTSUP, JP1, JP3, SLEW, SYNC, VIN2	Header, 3-pin, 100-mil spacing	0.100 x 3	Sullins	PEC03SAAN
2	Delay, ROSC	Header, 6-pin, 100-mil spacing	0.100 x 3	Sullins	PEC06DAAN
13	Delay, EN1, EN2, EN3, EN4, EXTSUP, JP3, JP5, JP6, PGATE, SLEW, SYNC, VIN2	Connector jumper, shorting, 100-mil spacing	0.1	Sullins	SPC02SYAN
3	L1, L2, L3	Inductor, SMT, 8.2-µH	12.5mm x 12.5mm	Coiltronics	DR127-8R2-R

Table 2. TPS4334xEVM Bill of Materials (continued)

Count	REF DES	Description	Size	MFR	Part Number
1	Q1	MOSFET, P-Channel 20-V	Micro8	IR	IRF7663TRPBF
2	Q2, Q3	MOSFET, Dual N-Channel	SO8	Vishay	SI4946BEY-T1-E3
4	R1, R18, R19, R36	Resistor, chip, 80.6-kohms, 1/10W, 1%	603	STD	STD
2	R2, R17	Resistor, chip, 255-kohms, 1/10W, 1%	603	STD	STD
4	R3, R20, R21, R33	Resistor, chip, 2-kohms, 1/10W, 1%	603	STD	STD
6	R4, R5, R14, R15, R25, R29	Resistor, chip, 0-ohms, 1/10W, 1%	603	STD	STD
5	R6, R7, R26, R31, R32	Resistor, chip, 10-kohms, 1/10W, 1%	603	STD	STD
2	R8, R9	Resistor, chip, 0.01-ohms, 1 W, 1%	2512	Vishay	WSL2512R0100FEA
4	R10, R11, R28, R38	Do not populate			
3	R12, R13, R34	Resistor, chip, 49.9-ohms, 1/10W, 1%	603	STD	STD
1	R16	Resistor, chip, 432-kohms, 1/10W, 1%	603	STD	STD
1	R22	Resistor, chip, 18.2-kohms, 1/10W, 1%	603	STD	STD
1	R23	Resistor, chip, 11-kohms, 1/10W, 1%	603	STD	STD
1	R24	Resistor, chip, 40.2-kohms, 1/10W, 1%	603	STD	STD
1	R27	Resistor, chip, 100-kohms, 1/10W, 1%	603	STD	STD
1	R30	Resistor, chip, 10-kohms, 1/10W, 1%	603	STD	STD
1	R35	Resistor, chip, 102-kohms, 1/10W, 1%	603	STD	STD
1	U1	IC, TPS43340QPHPR or TPS43341QPHPR		TI	TPS43340QPHP or TPS43341QPHPR

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 4.0x V to 36 V (4.0V to 10V for switcher 3) and the output voltage range of 09 V to 12 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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