19-5545; Rev 0; 9/10

Current-Mode PWM Controllers with Frequency Dithering for EMI-Sensitive Power Supplies

General Description

The MAX5975_ current-mode PWM controllers contain all the control circuitry required for the design of wide-input-voltage forward and flyback power supplies in Power-over-Ethernet (PoE) IEEE® 802.3af/at powered devices. The MAX5975A is well-suited for universal input (rectified 85V AC to 265V AC) or telecom (-36V DC to -72V DC) power supplies. The MAX5975B is available for low-voltage supplies (12V to 24V) such as wall adapters.

The devices are suitable for both isolated and nonisolated designs. Because the devices have an internal error amplifier with a 1% accurate reference, they can be used in nonisolated power supplies without the need for an external shunt regulator.

An enable input (EN) is used to shut down the devices. Programmable soft-start eliminates output voltage overshoot. The MAX5975A has an internal bootstrap UVLO with large hysteresis that requires 20V for startup, while the MAX5975B requires 10V for startup.

The switching frequency for the ICs is programmable from 100kHz to 600kHz with an external resistor. For EMI-sensitive design, use the programmable frequency dithering feature for low-EMI spread-spectrum operation. The duty cycle is also programmable up to the 80% maximum duty-cycle limit. These devices are available in 16-lead TQFN packages and are rated for operation over the -40°C to +85°C temperature range.

Applications

PoE IEEE 802.3af/at Powered Devices

Flyback/Forward DC-DC Converters

IP Phones

Wireless Access Nodes

Security Cameras

Power Devices in PoE/Power-over-MDI

Features

- **Peak Current-Mode Control, Forward/Flyback PWM Controllers**
- **Internal 1% Error Amplifier**
- **100kHz to 600kHz Programmable ±8% Switching Frequency**
- **Switching Frequency Synchronization Up to 1.2MHz**
- **Programmable Frequency Dithering for Low-EMI Spread-Spectrum Operation**
- **PWM Soft-Start, Current Slope Compensation**
- **Programmable Feed-Forward Maximum Duty-Cycle Clamp, 80% Maximum Limit**
- **Frequency Foldback for High-Efficiency Light-Load Operation**
- **Internal Bootstrap UVLO with Large Hysteresis**
- **100µA (typ) Startup Supply Current**
- **Fast Cycle-by-Cycle Peak Current-Limit, 35ns Typical Propagation Delay**
- **115ns Current-Sense Internal Leading-Edge Blanking**
- **Output Short-Circuit Protection with Hiccup Mode**
- **3mm x 3mm, Lead-Free, 16-Pin TQFN**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	UVLO THRESHOLD (V)
MAX5975AETE+	-40°C to +85°C	16 TQFN-EP*	+AIC	20
MAX5975BETE+	-40°C to +85°C	16 TQFN-EP*	+AID	10

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

IN to GND .... -0.3V to +26V
EN, NDRV to GND .... -0.3V to (V_{IN} + 0.3V)
RT, FFB, COMP, SS, DCLMP, DITHER/SYNC
to GND .... -0.3V to +6V
FB to GND .... -0.3V to +6V
CS, CSSC to GND .... -0.8V to +6V
PGND to GND .... -0.3V to +0.3V
Maximum Input/Output Current (continuous)
NDRV 100mA
NDRV (pulsed for less than 100ns) .... ±1A

Continuous Power Dissipation (T_A = +70°C) (Note 1)
16-Pin TQFN (derate 20.8mW/°C above +70°C) 1666mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
16-Pin TQFN .... +7°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
16-Pin TQFN .... +48°C/W
Operating Temperature Range .... -40°C to +85°C
Maximum Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V (for MAX5975A, bring V_{IN} up to 21V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = +2V, NDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, C_{IN} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT/STARTUP (IN)							
Bootstrap UVLO Wakeup Level	V_{INUVR}	V_{IN} rising	MAX5975A	19.1	19.8	20.4	V
			MAX5975B	9.4	9.8	10.25	
Bootstrap UVLO Shutdown Level	V_{INUVF}	V_{IN} falling		6.65	7	7.35	V
IN Supply Current in Undervoltage Lockout	I_{START}	V_{IN} = +18V (for MAX5975A); V_{IN} = +9V (for MAX597BA), when in bootstrap UVLO			100	150	µA
IN Supply Current After Startup	I_C	V_{IN} = +12V			1.8	3	mA
ENABLE (EN)							
Enable Threshold	V_{ENR}	V_{EN} rising		1.17	1.215	1.26	V
	V_{ENF}	V_{EN} falling		1.09	1.14	1.19	
Input Current	I_{EN}					1	µA
OSCILLATOR (RT)							
RT Bias Voltage	V_{RT}				1.23		V
NDRV Switching Frequency Range	f_{SW}			100		600	kHz
NDRV Switching Frequency Accuracy				-8		+8	%
Maximum Duty Cycle	D_{MAX}	f_{SW} = 250kHz		81	82.5	84	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V (for MAX5975A, bring V_{IN} up to 21V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = +2V, NDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, C_{IN} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONIZATION (SYNC)						
Synchronization Logic-High Input	$V_{IH-SYNC}$		2.91			V
Synchronization Pulse Width				50		ns
Synchronization Frequency Range	f_{SYNCIN}		1.1 x f_{SW}		2 x f_{SW}	kHz
Maximum Duty Cycle During Synchronization				D_{MAX} x f_{SYNC}/ f_{SW}		%
DITHERING RAMP GENERATOR (DITHER)						
Charging Current		V_{DITHER} = 0V	45	50	55	µA
Discharging Current		V_{DITHER} = 2.2V	43	50	57	µA
Ramp's High Trip Point				2		V
Ramp's Low Trip Point				0.4		V
SOFT-START AND RESTART (SS)						
Charging Current	I_{SS-CH}		9.5	10	10.5	µA
Discharging Current	I_{SS-D}	V_{SS} = 2V, normal shutdown	0.65	1.34	2	mA
	I_{SS-DH}	(V_{EN} < V_{ENF} or V_{IN} < V_{INUVF}), V_{SS} = 2V, hiccup mode discharge for $t_{RESTART}$ (Note 3)	1.6	2	2.4	µA
Discharge Threshold to Disable Hiccup and Restart	V_{SS-DTH}			0.15		V
Minimum Restart Time During Hiccup Mode	$t_{RSTRT-MIN}$			1024		Clock Cycles
Normal Operating High Voltage	V_{SS-HI}			5		V
Duty-Cycle Control Range	$V_{SS-DMAX}$	D_{MAX} (typ) = ($V_{SS-DMAX}$/2.43V)	0		2	V
DUTY-CYCLE CLAMP (DCLMP)						
DCLMP Input Current	I_{DCLMP}	V_{DCLMP} = 0 to 5V	-100	0	+100	nA
Duty-Cycle Control Range	$V_{DCLMP-R}$	D_{MAX} (typ) = 1 - (V_{DCLMP}/2.43V), V_{DCLMP} = 0.5V	75	77.3	79.5	%
		D_{MAX} (typ) = 1 - (V_{DCLMP}/2.43V), V_{DCLMP} = 1V	56	58	60	%
		D_{MAX} (typ) = 1 - (V_{DCLMP}/2.43V), V_{DCLMP} = 2V	17	18.6	20.5	%
NDRV DRIVER						
Pulldown Impedance	R_{NDRV-N}	I_{NDRV} (sinking) = 100mA		1.9	3.4	Ω
Pullup Impedance	R_{NDRV-P}	I_{NDRV} (sourcing) = 50mA		4.7	8.3	Ω
Peak Sink Current				1		A
Peak Source Current				0.65		A
Fall Time	t_{NDRV-F}	C_{NDRV} = 1nF		14		ns
Rise Time	t_{NDRV-R}	C_{NDRV} = 1nF		27		ns

Current-Mode PWM Controllers with Frequency Dithering for EMI-Sensitive Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V (for MAX5975A, bring V_{IN} up to 21V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = +2V, NDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, C_{IN} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

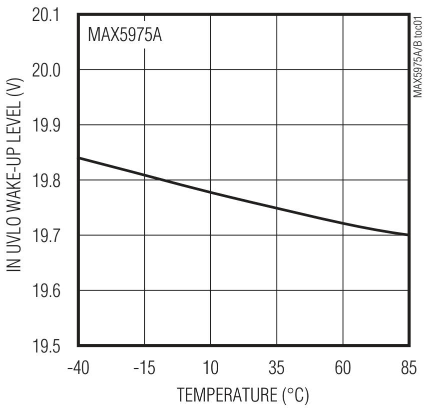
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-LIMIT COMPARATORS (CS)						
Cycle-by-Cycle Peak Current-Limit Threshold	$V_{CS-PEAK}$		375	393	410	mV
Number of Consecutive Peak Current-Limit Events to Hiccup	N_{HICCUP}			8		Events
Current-Sense Leading-Edge Blanking Time	$t_{CS-BLANK}$	From NDRV rising edge		115		ns
Propagation Delay from Comparator Input to NDRV	t_{PDCS}	From CS rising (10mV overdrive) to NDRV falling (excluding leading-edge blanking)		35		ns
Minimum On-Time	t_{ON-MIN}		100	150	200	ns
SLOPE COMPENSATION (CSSC)						
Slope Compensation Current Ramp Height		Current ramp's peak added to CSSC input per switching cycle	47	52	58	µA
PWM COMPARATOR						
Comparator Offset Voltage	V_{PWM-OS}	V_{COMP} - V_{CSSC}	1.35	1.7	2	V
Current-Sense Gain	A_{CS-PWM}	$\Delta V_{COMP}/\Delta V_{CSSC}$ (Note 4)	3.1	3.33	3.6	V/V
Current-Sense Leading-Edge Blanking Time	$t_{CSSC-BLANK}$	From NDRV rising edge		115		ns
Comparator Propagation Delay	t_{PWM}	Change in V_{CSSC} = 10mV (including internal leading-edge blanking)		150		ns
ERROR AMPLIFIER						
FB Reference Voltage	V_{REF}	V_{FB} when I_{COMP} = 0, V_{COMP} = 2.5V	1.202	1.215	1.227	V
FB Input Bias Current	I_{FB}	V_{FB} = 0 to 1.75V	-500		+100	nA
Voltage Gain	A_{EAMP}			80		dB
Transconductance	g_M		1.8	2.66	3.5	mS
Transconductance Bandwidth	BW	Open loop (typical gain = 1) -3dB frequency		30		MHz
Source Current		V_{FB} = 1V, V_{COMP} = 2.5V	300	375	455	µA
Sink Current		V_{FB} = 1.75V, V_{COMP} = 1V	300	375	455	µA
FREQUENCY FOLDBACK (FFB)						
V_{CSAVG}-to-FFB Comparator Gain				10		V/V
FFB Bias Current	I_{FFB}	V_{FFB} = 0V, V_{CS} = 0V (not in FFB mode)	26	30	33	µA
NDRV Switching Frequency During Foldback	f_{SW-FB}			$f_{SW}/2$		kHz

Note 2: The devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 3: See the *Output Short-Circuit Protection with Hiccup Mode* section.
Note 4: The parameter is measured at the trip point of latch with V_{FB} = 0V. Gain is defined as $\Delta V_{COMP}/\Delta V_{CSSC}$ for 0.15V < ΔV_{CSSC} < 0.25V.

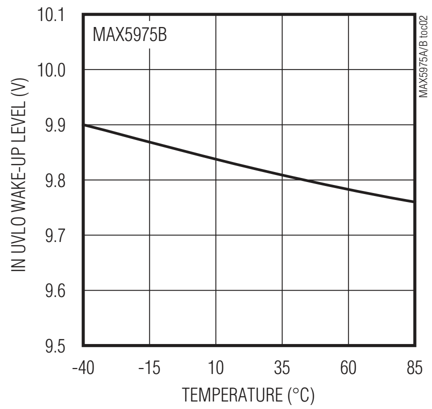
Typical Operating Characteristics

(V_{IN} = 12V (for MAX5975A, bring V_{IN} up to 21V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = +2V, NDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, unless otherwise noted.)

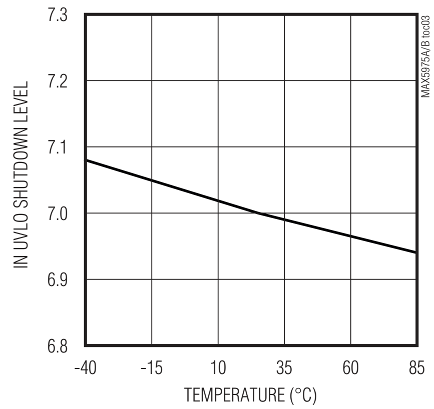
IN UVLO WAKE-UP LEVEL vs. TEMPERATURE



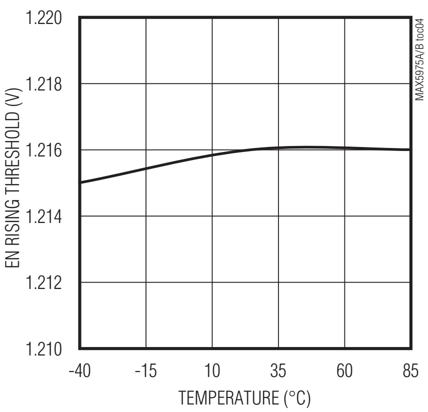
IN UVLO WAKE-UP LEVEL vs. TEMPERATURE



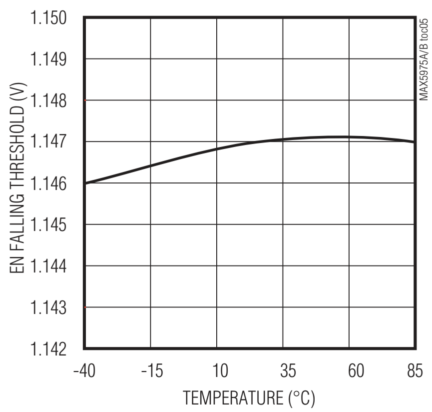
IN UVLO SHUTDOWN LEVEL vs. TEMPERATURE



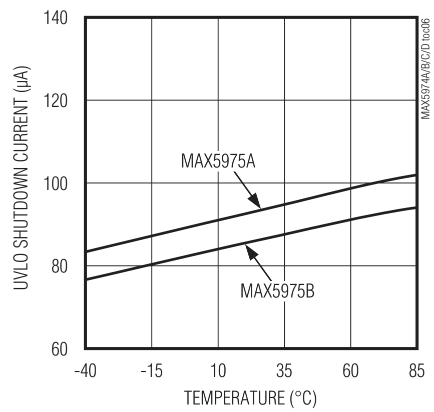
EN RISING THRESHOLD vs. TEMPERATURE



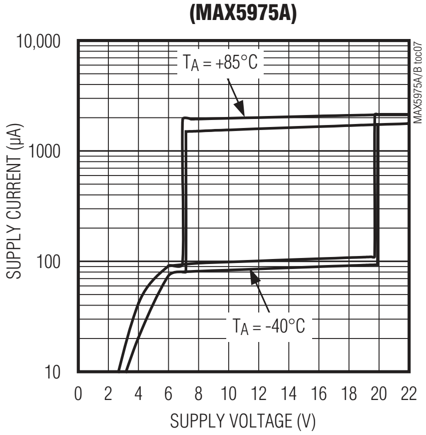
EN FALLING THRESHOLD vs. TEMPERATURE



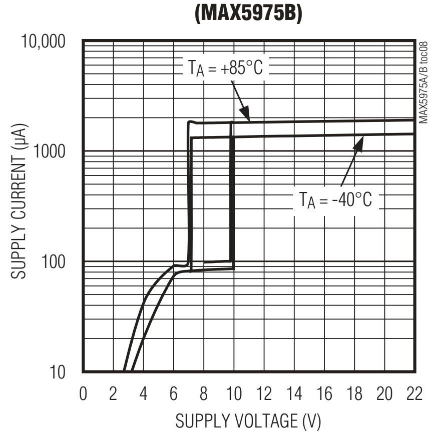
UVLO SHUTDOWN CURRENT vs. TEMPERATURE



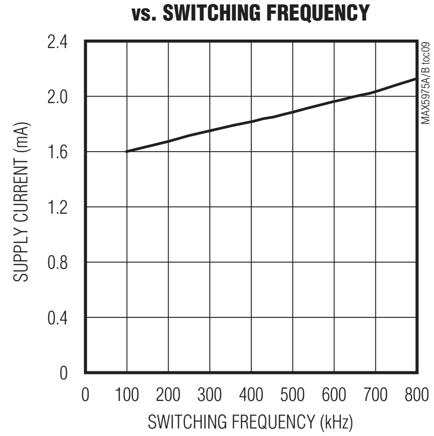
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5975A)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5975B)



SUPPLY CURRENT vs. SWITCHING FREQUENCY

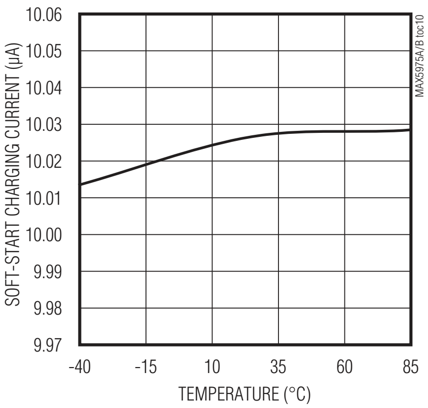


Current-Mode PWM Controllers with Frequency Dithering for EMI-Sensitive Power Supplies

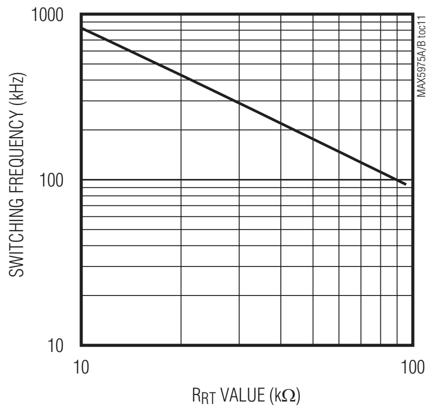
Typical Operating Characteristics (continued)

(V_{IN} = 12V (for MAX5975A, bring V_{IN} up to 21V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = +2V, NDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, unless otherwise noted.)

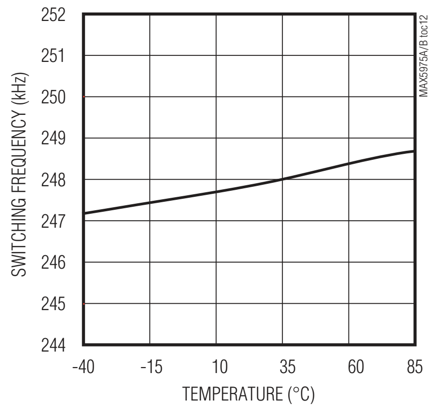
SOFT-START CHARGING CURRENT vs. TEMPERATURE



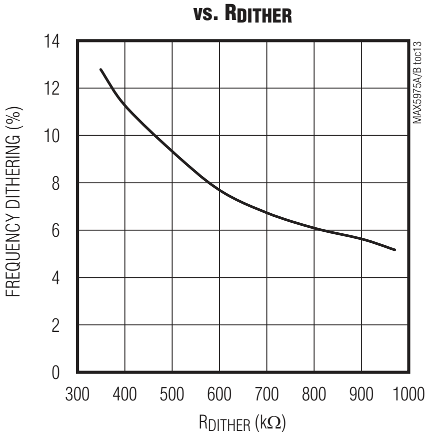
SWITCHING FREQUENCY vs. R_{RT} VALUE



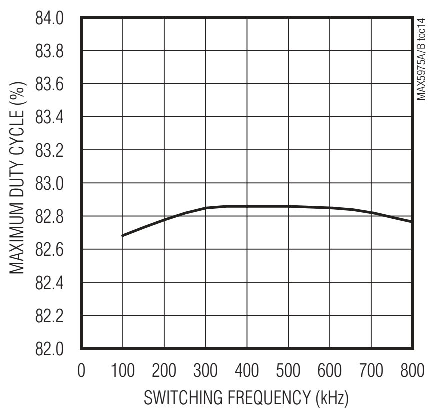
SWITCHING FREQUENCY vs. TEMPERATURE



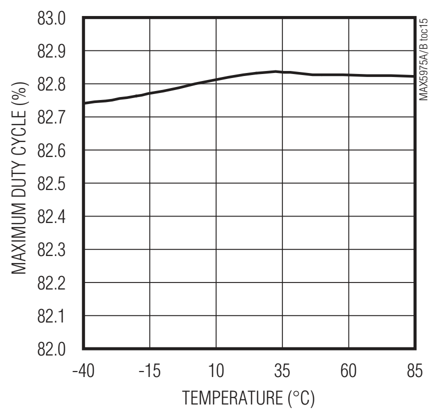
FREQUENCY DITHERING vs. R_{DITHER}



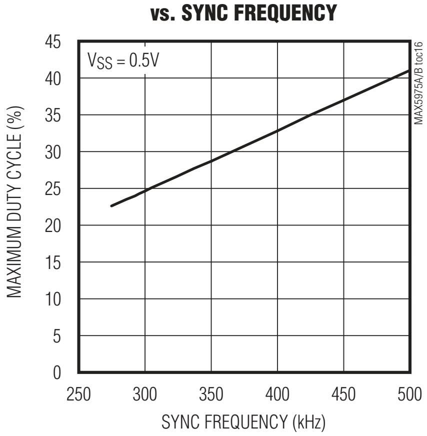
MAXIMUM DUTY CYCLE vs. SWITCHING FREQUENCY



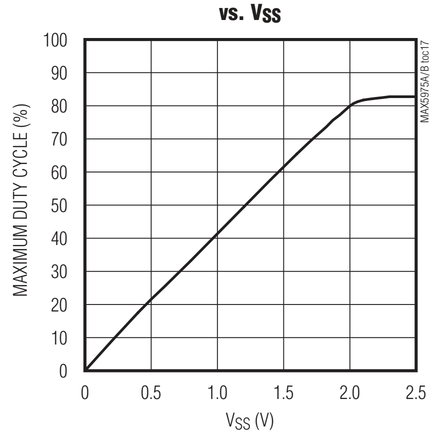
MAXIMUM DUTY CYCLE vs. TEMPERATURE



MAXIMUM DUTY CYCLE vs. SYNC FREQUENCY



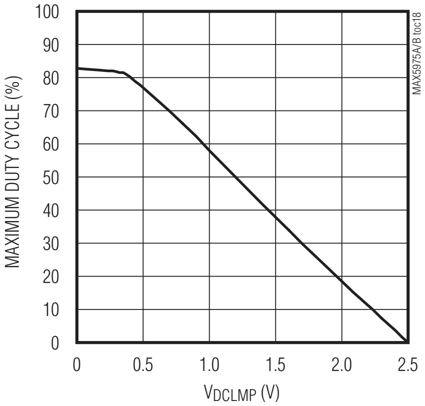
MAXIMUM DUTY CYCLE vs. V_{SS}



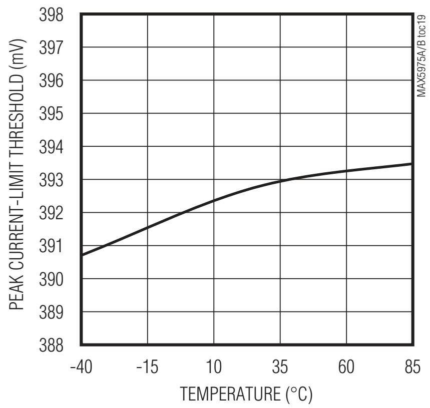
Typical Operating Characteristics (continued)

(V_{IN} = 12V (for MAX5975A, bring V_{IN} up to 21V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = +2V, NDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, unless otherwise noted.)

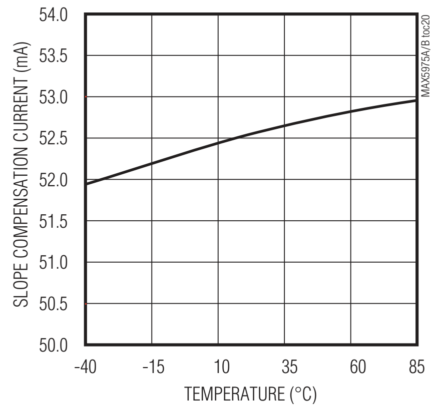
MAXIMUM DUTY CYCLE vs. V_{DCLMP}



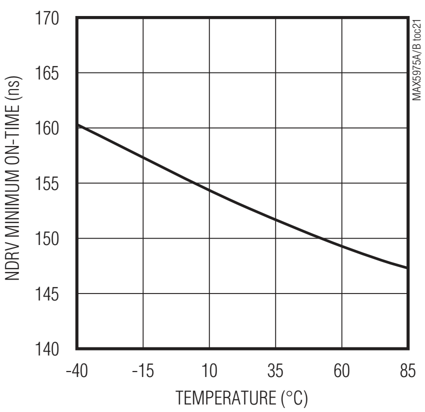
PEAK CURRENT-LIMIT THRESHOLD vs. TEMPERATURE



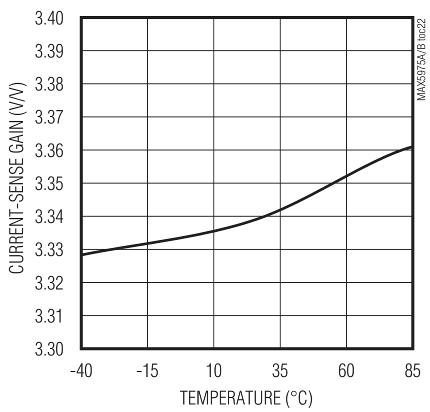
SLOPE COMPENSATION CURRENT vs. TEMPERATURE



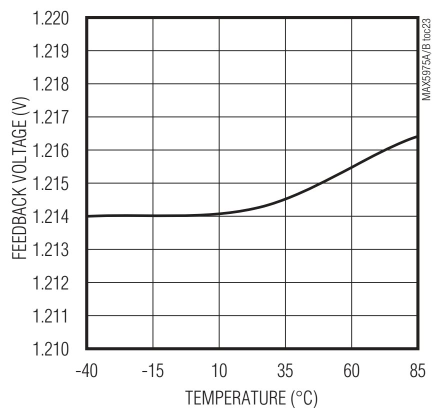
NDRV MINIMUM ON-TIME vs. TEMPERATURE



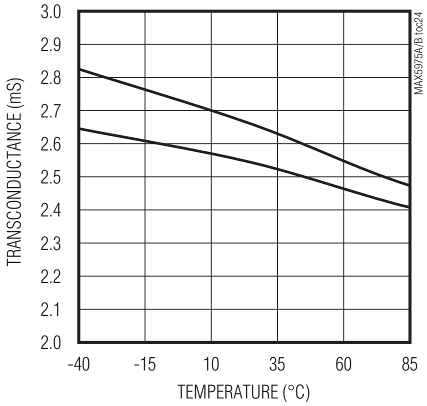
CURRENT-SENSE GAIN vs. TEMPERATURE



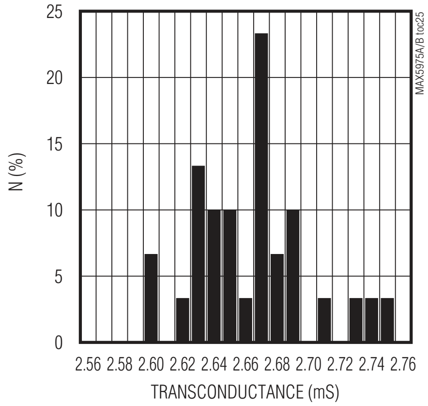
FEEDBACK VOLTAGE vs. TEMPERATURE



TRANSCONDUCTANCE vs. TEMPERATURE



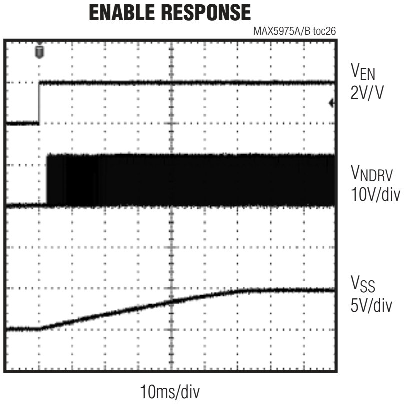
TRANSCONDUCTANCE HISTOGRAM



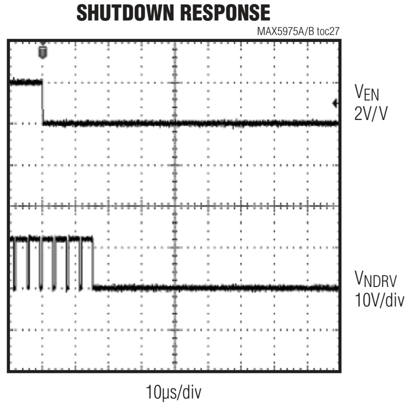
Typical Operating Characteristics (continued)

(V_{IN} = 12V (for MAX5975A, bring V_{IN} up to 21V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = +2V, NDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, unless otherwise noted.)

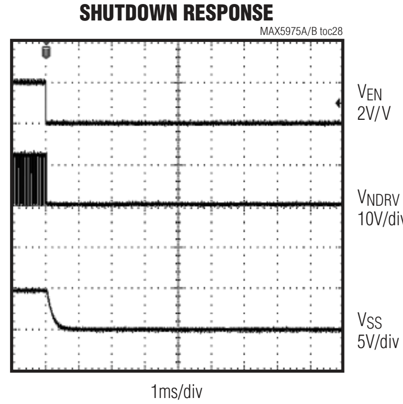
ENABLE RESPONSE



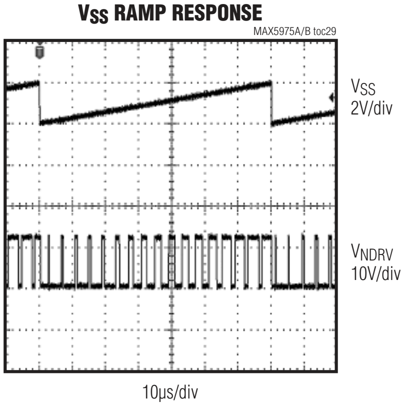
SHUTDOWN RESPONSE



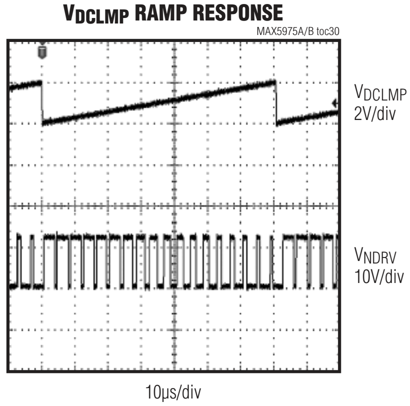
SHUTDOWN RESPONSE



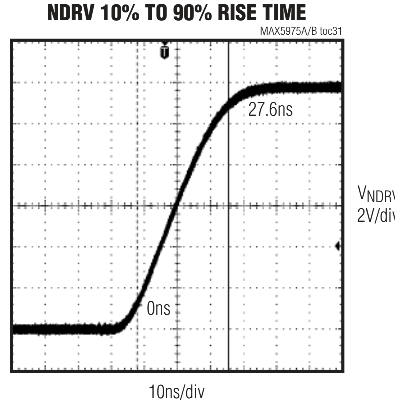
V_{SS} RAMP RESPONSE



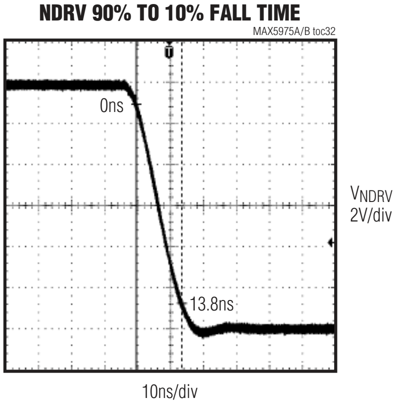
V_{DCLMP} RAMP RESPONSE



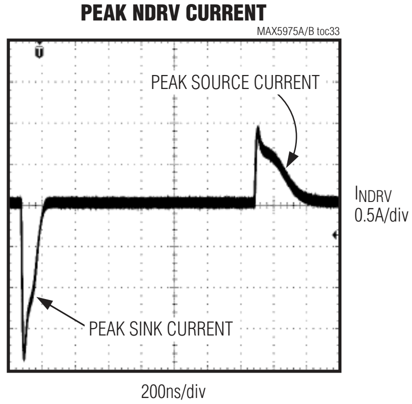
NDRV 10% TO 90% RISE TIME



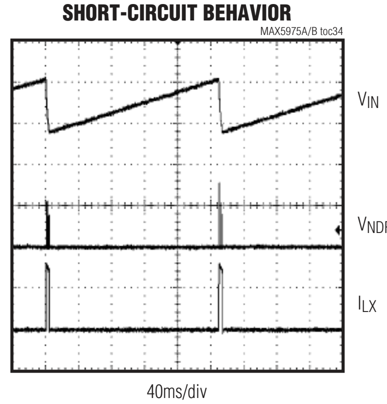
NDRV 90% TO 10% FALL TIME



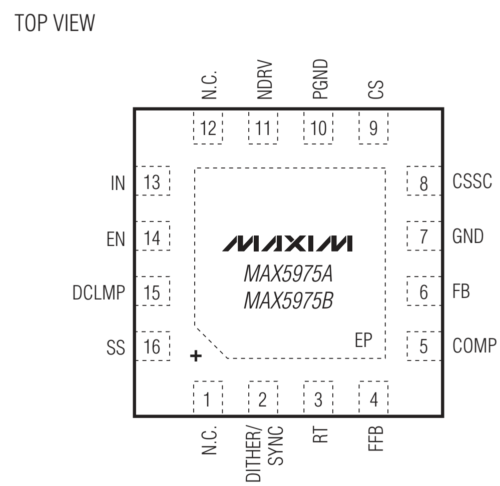
PEAK NDRV CURRENT



SHORT-CIRCUIT BEHAVIOR



Pin Configuration



TQFN

Pin Description

PIN	NAME	FUNCTION
1, 12	N.C.	No Connection. Not internally connected.
2	DITHER/ SYNC	Frequency Dithering Programming or Synchronization Connection. For spread-spectrum frequency operation, connect a capacitor from DITHER to GND, and a resistor from DITHER to RT. To synchronize the internal oscillator to the externally applied frequency, connect DITHER/SYNC to the synchronization pulse.
3	RT	Switching Frequency Programming Resistor Connection. Connect resistor R_{RT} from RT to GND to set the PWM switching frequency. See the *Oscillator/Switching Frequency* section to calculate the resistor value for the desired oscillator frequency.
4	FFB	Frequency Foldback Threshold Programming Input. Connect a resistor from FFB to GND to set the output average current threshold below which the converter folds back the switching frequency to 1/2 of its original value. Connect to GND to disable frequency foldback.
5	COMP	Transconductance Amplifier Output and PWM Comparator Input. COMP is level shifted down and connected to the inverting input of the PWM comparator.

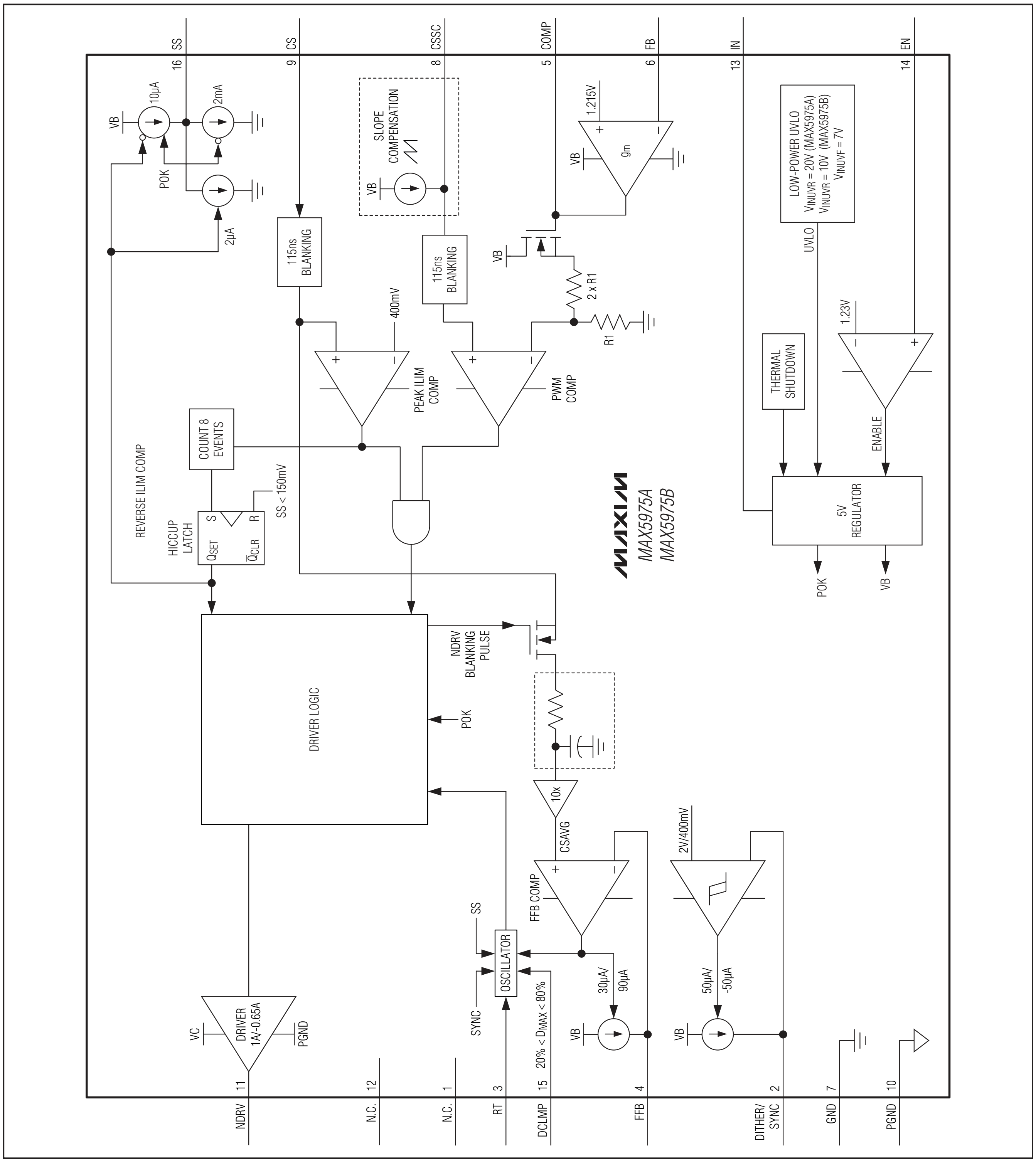
Current-Mode PWM Controllers with Frequency Dithering for EMI-Sensitive Power Supplies

Pin Description (continued)

PIN	NAME	FUNCTION
6	FB	Transconductance Amplifier Inverting Input
7	GND	Signal Ground
8	CSSC	Current Sense with Slope Compensation Input. A resistor connected from CSSC to CS programs the amount of slope compensation. See the *Programmable Slope Compensation* section.
9	CS	Current-Sense Input. Current-sense connection for average current sense and cycle-by-cycle current limit. Peak current-limit trip voltage is 400mV.
10	PGND	Power Ground. PGND is the return path for gate-driver switching currents.
11	NDRV	External Switching nMOS Gate-Driver Output
13	IN	Converter Supply Input. IN has wide UVLO hysteresis, enabling the design of efficient power supplies. When the enable input EN is used to program a UVLO level for the power source, connect a zener diode between IN and PGND to ensure that V_{IN} is always clamped below its absolute maximum rating of 26V.
14	EN	Enable Input. The gate drivers are disabled and the device is in a low-power UVLO mode, when the voltage on EN is below V_{ENF}. When the voltage on EN is above V_{ENR}, the device checks for other enable conditions. See the *Enable Input* section for more information about interfacing to EN.
15	DCLMP	Feed-Forward Maximum Duty-Cycle Clamp Programming Input. Connect a resistor-divider between the input supply voltage DCLMP and GND. The voltage at DCLMP sets the maximum duty cycle (D_{MAX}) of the converter inversely proportional to the input supply voltage, so that the MOSFET remains protected during line transients.
16	SS	Soft-Start Programming Capacitor Connection. Connect a capacitor from SS to GND to program the soft-start period. This capacitor also determines hiccup mode current-limit restart time. A resistor from SS to GND can also be used to set the D_{MAX} below 75%.
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Current-Mode PWM Controllers with Frequency Dithering for EMI-Sensitive Power Supplies

Block Diagram



Current-Mode PWM Controllers with Frequency Dithering for EMI-Sensitive Power Supplies

Detailed Description

The MAX5975_ is optimized for controlling a 25W to 50W forward/flyback converter in continuous-conduction mode. The power MOSFET gate driver (NDRV) is sized to optimize efficiency for 25W design. The feature-rich devices are ideal for PoE IEEE 802.3af/at-powered devices.

The MAX5975A offers a bootstrap UVLO wakeup level of 20V with a wide hysteresis of 13V. The low startup and operating currents allow the use of a smaller storage capacitor at the input without compromising startup and hold times. The device is well-suited for universal input (rectified 85V AC to 265V AC) or telecom (-36V DC to -72V DC) power supplies.

The MAX5975B has a UVLO rising threshold of 10V and is well-suited for low-input voltage (12V DC to 24V DC) power sources such as wall adapters.

Power supplies designed with the MAX5975A use a high-value startup resistor, R_{IN}, that charges a reservoir capacitor, C_{IN} (see the *Typical Applications Circuits*). During this initial period, while the voltage is less than the internal bootstrap UVLO threshold, the device typically consumes only 100µA of quiescent current. This low startup current and the large bootstrap UVLO hysteresis help to minimize the power dissipation across R_{IN} even at the high end of the universal AC input voltage (265V AC).

Feed-forward maximum duty-cycle clamping detects changes in line conditions and adjusts the maximum duty cycle accordingly to eliminate the clamp voltage's (i.e., the main power FET's drain voltage) dependence on the input voltage.

For EMI-sensitive applications, the programmable frequency dithering feature allows up to ±10% variation in the switching frequency. This spread-spectrum modulation technique spreads the energy of switching harmonics over a wider band while reducing their peaks, helping to meet stringent EMI goals.

The devices include a cycle-by-cycle current limit that turns off the driver whenever the internally set threshold of 400mV is exceeded. Eight consecutive occurrences of current-limit event trigger hiccup mode, which protects external components by halting switching for a period of time (t_{RSTRT}) and allowing the overload current to dissipate in the load and body diode of the synchronous rectifier before soft-start is reattempted.

Current-Mode Control Loop

The advantages of current-mode control over voltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Secondly, the stability requirements of the current-mode controller are reduced to that of a single-pole system, unlike the double pole in voltage-mode control.

The devices use a current-mode control loop where the scaled output of the error amplifier (COMP) is compared to a slope-compensated current-sense signal at CSSC.

Enable Input

The enable input EN is used to enable or disable the device. Connect EN to IN for always enabled applications. Connecting EN to ground disables the device and reduces current consumption to 100µA.

The enable input has an accurate threshold of 1.26V (max). For applications that require a UVLO on the power source, connect a resistive divider from the power source to EN to GND as shown in Figure 1. A zener diode between IN and PGND is required to prevent IN from exceeding its absolute maximum rating of 26V when the device is disabled. The zener diode should be inactive below the maximum UVLO rising threshold voltage $V_{INUVR(MAX)}$ (21V for the MAX5975A and 10.5V for the MAX5975B). Design the resistive divider by first selecting the value of R_{EN1} to be on the order of 100kΩ. Then calculate R_{EN2} as follows:

$$R_{EN2} = R_{EN1}\frac{V_{EN(MAX)}}{V_{S(UVLO)} - V_{EN(MAX)}}$$

where $V_{EN(MAX)}$ is the maximum enable threshold voltage and is equal to 1.26V and $V_{S(UVLO)}$ is the desired UVLO threshold for the power source, below which the devices are disabled.

In the case where EN is externally controlled and UVLO for the power source is unnecessary, connect EN to IN and an open-drain or open-collector output as shown in Figure 2. The digital output connected to EN should be capable of withstanding IN's absolute maximum voltage of 26V.

Bootstrap Undervoltage Lockout

The device has an internal bootstrap UVLO that is very useful when designing high-voltage power supplies (see the *Block Diagram*). This allows the device to bootstrap itself during initial power-up. The MAX5975A soft-starts when V_{IN} exceeds the bootstrap UVLO threshold of V_{INUVR} (20V typ).

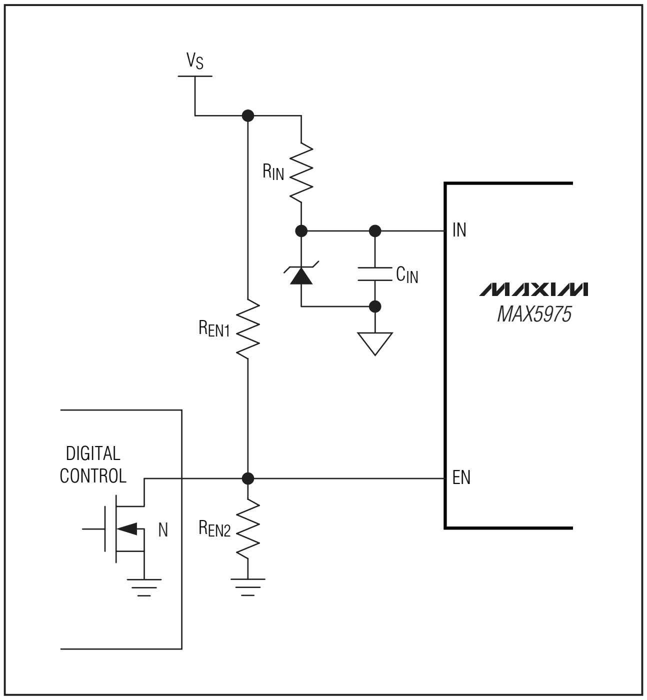


Figure 1. Programmable UVLO for the Power Source

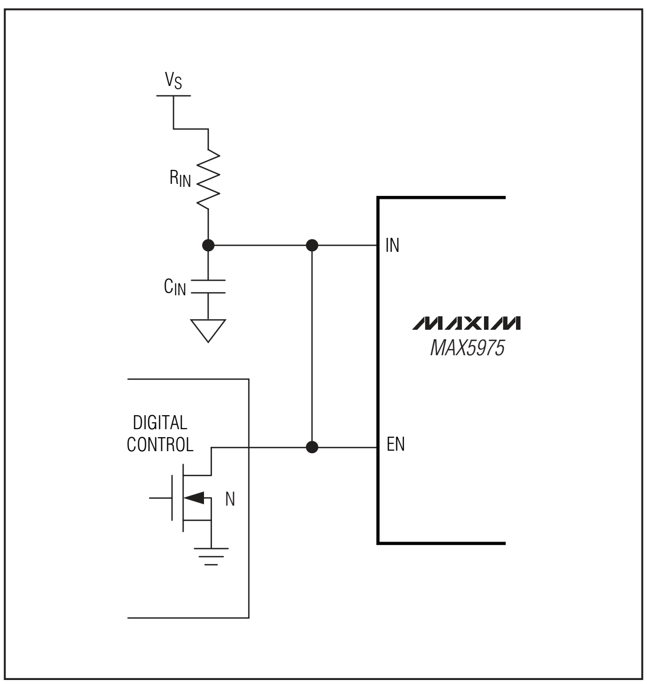


Figure 2. External Control of the Enable Input

Because the MAX5975B is designed for use with low-voltage power sources such as wall adapters outputting 12V to 24V, it has a lower UVLO wakeup threshold of 10V.

Startup Operation

The device starts up when the voltage at IN exceeds 20V (MAX5975A) or 10V (MAX5975B) and the enable input voltage is greater than 1.26V.

During normal operation, the voltage at IN is normally derived from a tertiary winding of the transformer. However, at startup there is no energy being delivered through the transformer; hence, a special bootstrap sequence is required. In the *Typical Applications Circuits*, C_{IN} charges through the startup resistor, R_{IN}, to an intermediate voltage. Only 100µA of the current supplied through R_{IN} is used by the ICs, the remaining input current charges C_{IN} until V_{IN} reaches the bootstrap UVLO wakeup level. Once V_{IN} exceeds this level, NDRV begins switching the n-channel MOSFET and transfers energy to the secondary and tertiary outputs. If the voltage on the tertiary output builds to higher than 7V (the bootstrap UVLO shutdown level), then startup has been accomplished and sustained operation commences. If V_{IN} drops below 7V before startup is complete, the device goes back to low-current UVLO. In this case, increase the value of C_{IN} to store enough energy to allow the voltage at the tertiary winding to build up.

Soft-Start

A capacitor from SS to GND, C_{SS}, programs the soft-start time. V_{SS} controls the oscillator duty cycle during startup to provide a slow and smooth increase of the duty cycle to its steady-state value. Calculate the value of C_{SS} as follows:

$$C_{SS} = \frac{I_{SS\text{-}CH} \times t_{SS}}{2V}$$

where $I_{SS\text{-}CH}$ (10µA typ) is the current charging C_{SS} during soft-start and t_{SS} is the programmed soft-start time.

A resistor can also be added from the SS pin to GND to clamp V_{SS} < 2V and, hence, program the maximum duty cycle to be less than 80% (see the *Duty-Cycle Clamping* section).

n-Channel MOSFET Gate Driver

The NDRV output drives an external n-channel MOSFET. NDRV can source/sink in excess of 650mA/1000mA peak current; therefore, select a MOSFET that yields acceptable conduction and switching losses. The external MOSFET used must be able to withstand the maximum clamp voltage.

Current-Mode PWM Controllers with Frequency Dithering for EMI-Sensitive Power Supplies

Oscillator/Switching Frequency

The ICs' switching frequency is programmable between 100kHz and 600kHz with a resistor R_{RT} connected between RT and GND. Use the following formula to determine the appropriate value of R_{RT} needed to generate the desired output-switching frequency (f_{SW}):

$$R_{RT} = \frac{8.7 \times 10^9}{f_{SW}}$$

where f_{SW} is the desired switching frequency.

Peak Current Limit

The current-sense resistor (R_{CS} in the *Typical Application Circuits*), connected between the source of the n-channel MOSFET and PGND, sets the current limit. The current-limit comparator has a voltage trip level ($V_{CS\text{-}PEAK}$) of 400mV. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{400\text{mV}}{I_{PRI}}$$

where I_{PRI} is the peak current in the primary side of the transformer, which also flows through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (NDRV) terminates the current on-cycle, within 35ns (typ).

The devices implement 115ns of leading-edge blanking to ignore leading-edge current spikes. These spikes are caused by reflected secondary currents, current-discharging capacitance at the FET's drain, and gate-charging current. Use a small RC network for additional filtering of the leading-edge spike on the sense waveform when needed. Set the corner frequency between 10MHz and 20MHz.

After the leading-edge blanking time, the device monitors V_{CS} for any breaches of the peak current limit of 400mV. The duty cycle is terminated immediately when V_{CS} exceeds 400mV.

Output Short-Circuit Protection with Hiccup Mode

When the device detects eight consecutive peak current-limit events, the driver output is turned off for a restart period, t_{RSTRT}. After t_{RSTRT}, the device undergoes soft-start. The duration of the restart period depends on the value of the capacitor at SS (C_{SS}). During this period, C_{SS} is discharged with a pulldown current of $I_{SS\text{-}DH}$ (2µA typ). Once its voltage reaches 0.15V, the restart period ends and the device initiates a soft-start sequence. An internal counter ensures that the minimum restart period ($t_{RSTRT\text{-}MIN}$) is 1024 clock cycles when the time required for C_{SS} to discharge to 0.15V is less than 1024 clock cycles. Figure 3 shows the behavior of the device prior and during hiccup mode.

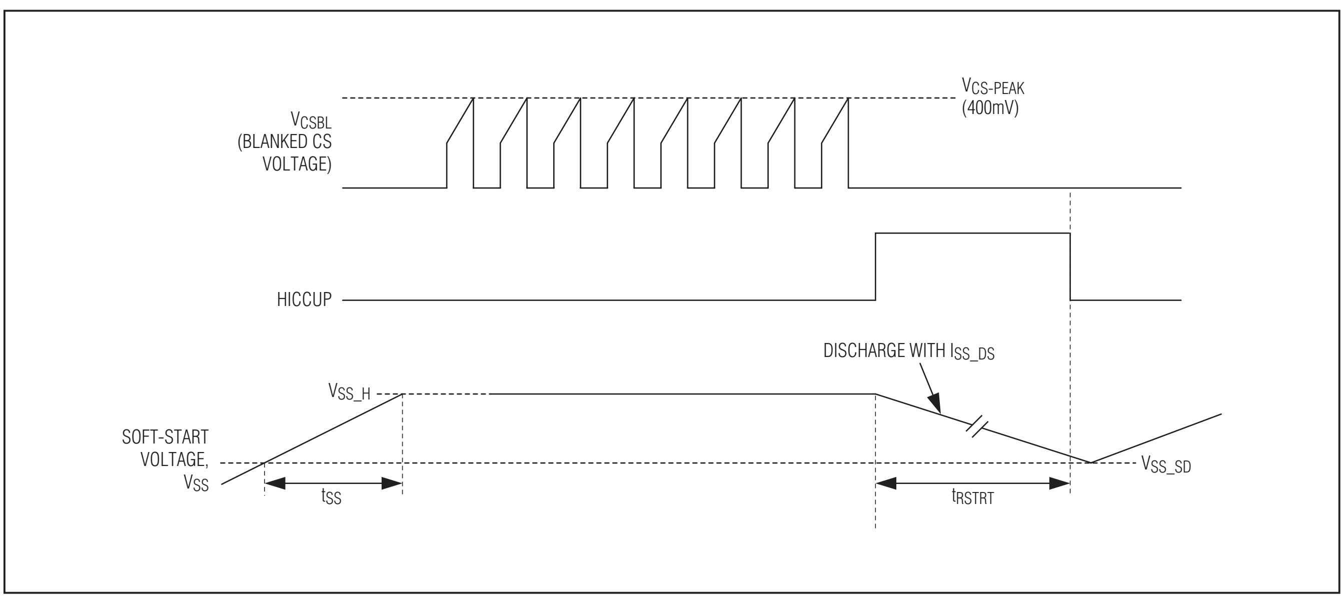


Figure 3. Hiccup Mode Timing Diagram

Frequency Foldback for High-Efficiency Light-Load Operation

The frequency foldback threshold can be programmed from 0 to 20% of the full load current using a resistor from FFB to GND.

Figure 4 shows device operation in frequency foldback mode. Calculate the value of R_{FFB} as follows:

$$R_{FFB} = \frac{10 \times I_{LOAD(LIGHT)} \times R_{CS}}{I_{FFB}}$$

where R_{FFB} is the resistor connected to FFB, $I_{LOAD(LIGHT)}$ is the current at light-load conditions that triggers frequency foldback, R_{CS} is the value of the sense resistor connected between CS and PGND, and I_{FFB} is the current sourced from FFB to R_{FFB} (30µA typ).

Duty-Cycle Clamping

The maximum duty cycle is determined by the lowest of three voltages: 2V, the voltage at SS (V_{SS}), and the voltage (2.43V - V_{DCLMP}). The maximum duty cycle is calculated as:

$$D_{MAX} = \frac{V_{MIN}}{2.43V}$$

where V_{MIN} = minimum (2V, V_{SS}, 2.43V - V_{DCLMP}).

SS

By connecting a resistor between SS and ground, the voltage at SS can be made to be lower than 2V. V_{SS} is calculated as follows:

$$V_{SS} = R_{SS} \times I_{SS-CH}$$

where R_{SS} is the resistor connected between SS and GND, and I_{SS-CH} is the current sourced from SS to R_{SS} (10µA typ).

DCLMP

To set D_{MAX} using supply voltage feed forward, connect a resistive divider between the supply voltage, DCLMP, and GND as shown in the *Typical Applications Circuits*. This feed-forward duty-cycle clamp ensures that the external n-channel MOSFET is not stressed during supply transients. V_{DCLMP} is calculated as follows:

$$V_{DCLMP} = \frac{R_{DCLMP2}}{R_{DCLMP1} + R_{DCLMP2}} \times V_S$$

where R_{DCLMP1} and R_{DCLMP2} are the resistive divider values shown in the *Typical Applications Circuits* and V_S is the input supply voltage.

Oscillator Synchronization

The internal oscillator can be synchronized to an external clock by applying the clock to SYNC/DITHER directly. The external clock frequency can be set anywhere between 1.1x to 2x the internal clock frequency.

Using an external clock increases the maximum duty cycle by a factor equal to f_{SYNC}/f_{SW}. This factor should be accounted for in setting the maximum duty cycle using any of the methods described in the *Duty-Cycle Clamping* section. The formula below shows how the maximum duty cycle is affected by the external clock frequency:

$$D_{MAX} = \frac{V_{MIN}}{2.43V} \times \frac{f_{SYNC}}{f_{SW}}$$

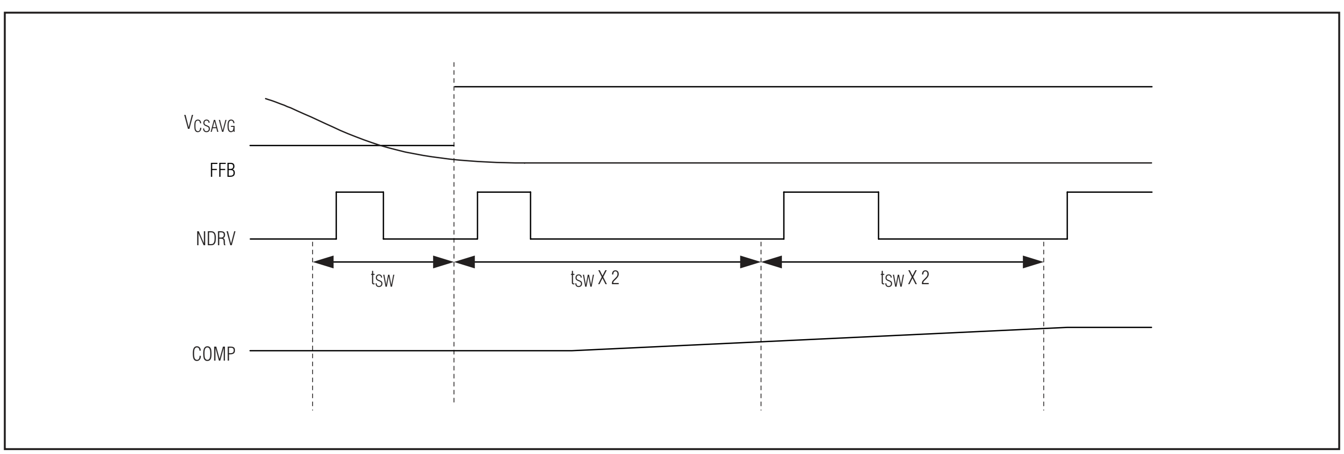


Figure 4. Entering Frequency Foldback

where V_{MIN} is described in the *Duty-Cycle Clamping* section, f_{SW} is the switching frequency as set by the resistor connected between RT and GND, and f_{SYNC} is the external clock frequency.

Frequency Dithering for Spread-Spectrum Applications (Low EMI)

The switching frequency of the converter can be dithered in a range of ±10% by connecting a capacitor from SYNC/DITHER to GND, and a resistor from DITHER to RT as shown in the *Typical Applications Circuits*. This results in lower EMI.

A current source at SYNC/DITHER charges the capacitor C_{DITHER} to 2V at 50µA. Upon reaching this trip point, it discharges C_{DITHER} to 0.4V at 50µA. The charging and discharging of the capacitor generates a triangular waveform on SYNC/DITHER with peak levels at 0.4V and 2V and a frequency that is equal to:

$$f_{TRI} = \frac{50\mu A}{C_{DITHER} \times 3.2V}$$

Typically, f_{TRI} should be set close to 1kHz. The resistor R_{DITHER} connected from SYNC/DITHER to RT determines the amount of dither as follows:

$$\%DITHER = \frac{4}{3} \times \frac{R_{RT}}{R_{DITHER}}$$

where %DITHER is the amount of dither expressed as a percentage of the switching frequency. Setting R_{DITHER} to 10 x R_{RT} generates ±10% dither.

Programmable Slope Compensation

The devices generate a current ramp at CSSC such that its peak is 50µA at 80% duty cycle of the oscillator. An external resistor connected from CSSC to CS then converts this current ramp into programmable slope-compensation amplitude, which is added to the current-sense signal for stability of the peak current-mode control loop. The ramp rate of the slope compensation signal is given by:

$$m = \frac{R_{CSSC} \times 50\mu A \times f_{SW}}{80\%}$$

where m is the ramp rate of the slope-compensation signal, R_{CSSC} is the value of the resistor connected between CSSC and CS used to program the ramp rate, and f_{SW} is the switching frequency.

Error Amplifier

The MAX5975A/MAX5975B include an internal error amplifier. The noninverting input of the error amplifier is connected to the internal 1.215V reference and feedback is provided at the inverting input. High 80dB open-loop gain and 30MHz unity-gain bandwidth allow good closed-loop bandwidth and transient response. Calculate the power-supply output voltage using the following equation:

$$V_{OUT} = V_{REF} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}}$$

where V_{REF} = 1.215V.

Applications Information

Startup Time Considerations

The bypass capacitor at IN, C_{IN}, supplies current immediately after the devices wake up (see the *Typical Application Circuits*). Large values of C_{IN} increase the startup time, but also supply gate charge for more cycles during initial startup. If the value of C_{IN} is too small, V_{IN} drops below 7V because NDRV does not have enough time to switch and build up sufficient voltage across the tertiary output, which powers the device. The device goes back into UVLO and does not start. Use a low-leakage capacitor for C_{IN}.

MAX5975A

Typically, offline power supplies keep startup times to less than 500ms even in low-line conditions (85V AC input for universal offline or 36V DC for telecom applications). Size the startup resistor, R_{IN}, to supply both the maximum startup bias of the device (150µA) and the charging current for C_{IN}. C_{IN} must be charged to 20V within the desired 500ms time period. C_{IN} must store enough charge to deliver current to the device for at least the soft-start time (t_{SS}) set by C_{SS}. To calculate the approximate amount of capacitance required, use the following formula:

$$I_G = Q_{GTOT} f_{SW}$$

$$C_{IN} = \frac{(I_{IN} + I_G)(t_{SS})}{V_{HYST}}$$

where I_{IN} is the internal supply current (1.7mA) after startup, Q_{GTOT} is the total gate charge for the n-channel FET, f_{SW} is the switching frequency, V_{HYST} is the bootstrap UVLO hysteresis (13V typ), and t_{SS} is the soft-start time. R_{IN} is then calculated as follows:

$$R_{IN} \cong \frac{V_{S(MIN)} - V_{INUVR}}{I_{START}}$$

where $V_{S(MIN)}$ is the minimum input supply voltage for the application (36V for telecom), V_{INUVR} is the bootstrap UVLO wake-up level (20V), and I_{START} is the IN supply current at startup (150µA max).

Choose a higher value for R_{IN} than the one calculated above if longer startup time can be tolerated in order to minimize power loss on this resistor.

MAX5975B

The parameters governing the design of the bootstrap circuit are different for the MAX5975B. While the above design equations remain valid, the following values must be used when designing for R_{IN} and C_{IN}: V_{HYST} = 3V and $V_{S(MIN)}$ is the minimum output voltage of the wall adapter.

Bias Circuit

An in-phase tertiary winding is needed to power the bias circuit. The voltage across the tertiary V_T during the on-time is:

$$V_T = V_{OUT} \times \frac{N_T}{N_S}$$

where V_{OUT} is the output voltage and N_T/N_S is the turns ratio from the tertiary to the secondary winding. Select the turns ratio so that V_T is above the UVLO shutdown level (7.5V max).

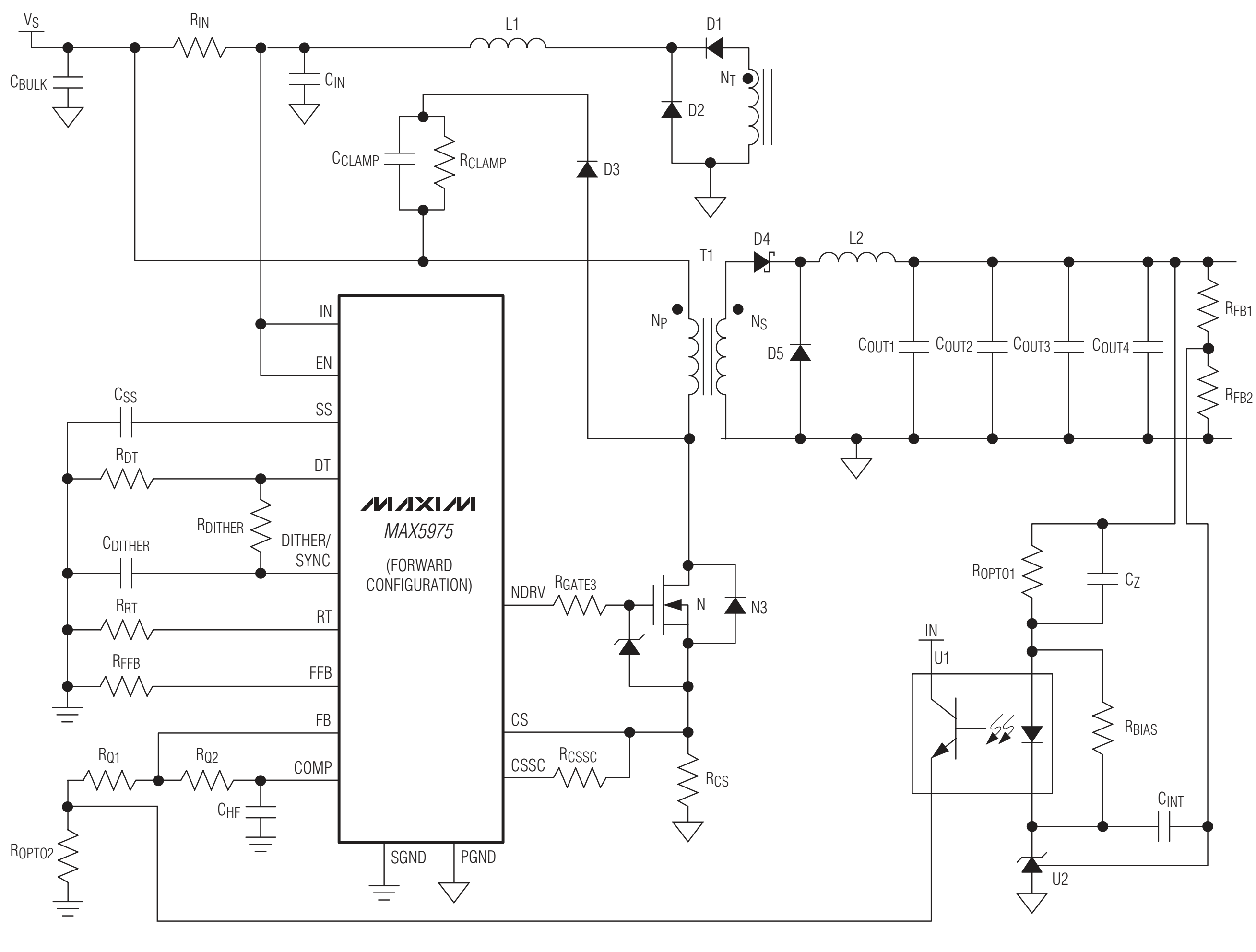
Layout Recommendations

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dV/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the main MOSFET presents a dV/dt source; therefore, minimize the surface area of the MOSFET heatsink as much as possible. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use a ground plane for best results.

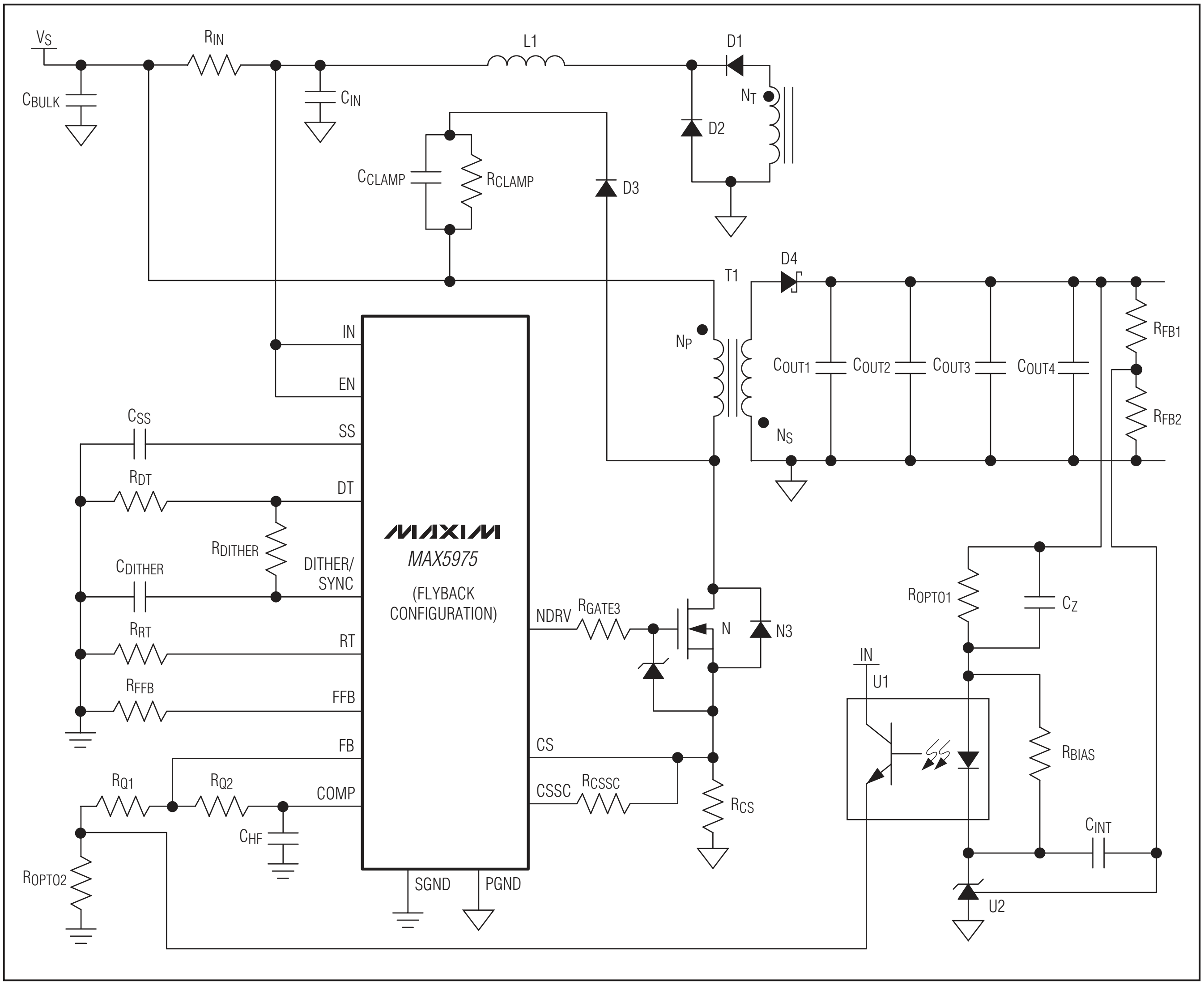
For universal AC input design, follow all applicable safety regulations. Offline power supplies may require UL, VDE, and other similar agency approvals.

Current-Mode PWM Controllers with Frequency Dithering for EMI-Sensitive Power Supplies

Typical Application Circuits



Typical Application Circuits (continued)



Chip Information

PROCESS: BiCMOS

Package Information

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PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1655+4	21-0136	90-0031

Current-Mode PWM Controllers with Frequency Dithering for EMI-Sensitive Power Supplies

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—

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