

AMC3301 Precision, ± 250 -mV Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter

1 Features

- 3.3-V or 5-V single supply with integrated DC/DC converter
- ± 250 -mV input voltage range optimized for current measurement using shunt resistors
- Fixed gain: 8.2
- Low DC errors:
 - Offset voltage: $\pm 150 \mu\text{V}$ (max)
 - Offset drift: $\pm 1 \mu\text{V}/^\circ\text{C}$ (max)
 - Gain error: $\pm 0.2\%$ (max)
 - Gain error drift: $\pm 40 \text{ ppm}/^\circ\text{C}$ (max)
 - Nonlinearity: $\pm 0.04\%$ (max)
- High CMTI: $85 \text{ kV}/\mu\text{s}$ (min)
- System-level diagnostic features
- Meets CISPR-11 and CISPR-25 EMI standards
- Safety-related certifications:
 - $6000\text{-V}_{\text{PK}}$ reinforced isolation per DIN VDE V 0884-11
 - $4250\text{-V}_{\text{RMS}}$ isolation for 1 minute per UL1577
- Fully specified over the extended industrial temperature range: -40°C to $+125^\circ\text{C}$

2 Applications

- Isolated shunt-based current sensing in:
 - [Protection relays](#)
 - [Motor drives](#)
 - [Power supplies](#)
 - [Photovoltaic inverters](#)

3 Description

The AMC3301 is a precision, isolated amplifier optimized for shunt-based current measurements. The fully integrated, isolated DC/DC converter allows single-supply operation from the low-side of the device, which makes the device a unique solution for space-constrained applications. The reinforced capacitive isolation barrier is certified according to VDE V 0884-11 and UL1577 and supports a working voltage of up to $1.2 \text{ kV}_{\text{RMS}}$.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from hazardous voltages and damage.

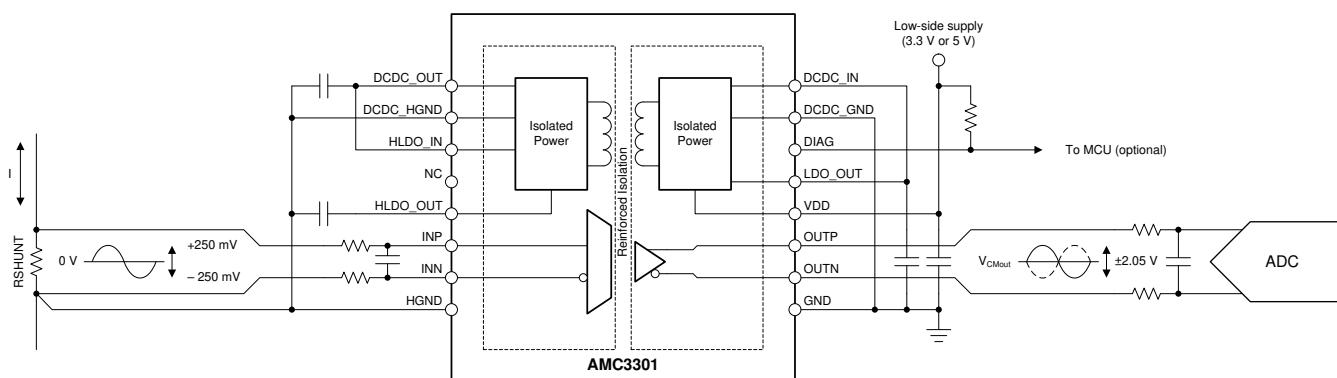
The input of the AMC3301 is optimized for direct connection to a low-impedance shunt resistor or other, low-impedance voltage source with low signal levels. The excellent DC accuracy and low temperature drift supports accurate current measurements over the extended industrial temperature range from -40°C to $+125^\circ\text{C}$.

The integrated DC/DC converter fault-detection and diagnostic output pin of the AMC3301 simplify system-level design and diagnostics.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|--------------------|
| AMC3301 | SOIC (16) | 10.30 mm × 7.50 mm |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application



Table of Contents

| | | | |
|--|----|--|----|
| 1 Features | 1 | 7.2 Functional Block Diagram..... | 18 |
| 2 Applications | 1 | 7.3 Feature Description..... | 18 |
| 3 Description | 1 | 7.4 Device Functional Modes..... | 21 |
| 4 Revision History | 2 | 8 Application and Implementation | 22 |
| 5 Pin Configuration and Functions | 3 | 8.1 Application Information..... | 22 |
| 6 Specifications | 4 | 8.2 Typical Application..... | 22 |
| 6.1 Absolute Maximum Ratings | 4 | 9 Power Supply Recommendations | 26 |
| 6.2 ESD Ratings | 4 | 10 Layout | 27 |
| 6.3 Recommended Operating Conditions | 4 | 10.1 Layout Guidelines..... | 27 |
| 6.4 Thermal Information | 5 | 10.2 Layout Example..... | 27 |
| 6.5 Power Ratings | 5 | 11 Device and Documentation Support | 28 |
| 6.6 Insulation Specifications | 6 | 11.1 Device Support..... | 28 |
| 6.7 Safety-Related Certifications | 7 | 11.2 Documentation Support..... | 28 |
| 6.8 Safety Limiting Values | 7 | 11.3 Receiving Notification of Documentation Updates.. | 28 |
| 6.9 Electrical Characteristics | 8 | 11.4 Support Resources..... | 28 |
| 6.10 Switching Characteristics | 10 | 11.5 Trademarks..... | 28 |
| 6.11 Timing Diagram..... | 10 | 11.6 Electrostatic Discharge Caution..... | 28 |
| 6.12 Insulation Characteristics Curves..... | 11 | 11.7 Glossary..... | 28 |
| 6.13 Typical Characteristics..... | 12 | 12 Mechanical, Packaging, and Orderable Information | 28 |
| 7 Detailed Description | 18 | | |
| 7.1 Overview..... | 18 | | |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (July 2020) to Revision B (May 2021) | Page |
|---|------|
| • Changed Features section: changed <i>Offset voltage</i> and <i>Offset drift</i> sub-bullets in <i>Low DC errors</i> bullet, rearranged bullets, added last bullet..... | 1 |
| • Changed target application from <i>Isolated voltage sensing</i> to <i>Isolated shunt-based current sensing</i> in <i>Applications</i> section..... | 1 |
| • Changed <i>Pin Configuration and Functions</i> section..... | 3 |
| • Changed <i>Absolute Maximum Ratings</i> : changed max for <i>DIAG</i> pin from 5.5 V to 6.5 V..... | 4 |
| • Changed overvoltage category for rated mains voltage ≤ 600 V from I-IV to I-III and for rated mains voltage ≤ 1000 V from I-III to I-II | 6 |
| • Changed <i>output bandwidth (BW) (min)</i> from 250 kHz to 290 kHz..... | 8 |
| • Changed <i>Typical Characteristics</i> section. Removed histograms, editorial changes..... | 12 |
| • Changed <i>Functional Block Diagram</i> figure..... | 18 |
| • Changed <i>Data Isolation Channel Signal Transmission</i> section..... | 19 |
| • Changed <i>Analog Output</i> section..... | 20 |
| • Changed <i>Diagnostic Output</i> section: added <i>DIAG Output Under Different Operating Conditions</i> figure..... | 21 |
| • Changed <i>Typical Application</i> section..... | 22 |
| • Changed <i>Input Filter Design</i> section: changed <i>Differential Input Filter</i> figure..... | 23 |
| • Added <i>Differential to Single-Ended Output Conversion</i> section..... | 24 |
| • Changed <i>Step Response of the AMC3301</i> figure..... | 24 |
| • Changed <i>Power Supply Recommendations</i> section: changed nominal value in the first sentence from 3.3 V (or 5 V) ± 10 V to 3.3 V or 5 V, changed <i>primary-side</i> to <i>low-side</i> , <i>secondary-side</i> to <i>high-side</i> , and <i>Decoupling the AMC3301</i> figure..... | 26 |
| • Changed <i>Recommended Layout of the AMC3301</i> figure..... | 27 |

| Changes from Revision * (August 2019) to Revision A (July 2020) | Page |
|---|------|
| • Changed document status from advance information to production data | 1 |

5 Pin Configuration and Functions

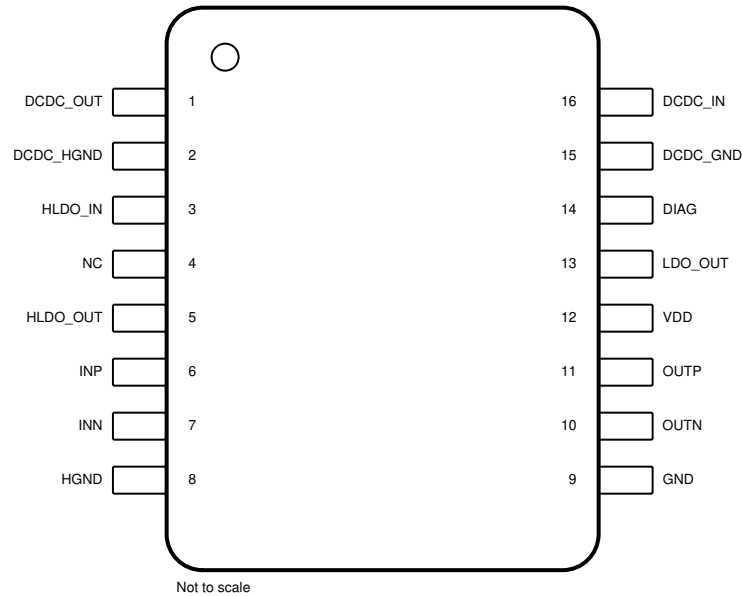


Figure 5-1. DWE Package, 16-Pin SOIC, Top View

Table 5-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----|-----------|-------------------------|---|
| NO. | NAME | | |
| 1 | DCDC_OUT | Power | High-side output of the isolated DC/DC converter; connect this pin to the HLDO_IN pin. ⁽¹⁾ |
| 2 | DCDC_HGND | High-side power ground | High-side ground reference for the isolated DC/DC converter; connect this pin to the HGND pin. |
| 3 | HLDO_IN | Power | Input of the high-side LDO; connect this pin to the DCDC_OUT pin. ⁽¹⁾ |
| 4 | NC | — | No internal connection; connect this pin to HGND or leave this pin unconnected. |
| 5 | HLDO_OUT | Power | Output of the high-side LDO. ⁽¹⁾ |
| 6 | INP | Analog input | Noninverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage. ⁽²⁾ |
| 7 | INN | Analog input | Inverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage. ⁽²⁾ |
| 8 | HGND | High-side signal ground | High-side analog ground; connect this pin to the DCDC_HGND pin. |
| 9 | GND | Low-side signal ground | Low-side analog ground; connect this pin to the DCDC_GND pin. |
| 10 | OUTN | Analog output | Inverting analog output. |
| 11 | OUTP | Analog output | Noninverting analog output. |
| 12 | VDD | Low-side power | Low-side power supply. ⁽¹⁾ |
| 13 | LDO_OUT | Power | Output of the low-side LDO; connect this pin to the DCDC_IN pin. The output of the LDO must not be loaded by external circuitry. ⁽¹⁾ |
| 14 | DIAG | Digital output | Active-low, open-drain status indicator output; connect this pin to the pullup supply (for example, VDD) using a resistor or leave this pin floating if not used. |
| 15 | DCDC_GND | Low-side power ground | Low-side ground reference for the isolated DC/DC converter; connect this pin to the GND pin. |
| 16 | DCDC_IN | Power | Low-side input of the isolated DC/DC converter; connect this pin to the LDO_OUT pin. ⁽¹⁾ |

(1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.

(2) See the [Layout](#) section for details.

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

| | | MIN | MAX | UNIT |
|------------------------|--|-----------|-----------------------|------|
| Power-supply voltage | VDD to GND | -0.3 | 6.5 | V |
| Analog input voltage | INP, INN | HGND – 6 | $V_{HLDO_OUT} + 0.5$ | V |
| Analog output voltage | OUTP, OUTN | GND – 0.5 | VDD + 0.5 | V |
| Digital output voltage | DIAG | GND – 0.5 | 6.5 | V |
| Input current | Continuous, any pin except power-supply pins | -10 | 10 | mA |
| Temperature | Junction, T_J | | 150 | °C |
| | Storage, T_{stg} | -65 | 150 | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|-------------|-------------------------|--|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | | Charged device model (CDM), per JESD22-C101 (2) | ±1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT | |
|--------------------------|---|-----------------------------------|-------|-----------------|------|---|
| POWER SUPPLY | | | | | | |
| VDD | Low-side power supply | VDD to GND | 3 | 3.3 | 5.5 | V |
| ANALOG INPUT | | | | | | |
| $V_{Clipping}$ | Differential input voltage before clipping output | $V_{IN} = V_{INP} - V_{INN}$ | ±320 | | mV | |
| V_{FSR} | Specified linear differential full-scale voltage | $V_{IN} = V_{INP} - V_{INN}$ | -250 | 250 | mV | |
| | Absolute common-mode input voltage (1) | $(V_{INP} + V_{INN}) / 2$ to HGND | -2 | V_{HLDO_OUT} | V | |
| V_{CM} | Operating common-mode input voltage | $(V_{INP} + V_{INN}) / 2$ to HGND | -0.16 | 1 | V | |
| TEMPERATURE RANGE | | | | | | |
| T_A | Specified ambient temperature | | -40 | 125 | °C | |

- (1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | AMC3301 | UNIT |
|-------------------------------|--|------------|------|
| | | DWE (SOIC) | |
| | | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 73.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 31 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 44 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 16.7 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 42.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---------------------------|-----------------|-----|-----|-----|------|
| P_D | Maximum power dissipation | VDD = 5.5 V | | | 231 | mW |
| | | VDD = 3.6 V | | | 151 | |

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|--|--------------------|------------------|
| GENERAL | | | | |
| CLR | External clearance ⁽¹⁾ | Shortest pin-to-pin distance through air | ≥ 8 | mm |
| CPG | External creepage ⁽¹⁾ | Shortest pin-to-pin distance across the package surface | ≥ 8 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance - capacitive signal isolation) | ≥ 21 | μm |
| | | Minimum internal gap (internal clearance - transformer power isolation) | ≥ 120 | |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | ≥ 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 600 V _{RMS} | I-III | |
| | | Rated mains voltage ≤ 1000 V _{RMS} | I-II | |
| DIN VDE V 0884-11 (VDE V 0884-11): 2017-01⁽²⁾ | | | | |
| V _{IORM} | Maximum repetitive peak isolation voltage | At AC voltage (bipolar) | 1700 | V _{PK} |
| V _{IOWM} | Maximum-rated isolation working voltage | At AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test | 1200 | V _{RMS} |
| | | At DC voltage | 1700 | V _{DC} |
| V _{IOTM} | Maximum transient isolation voltage | V _{TEST} = V _{IOTM} , t = 60 s (qualification test) | 6000 | V _{PK} |
| | | V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production test) | 7200 | V _{PK} |
| V _{IOSM} | Maximum surge isolation voltage ⁽³⁾ | Test method per IEC 60065, 1.2/50-μs waveform, V _{TEST} = 1.6 × V _{IOSM} = 10000 V _{PK} (qualification) | 6250 | V _{PK} |
| q _{pd} | Apparent charge ⁽⁴⁾ | Method a, after input/output safety test subgroup 2 / 3, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s | ≤ 5 | pC |
| | | Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s | ≤ 5 | |
| | | Method b1, at routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s, V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s | ≤ 5 | |
| C _{IO} | Barrier capacitance, input to output ⁽⁵⁾ | V _{IO} = 0.5 V _{PP} at 1 MHz | ~3.5 | pF |
| R _{IO} | Insulation resistance, input to output ⁽⁵⁾ | V _{IO} = 500 V at T _A = 25°C | > 10 ¹² | Ω |
| | | V _{IO} = 500 V at 100°C ≤ T _A ≤ 125°C | > 10 ¹¹ | |
| | | V _{IO} = 500 V at T _S = 150°C | > 10 ⁹ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| UL1577 | | | | |
| V _{ISO} | Withstand isolation voltage | V _{TEST} = V _{ISO} = 4250 V _{RMS} or 6000 V _{DC} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production test) | 4250 | V _{RMS} |

- Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings must be ensured by means of suitable protective circuits.
- Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- Apparent charge is electrical discharge caused by a partial discharge (pd).
- All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

| VDE | UL |
|--|--|
| Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11 | Recognized under 1577 component recognition and CSA component acceptance NO 5 programs |
| Reinforced insulation | Single protection |
| Certificate number: 40040142 | File number: E181974 |

6.8 Safety Limiting Values

Safety limiting ⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---|--|-----|-----|------|------|
| I _S | Safety input, output, or supply current | R _{θJA} = 73.5°C/W, VDD = 5.5 V, T _J = 150°C, T _A = 25°C | | | 309 | mA |
| | | R _{θJA} = 73.5°C/W, VDD = 3.6 V, T _J = 150°C, T _A = 25°C | | | 472 | |
| P _S | Safety input, output, or total power | R _{θJA} = 73.5°C/W, T _J = 150°C, T _A = 25°C | | | 1700 | mW |
| T _S | Maximum safety temperature | | | | 150 | °C |

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where T_{J(max)} is the maximum junction temperature.

$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum low-side voltage.

6.9 Electrical Characteristics

minimum and maximum specifications apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ to 5.5 V , $I_{NP} = -250\text{ mV}$ to $+250\text{ mV}$, $I_{NN} = \text{HGND} = 0\text{ V}$, and the external components listed in the *Typical Application* section; typical specifications are at $T_A = 25^\circ\text{C}$, and $V_{DD} = 3.3\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|--|--------|---------------|-------|------------------------------|
| ANALOG INPUT | | | | | | |
| R_{IN} | Single-ended input resistance | $I_{NN} = \text{HGND}$ | | 19 | | k Ω |
| R_{IND} | Differential input resistance | | | 22 | | |
| I_{IB} | Input bias current | $I_{NP} = I_{NN} = \text{HGND}$; $I_{IB} = (I_{IBP} + I_{IBN}) / 2$ | -41 | -30 | -24 | μA |
| TC_{IB} | Input bias current drift | | | 0.8 | | nA/ $^\circ\text{C}$ |
| I_{IO} | Input offset current | $I_{IO} = I_{IBP} - I_{IBN} $ | | 1.4 | | nA |
| C_{IN} | Single-ended input capacitance | $I_{NN} = \text{HGND}$, $f_{IN} = 275\text{ kHz}$ | | 2 | | pF |
| C_{IND} | Differential input capacitance | $f_{IN} = 275\text{ kHz}$ | | 1 | | |
| ANALOG OUTPUT | | | | | | |
| | Nominal gain | | | 8.2 | | V/V |
| V_{CMout} | Common-mode output voltage | | 1.39 | 1.44 | 1.49 | V |
| $V_{CLIPout}$ | Clipping differential output voltage | $V_{OUT} = (V_{OUTP} - V_{OUTN})$; $ V_{IN} = V_{INP} - V_{INN} > V_{Clipping}$ | | ± 2.49 | | V |
| $V_{Failsafe}$ | Failsafe differential output voltage | $V_{OUT} = (V_{OUTP} - V_{OUTN})$; $V_{DCDC_OUT} \leq V_{DCDCUV}$, or $V_{HLD0_OUT} \leq V_{HLD0UV}$ | | -2.57 | -2.5 | V |
| BW | Output bandwidth | | 290 | 334 | | kHz |
| R_{OUT} | Output resistance | On OUTP or OUTN | | 0.2 | | Ω |
| | Output short-circuit current | On OUTP or OUTN, sourcing or sinking, $I_{NP} = I_{NN} = \text{HGND}$, outputs shorted to either GND or VDD | | 14 | | mA |
| CMTI | Common-mode transient immunity | $ HGND - GND = 2\text{ kV}$ | 85 | 135 | | kV/ μs |
| ACCURACY | | | | | | |
| V_{OS} | Input offset voltage ^{(1) (2)} | $T_A = 25^\circ\text{C}$, $I_{NP} = I_{NN} = \text{HGND}$ | -0.15 | ± 0.02 | 0.15 | mV |
| TCV_{OS} | Input offset drift ^{(1) (2) (4)} | | -1 | ± 0.15 | 1 | $\mu\text{V}/^\circ\text{C}$ |
| E_G | Gain error ⁽¹⁾ | $T_A = 25^\circ\text{C}$ | -0.2% | $\pm 0.04\%$ | 0.2% | |
| TCE_G | Gain error drift ^{(1) (5)} | | -40 | ± 6 | 40 | ppm/ $^\circ\text{C}$ |
| | Nonlinearity ⁽¹⁾ | | -0.04% | $\pm 0.002\%$ | 0.04% | |
| | Nonlinearity drift ⁽¹⁾ | | | 0.9 | | ppm/ $^\circ\text{C}$ |
| SNR | Signal-to-noise ratio | $V_{IN} = 0.5\text{ V}_{PP}$, $f_{IN} = 1\text{ kHz}$, BW = 10 kHz, 10 kHz filter | 80 | 85 | | dB |
| | | $V_{IN} = 0.5\text{ V}_{PP}$, $f_{IN} = 10\text{ kHz}$, BW = 100 kHz, 1 MHz filter | 67 | 71 | | |
| THD | Total harmonic distortion ⁽³⁾ | $V_{IN} = 0.5\text{ V}_{PP}$, $f_{IN} = 10\text{ kHz}$, BW = 100 kHz | | -85 | | dB |
| | Output noise | $I_{NP} = I_{NN} = \text{HGND}$, $f_{IN} = 0\text{ Hz}$, BW = 100 kHz | | 300 | | μV_{RMS} |
| CMRR | Common-mode rejection ratio | $f_{IN} = 0\text{ Hz}$, $V_{CM\ min} \leq V_{CM} \leq V_{CM\ max}$ | | -97 | | dB |
| | | $f_{IN} = 10\text{ kHz}$, $V_{CM\ min} \leq V_{CM} \leq V_{CM\ max}$ | | -98 | | |
| PSRR | Power-supply rejection ratio | VDD from 3.0 V to 5.5 V, at dc, input referred | | -109 | | dB |
| | | $I_{NP} = I_{NN} = \text{HGND}$, VDD from 3.0 V to 5.5 V, 10 kHz / 100 mV ripple, input referred | | -98 | | |

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ to 5.5 V , $\text{INP} = -250\text{ mV}$ to $+250\text{ mV}$, $\text{INN} = \text{HGND} = 0\text{ V}$, and the external components listed in the *Typical Application* section; typical specifications are at $T_A = 25^\circ\text{C}$, and $V_{DD} = 3.3\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----|------|------|------|
| POWER SUPPLY | | | | | | |
| IDD | Low-side supply current | no external load on HLDO | | 27.5 | 40 | mA |
| | | 1 mA external load on HLDO | | 29.5 | 42 | |
| V _{DCDC_OUT} | DCDC output voltage | DCDC_OUT to HGND | 3.1 | 3.5 | 4.65 | V |
| V _{DCDCUV} | DCDC output undervoltage detection threshold voltage | DCDC output falling | 2.1 | 2.25 | | V |
| V _{HLDO_OUT} | High-side LDO output voltage | HLDO to HGND, up to 1 mA external load | 3 | 3.2 | 3.4 | V |
| V _{HLDOUV} | High-side LDO output undervoltage detection threshold voltage | HLDO output falling | 2.4 | 2.6 | | V |
| I _H | High-side supply current for auxiliary circuitry | Load connected from HLDO_OUT to HGND, non-switching | | | 1 | mA |
| t _{AS} | Analog settling time | VDD step to 3.0 V, to OUTP and OUTN valid, 0.1% settling | | 0.9 | 1.4 | ms |

- (1) The typical value includes one standard deviation ("sigma") at nominal operating conditions.
- (2) This parameter is input referred.
- (3) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
- (4) Offset error temperature drift is calculated using the box method, as described by the following equation:

$$TCV_{OS} = (Value_{MAX} - Value_{MIN}) / TempRange$$
- (5) Gain error temperature drift is calculated using the box method, as described by the following equation:

$$TCE_G (\text{ppm}) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25^\circ\text{C})} \times TempRange) \times 10^6$$

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|-------------------|-----|-----|-----|---------------|
| t_r | Output signal rise time | | | 1.3 | | μs |
| t_f | Output signal fall time | | | 1.3 | | μs |
| | V_{INx} to V_{OUTx} signal delay (50% – 10%) | Unfiltered output | | 1 | 1.5 | μs |
| | V_{INx} to V_{OUTx} signal delay (50% – 50%) | Unfiltered output | | 1.6 | 2.1 | μs |
| | V_{INx} to V_{OUTx} signal delay (50% – 90%) | Unfiltered output | | 2.5 | 3 | μs |

6.11 Timing Diagram

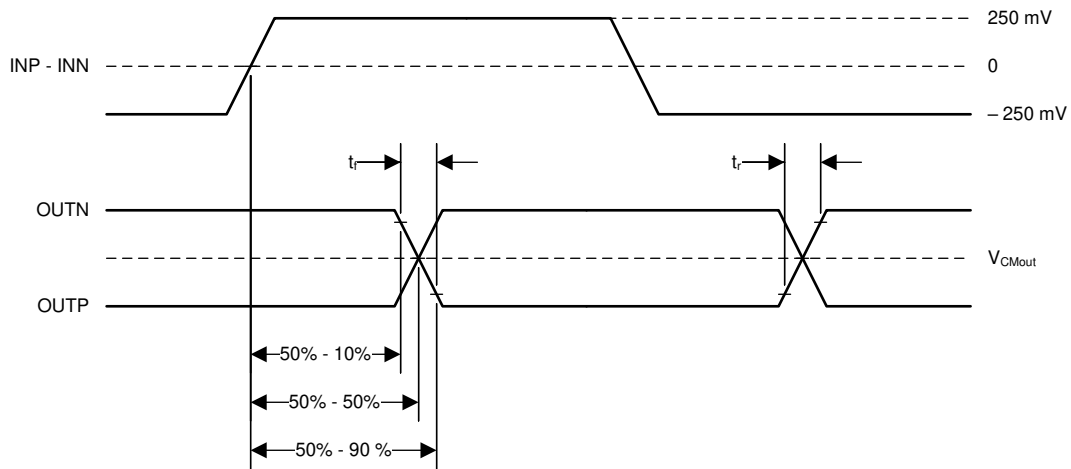


Figure 6-1. Rise, Fall, and Delay Time Waveforms

6.12 Insulation Characteristics Curves

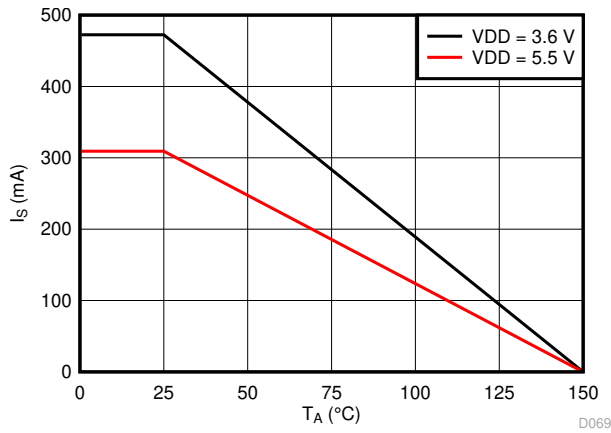


Figure 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

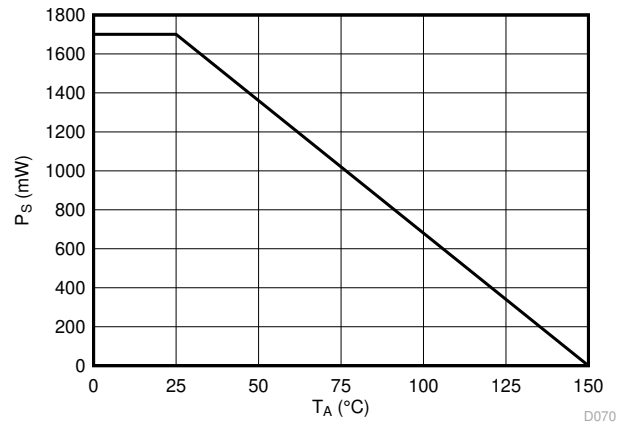
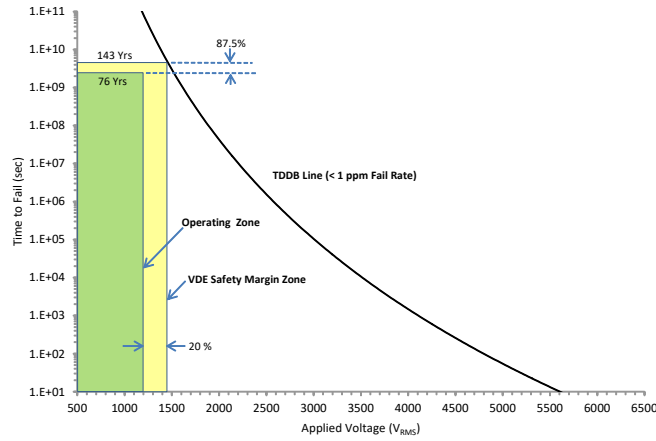


Figure 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1200 V_{RMS} , operating lifetime = 76 years

Figure 6-4. Reinforced Isolation Capacitor Lifetime Projection

6.13 Typical Characteristics

at VDD = 3.3 V, INP = -250 mV to +250 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

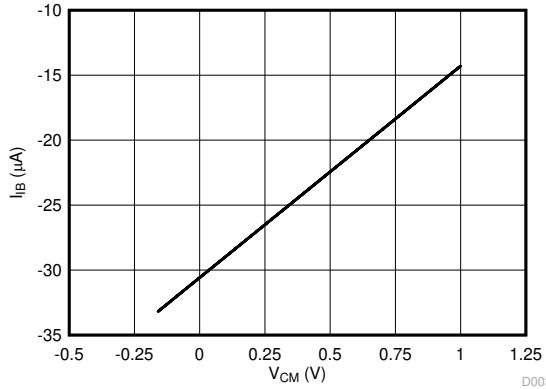


Figure 6-5. Input Bias Current vs Common-Mode Input Voltage

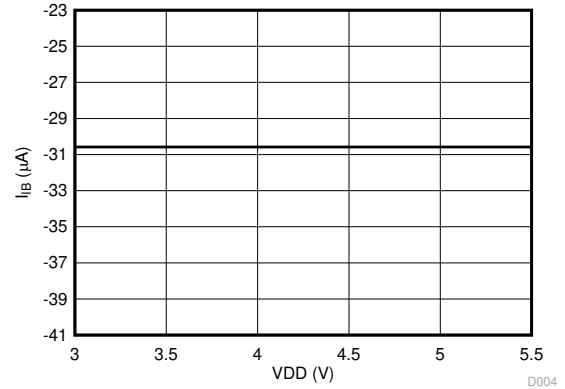


Figure 6-6. Input Bias Current vs Supply Voltage

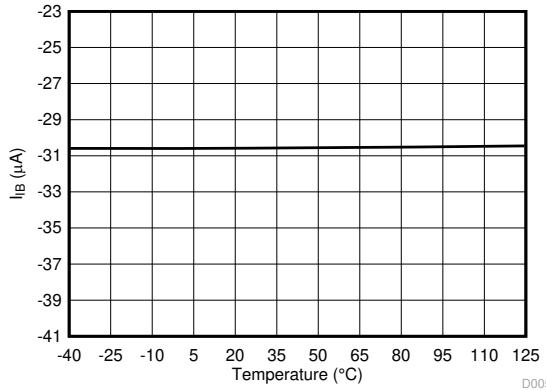


Figure 6-7. Input Bias Current vs Temperature

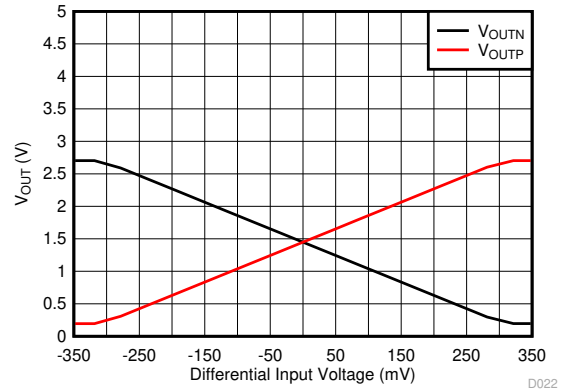


Figure 6-8. Output Voltage vs Input Voltage

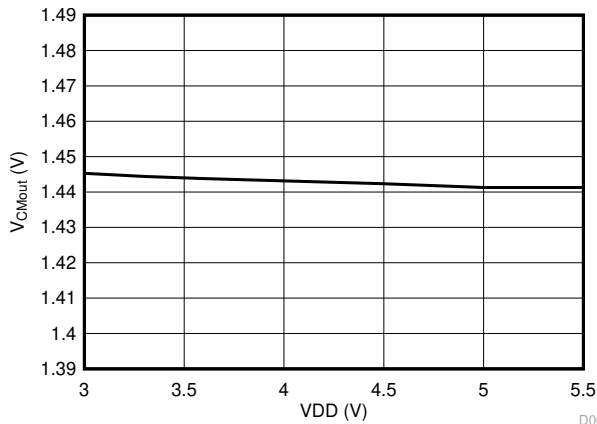


Figure 6-9. Output Common-Mode Voltage vs Supply Voltage

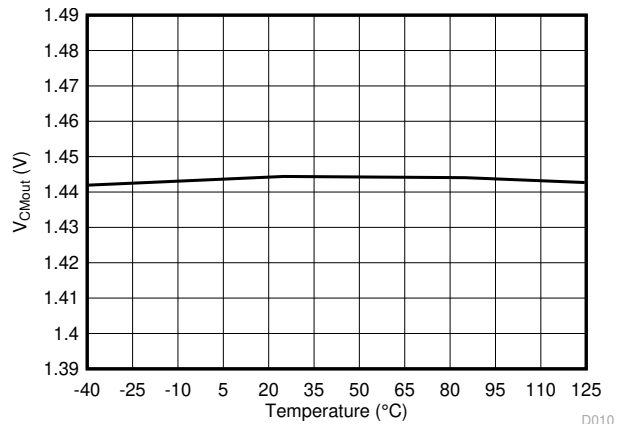


Figure 6-10. Output Common-Mode Voltage vs Temperature

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = -250 mV to +250 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

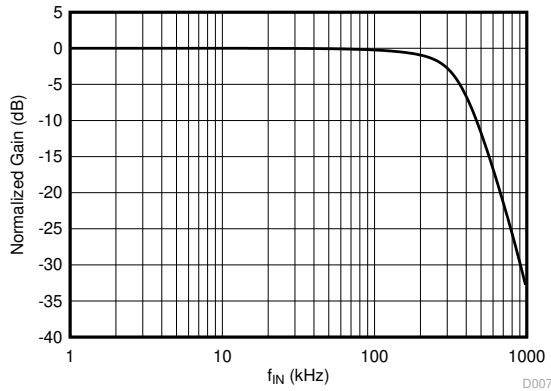


Figure 6-11. Normalized Gain vs Input Frequency

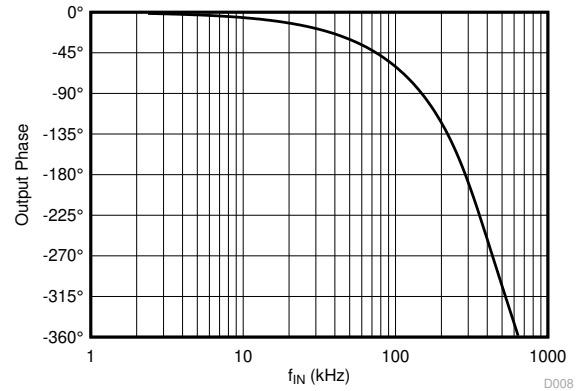


Figure 6-12. Output Phase vs Input Frequency

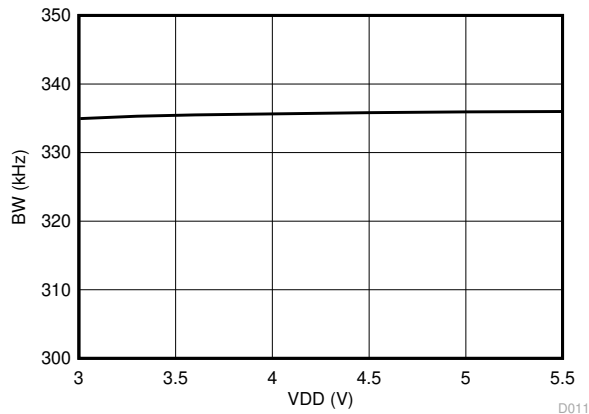


Figure 6-13. Output Bandwidth vs Supply Voltage

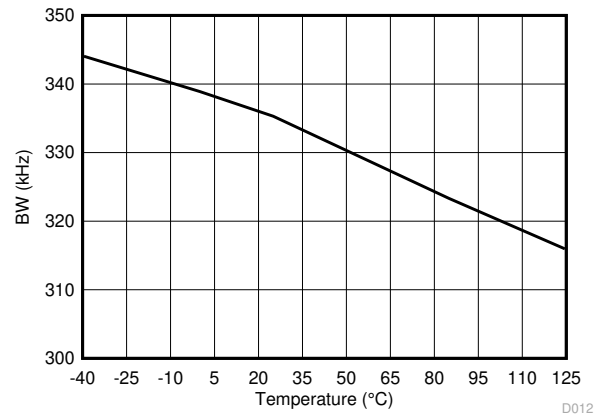


Figure 6-14. Output Bandwidth vs Temperature

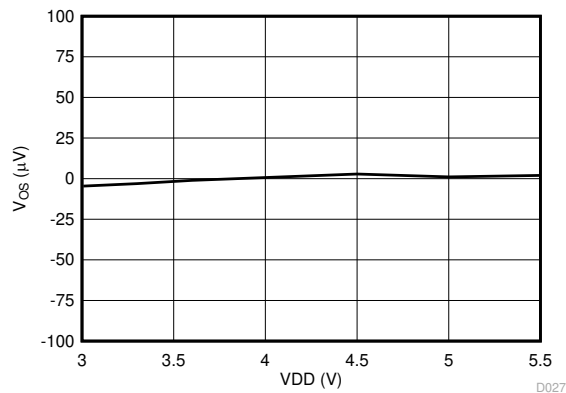


Figure 6-15. Input Offset Voltage vs Supply Voltage

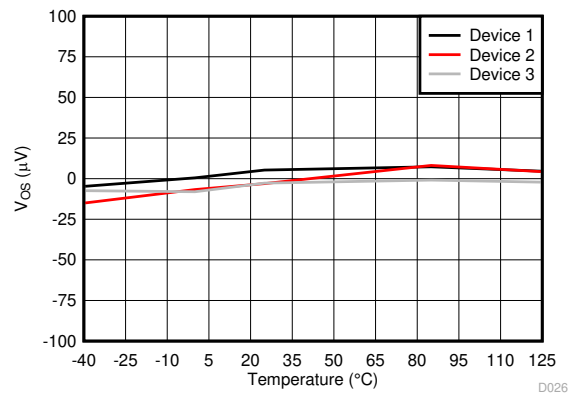


Figure 6-16. Input Offset Voltage vs Temperature

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = -250 mV to +250 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

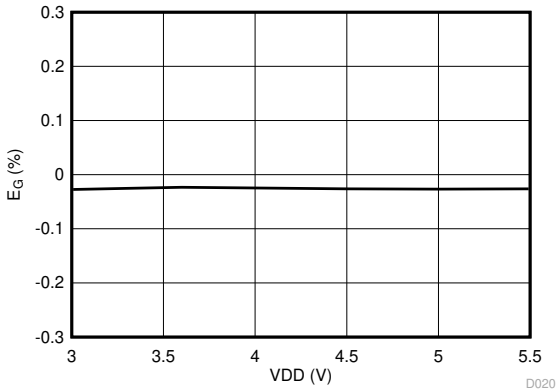


Figure 6-17. Gain Error vs Supply Voltage

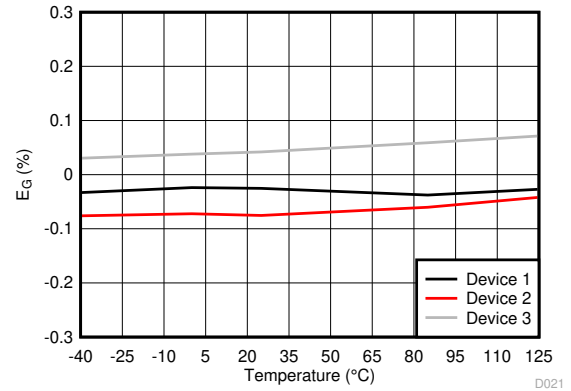


Figure 6-18. Gain Error vs Temperature

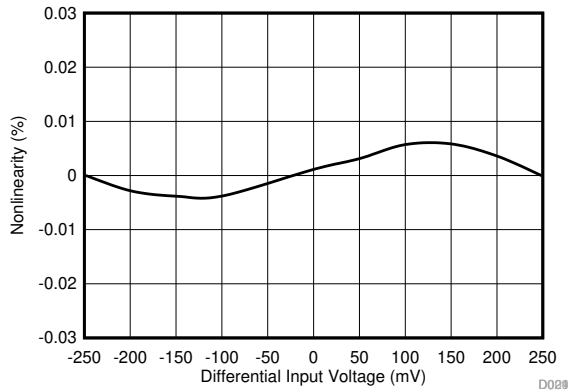


Figure 6-19. Nonlinearity vs Input Voltage

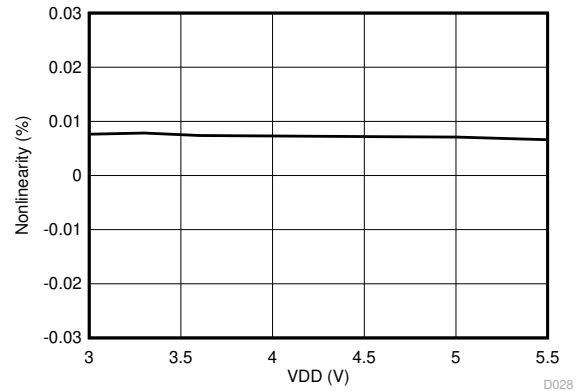


Figure 6-20. Nonlinearity vs Supply Voltage

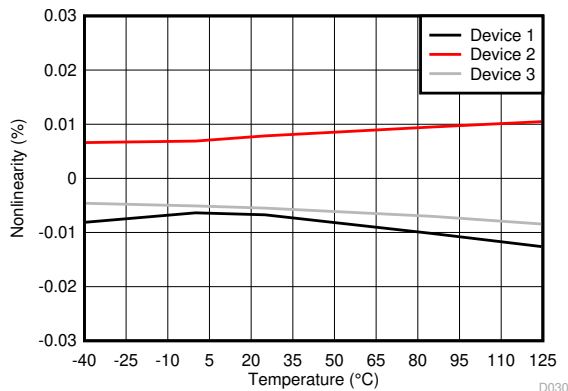


Figure 6-21. Nonlinearity vs Temperature

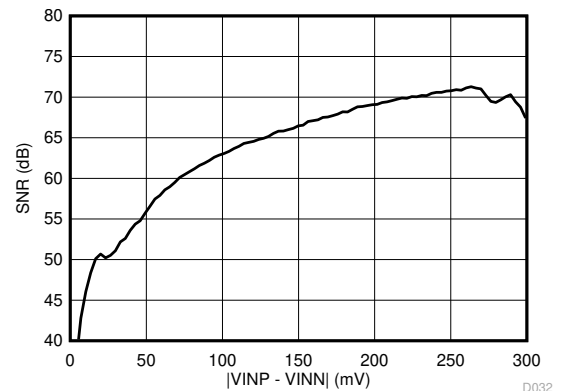


Figure 6-22. Signal-to-Noise Ratio vs Input Voltage

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = -250 mV to +250 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

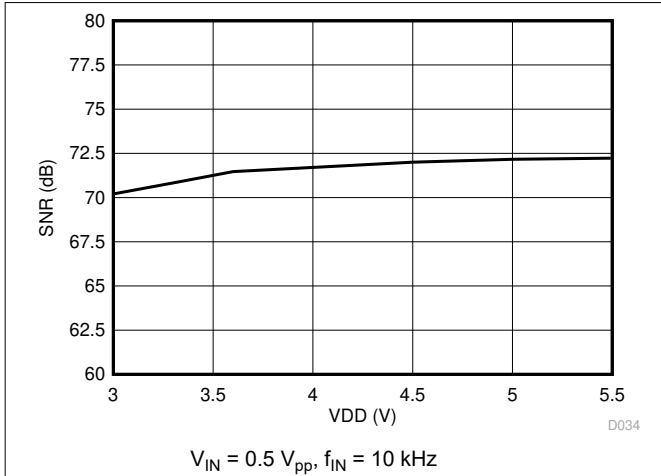


Figure 6-23. Signal-to-Noise Ratio vs Supply Voltage

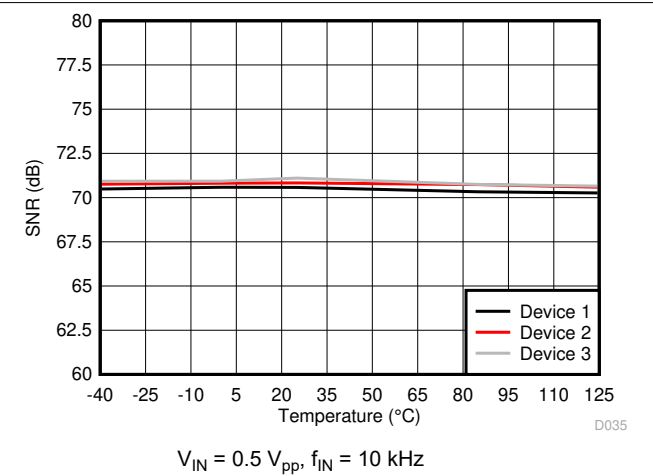


Figure 6-24. Signal-to-Noise Ratio vs Temperature

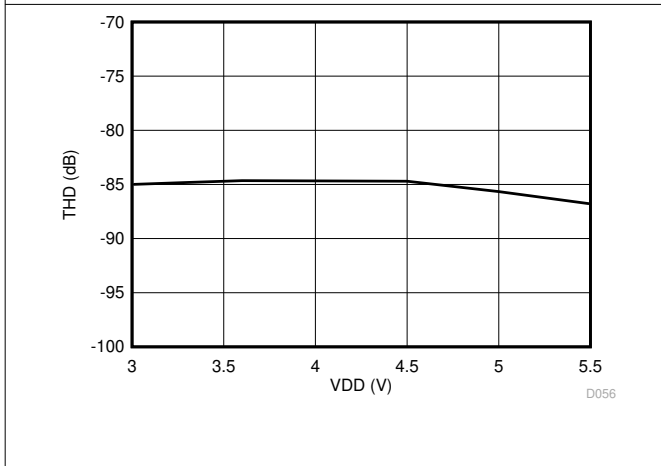


Figure 6-25. Total Harmonic Distortion vs Supply Voltage

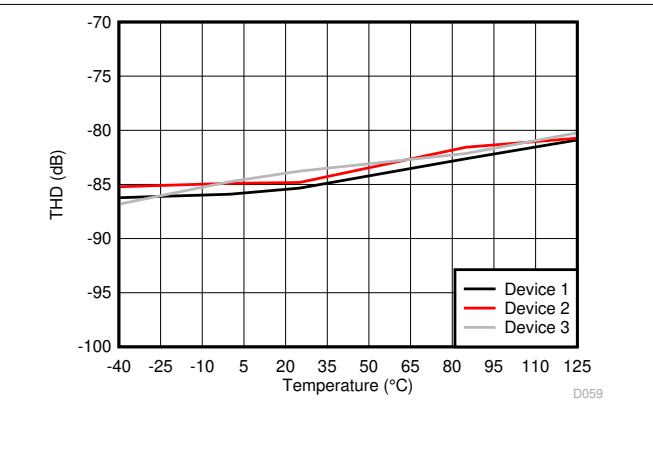


Figure 6-26. Total Harmonic Distortion vs Temperature

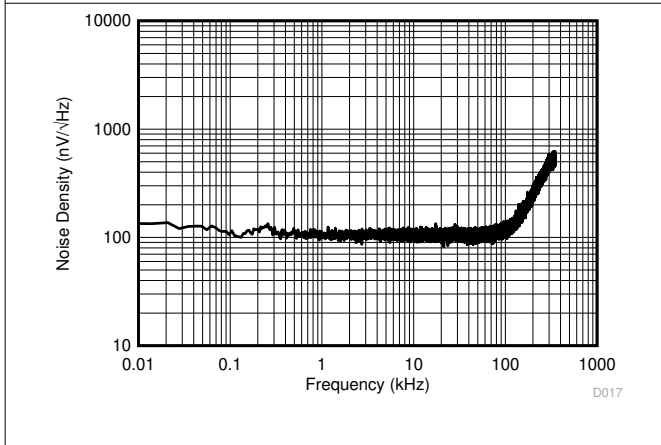


Figure 6-27. Input-Referred Noise Density vs Frequency

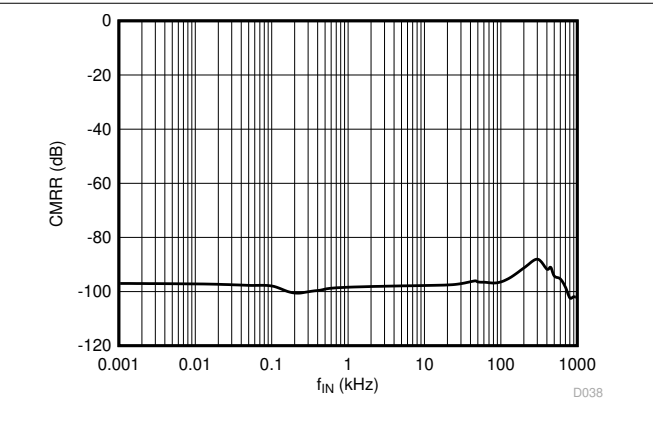


Figure 6-28. Common-Mode Rejection Ratio vs Input Frequency

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = -250 mV to +250 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

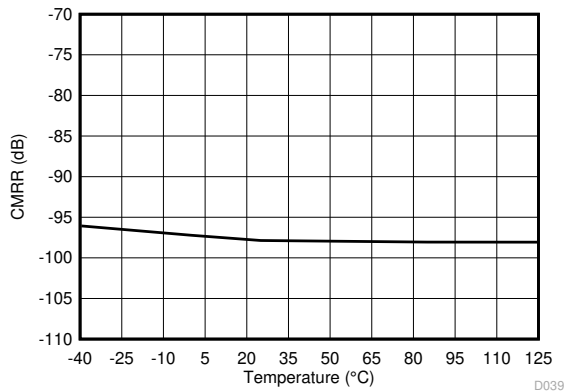


Figure 6-29. Common-Mode Rejection Ratio vs Temperature

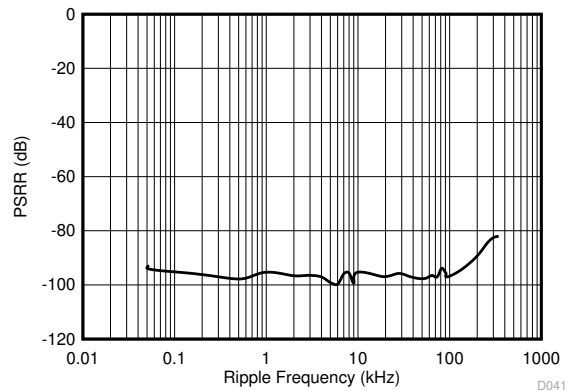


Figure 6-30. Power-Supply Rejection Ratio vs Ripple Frequency

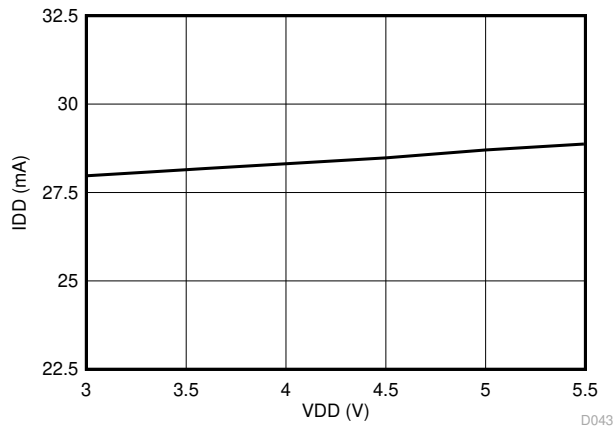


Figure 6-31. Supply Current vs Supply Voltage

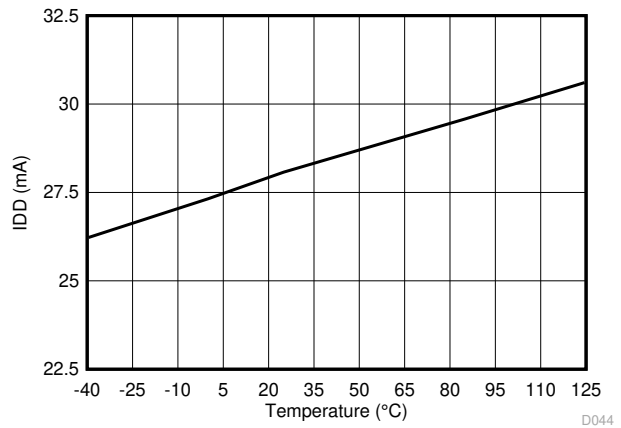


Figure 6-32. Supply Current vs Temperature

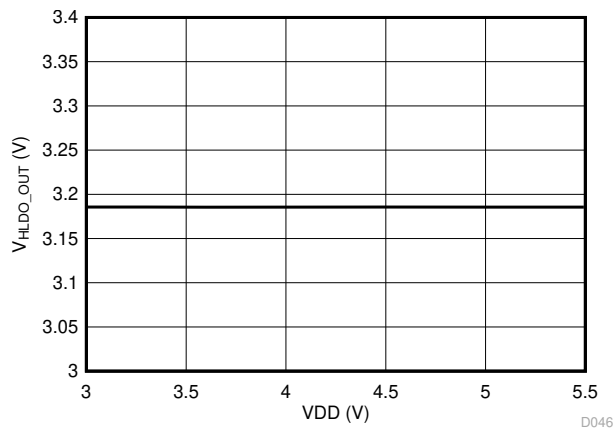


Figure 6-33. High-Side LDO Line Regulation

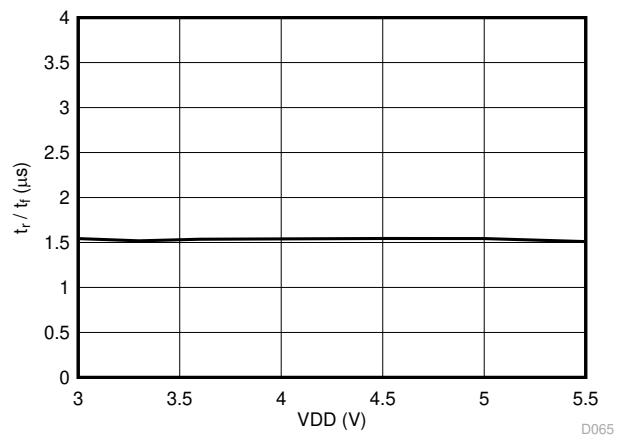


Figure 6-34. Output Rise and Fall time vs Supply Voltage

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = -250 mV to +250 mV, INN = HGND = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

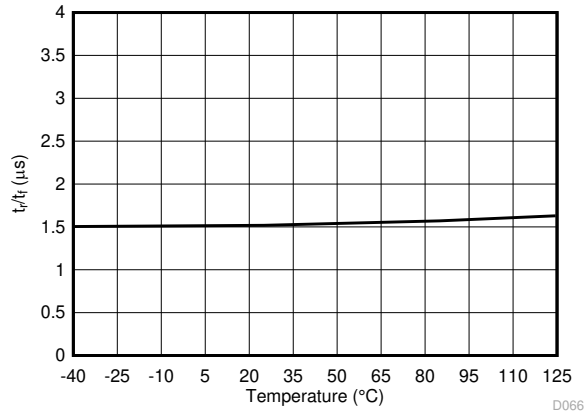


Figure 6-35. Output Rise and Fall Time vs Temperature

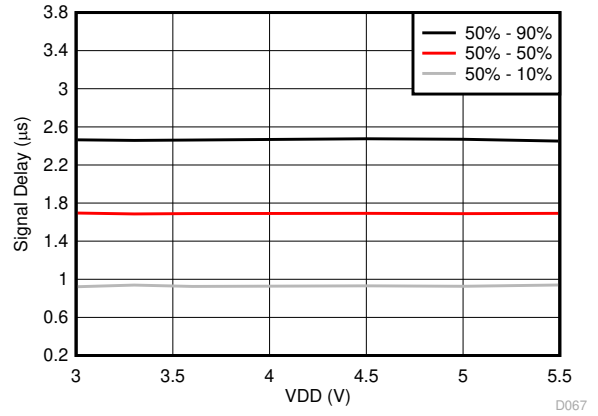


Figure 6-36. V_{IN} to V_{OUT} Signal Delay vs Supply Voltage

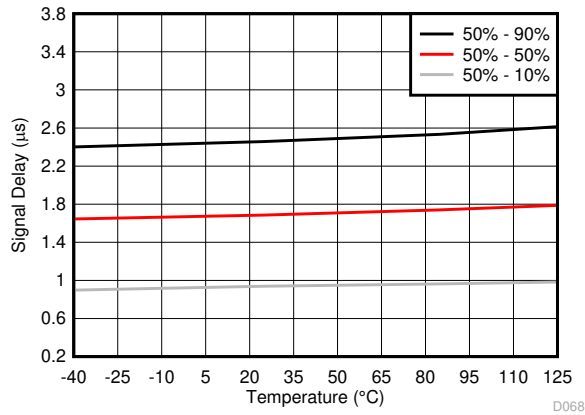


Figure 6-37. V_{IN} to V_{OUT} Signal Delay vs Temperature

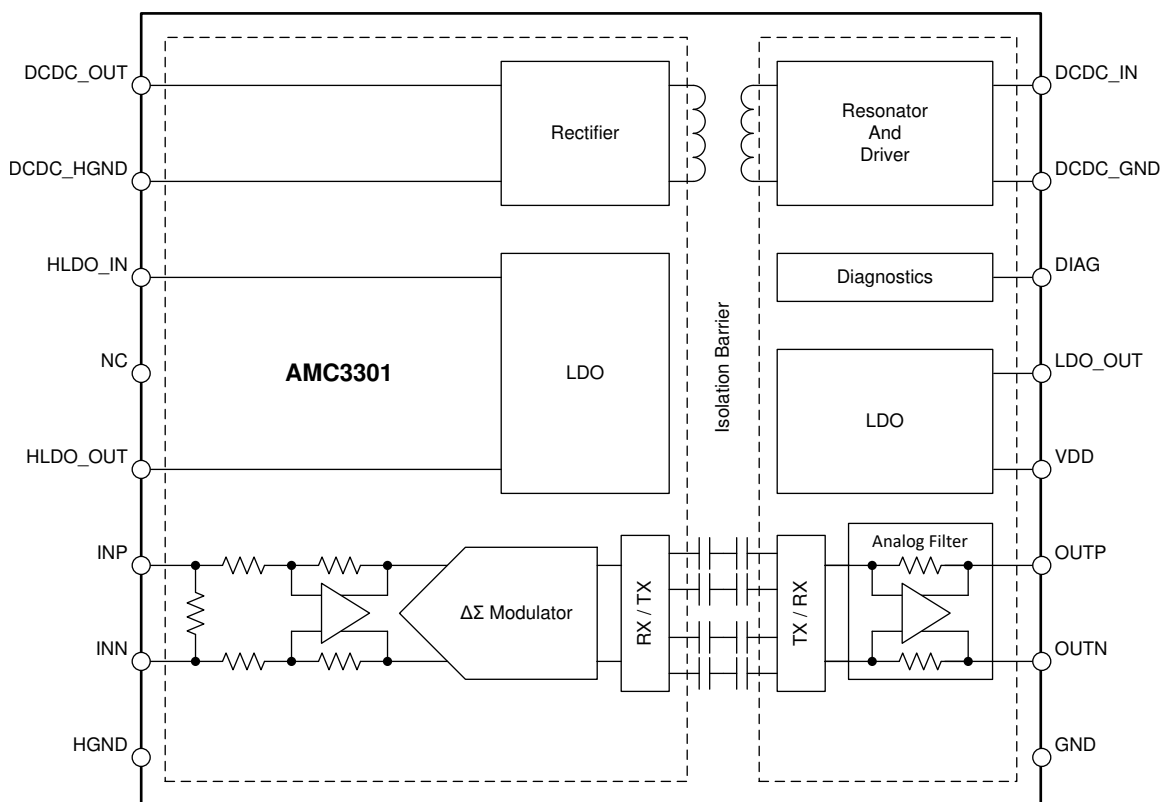
7 Detailed Description

7.1 Overview

The AMC3301 is a fully differential, precision, isolated amplifier with a fully integrated DC/DC converter that can supply the device from a single 3.3-V or 5-V voltage supply on the low-side. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator uses an internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (termed *TX* in the *Functional Block Diagram*) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. As shown in the *Functional Block Diagram*, the received bitstream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential output of the device.

The signal path is isolated by a double capacitive silicon dioxide (SiO_2) insulation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC3301 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R_{IND} . The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Data Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals (INP and INN). First, if the input voltages V_{INP} or V_{INN} exceed the range specified in the *Absolute Maximum Ratings* table, the input current must be limited to the absolute maximum value, because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within linear full-scale range (V_{FSR}) and within the common-mode input voltage range (V_{CM}) as specified in the *Recommended Operating Conditions* table.

7.3.2 Data Isolation Channel Signal Transmission

The AMC3301 uses an on-off keying (OOK) modulation scheme, as shown in [Figure 7-1](#), to transmit the modulator output bitstream across the capacitive SiO₂-based isolation barrier. The transmit driver (TX) shown in the [Functional Block Diagram](#) transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC3301 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and produces the output. The AMC3301 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

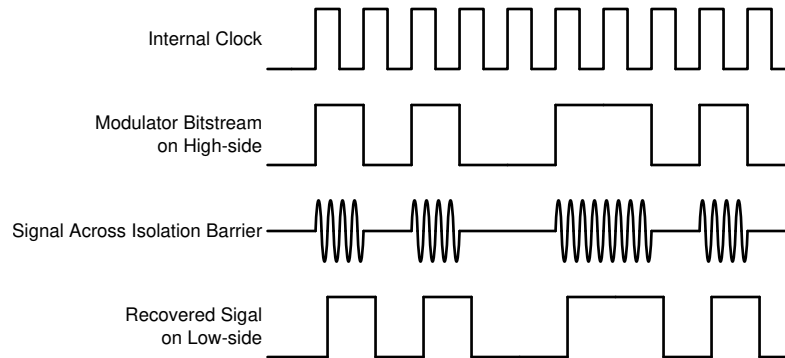


Figure 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC3301 offers a differential analog output comprised of the OOUTP and OOUTN pins. For differential input voltages ($V_{INP} - V_{INN}$) in the range from -250 mV to $+250$ mV, the device provides a linear response with a nominal gain of 8.2. For example, for a differential input voltage of 250 mV, the differential output voltage ($V_{OOUTP} - V_{OOUTN}$) is 2.05 V. At zero input (INP shorted to INN), both pins output the same common-mode output voltage V_{CMOut} , as specified in the [Electrical Characteristics](#) table. For absolute differential input voltages greater than 250 mV but less than 320 mV, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$ as shown in [Figure 7-2](#) if the differential input voltage exceeds the $V_{Clipping}$ value.

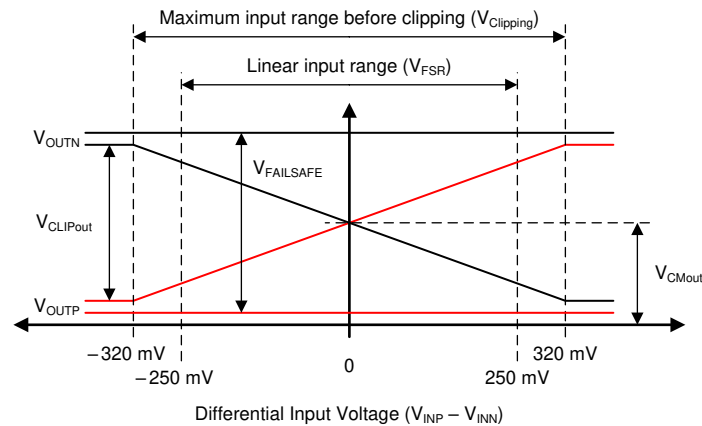


Figure 7-2. Output Behavior of the AMC3301

The AMC3301 provides a fail-safe output that simplifies diagnostics on system level. [Figure 7-2](#) shows the fail-safe mode, in which the AMC3301 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in two cases:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high side).
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds (brown-out).

Use the maximum $V_{FAILSAFE}$ voltage specified in the [Electrical Characteristics](#) table as a reference value for the fail-safe detection on the system level.

7.3.4 Isolated DC/DC Converter

The AMC3301 offers a fully integrated isolated DC/DC converter that includes the following components as illustrated in the [Functional Block Diagram](#):

- Low-dropout regulator (LDO) on the low-side to stabilize the supply voltage VDD that drives the low-side of the converter. This circuit does not output a constant voltage and is not intended for driving any external load.
- Low-side full-bridge inverter and drivers
- Laminate-based, air-core transformer for high-immunity to magnetic fields
- High-side full-bridge rectifier
- High-side LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path. The high-side LDO outputs a constant voltage and can provide a limited amount of current to power external circuitry.

The DC/DC converter uses a spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronized to the operation of the $\Delta\Sigma$ modulator to minimize the interference with data transmission and support the high analog performance of the device.

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC3301 and can source up to I_H of additional DC current for an optional auxiliary circuit such as an active filter, preamplifier, or comparator. I_H is specified in the [Electrical Characteristics](#) table as a DC, non-switching current.

7.3.5 Diagnostic Output

The open-drain DIAG pin can be monitored to confirm the device is operational and the output voltage is valid. As shown in [Figure 7-3](#), during power-up, the DIAG pin is actively held low until the high-side supply is in regulation and the device operates properly. During normal operation, the DIAG pin is in high-impedance (Hi-Z) state and is pulled high through an external pullup resistor. The DIAG pin is actively pulled low if:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high side). In this case, the amplifier outputs are driven to the V_{FAILSAFE} value that is shown in [Figure 7-2](#).
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds (brown-out). In this case, the low-side may still receive data from the high-side but the data may not be valid. The amplifier outputs are driven to the V_{FAILSAFE} value that is shown in [Figure 7-2](#).

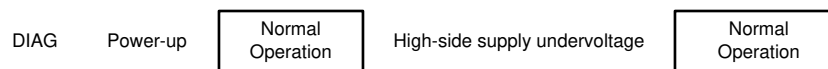


Figure 7-3. DIAG Output Under Different Operating Conditions

During normal operation, the DIAG pin is in a high-impedance state. Connect the DIAG pin to a pullup resistor or leave open if not used.

7.4 Device Functional Modes

The AMC3301 is operational when the power supply VDD is applied, as specified in the [Recommended Operating Conditions](#) table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The low input voltage range, low nonlinearity, and low temperature drift make the AMC3301 a high-performance solution for industrial applications where shunt-based current sensing with high common-mode voltage levels is required.

8.2 Typical Application

The AMC3301 is ideally suited for shunt-based current sensing applications where accurate current monitoring is required in the presence of high common-mode voltages. The AMC3301 integrates an isolated power supply for the high-voltage side and therefore makes the device particularly easy to use in applications that do not have a high-side supply readily available or where a high-side supply is referenced to a different ground potential than the signal to be measured.

Figure 8-1 shows a simplified schematic of the AMC3301 in a solar inverter where the phase current is measured on the grid-side of an LCL filter. Although the system offers a supply for the high-side gate driver, there is a large common-mode voltage between the gate driver supply ground reference and the shunt resistor on the other side of the LCL filter. Therefore, the gate driver supply is not suitable for powering the high-side of an isolated amplifier that measures the voltage across the shunt. The integrated isolated power supply of the AMC3301 solves that problem and enables current sensing at locations that is optimal for the system.

The diagram also shows the AMC3330 being used for sensing the AC output voltage.

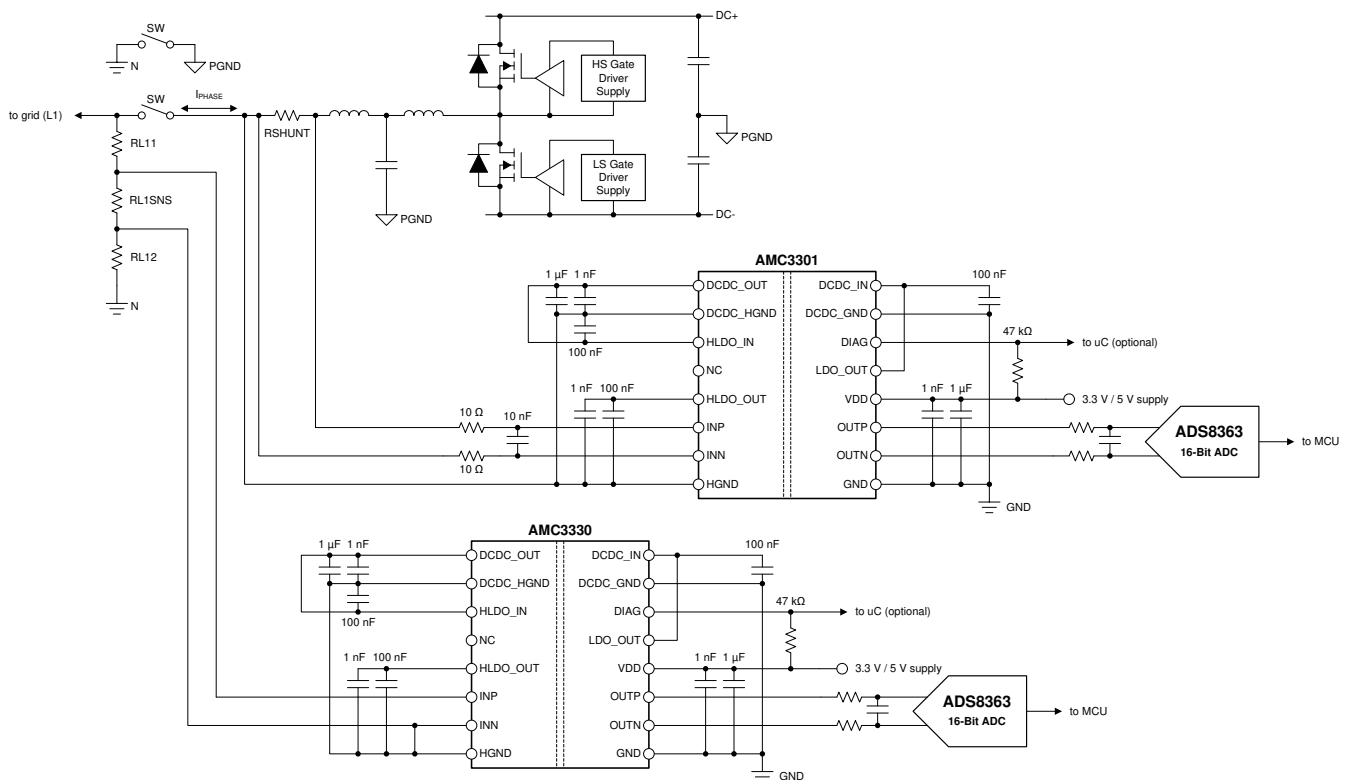


Figure 8-1. The AMC3301 in a Solar Inverter Application

8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

| PARAMETER | VALUE |
|---|------------------------|
| Supply voltage | 3.3 V or 5 V |
| Voltage drop across the shunt for a linear response (V_{SHUNT}) | ± 250 mV (maximum) |

8.2.2 Detailed Design Procedure

The AMC3301 requires a single 3.3-V or 5-V supply on its low-side. The high-side supply is internally generated by an integrated DC/DC converter as explained in the [Isolated DC/DC Converter](#) section.

The ground reference (HGND) is derived from the terminal of the shunt resistor that is connected to the negative input of the AMC3301 (INN). If a four-pin shunt is used, the inputs of the AMC3301 are connected to the inner leads and HGND is connected to one of the outer shunt leads. To minimize offset and improve accuracy, set the ground connection to a separate trace that connects directly to the shunt resistor rather than shorting HGND to INN directly at the input to the device. See the [Layout](#) section for more details.

8.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor, R_{SHUNT} :

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $|V_{SHUNT}| \leq |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

8.2.2.2 Input Filter Design

TI recommends placing an RC filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the $\Delta\Sigma$ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications, the structure shown in [Figure 8-2](#) achieves excellent performance.

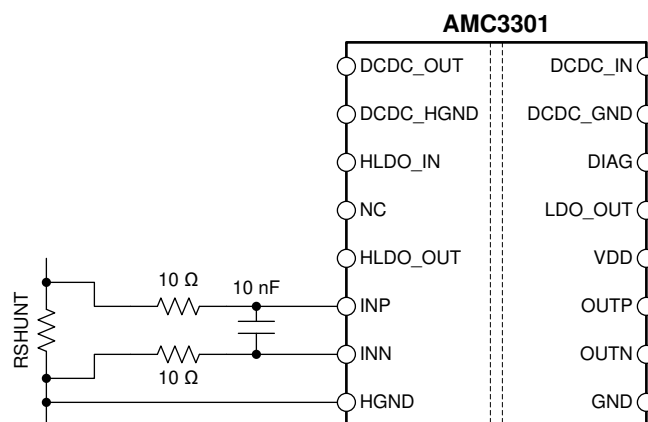


Figure 8-2. Differential Input Filter

8.2.2.3 Differential to Single-Ended Output Conversion

Figure 8-3 shows an example of a TLV6001 based signal conversion and filter circuit for systems using single-ended-input ADCs to convert the analog output voltage into digital. With $R1 = R2 = R3 = R4$, the output voltage equals $(V_{OUTP} - V_{OUTN}) + V_{REF}$. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system. For most applications, $R1 = R2 = R3 = R4 = 3.3\text{ k}\Omega$ and $C1 = C2 = 330\text{ pF}$ yields good performance.

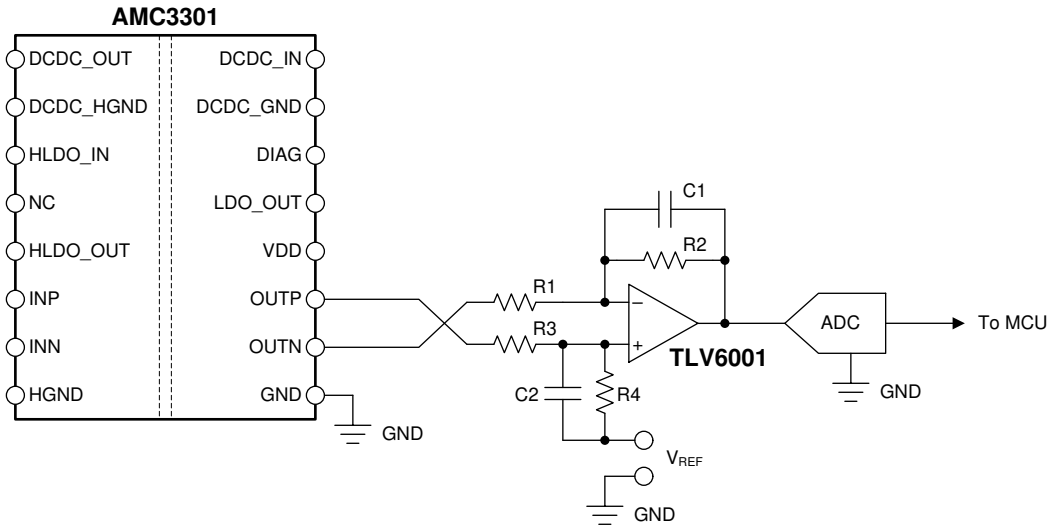


Figure 8-3. Connecting the AMC3301 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of successive-approximation-register (SAR) ADCs, see the [18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise reference guide](#) and [18-Bit Data Acquisition Block \(DAQ\) Optimized for Lowest Power reference guide](#), available for download at www.ti.com.

8.2.3 Application Curve

In frequency inverter applications, the power switches must be protected in case of an overcurrent condition. To allow for fast powering off of the system, a low delay caused by the isolated amplifier is required. Figure 8-4 shows the typical full-scale step response of the AMC3301. Consider the delay of the required window comparator and the MCU to calculate the overall response time of the system.

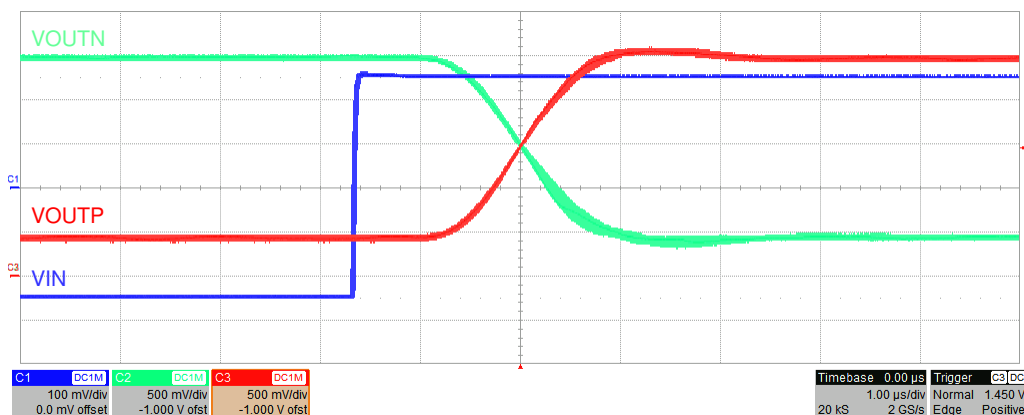


Figure 8-4. Step Response of the AMC3301

8.2.4 What To Do and What Not To Do

Do not leave the analog inputs INP and INN of the AMC3301 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and the output of the device is undetermined.

Connect the negative input (INN) to the high-side ground (HGND), either by a hard short or through a resistive path. A DC current path between INN and HGND is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the [Recommended Operating Conditions](#) table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting AGND to INN directly at the input to the device. See the [Layout](#) section for more details.

The high-side LDO can source a limited amount of current (I_H) to power external circuitry. Take care not to overload the high-side LDO.

The low-side LDO does not output a constant voltage and is not intended for powering any external circuitry. Do not connect any external load to the HLDO_OUT pin.

9 Power Supply Recommendations

The AMC3301 is powered from the low-side power supply (VDD) with a nominal value of 3.3 V or 5 V. TI recommends a low-ESR decoupling capacitor of 1 nF (C8 in Figure 9-1) placed as close as possible to the VDD pin, followed by a 1- μ F capacitor (C9) to filter this power-supply path.

The low-side of the DC/DC converter is decoupled with a low-ESR 100-nF capacitor (C4) positioned close to the device between the DCDC_IN and DCDC_GND pins. Use a 1- μ F capacitor (C2) to decouple the high side in addition to a low-ESR, 1-nF capacitor (C3) placed as close as possible to the device and connected to the DCDC_OUT and DCDC_HGND pins.

For the high-side LDO, use low-ESR capacitors of 1-nF (C6), placed as close as possible to the AMC3301, followed by a 100-nF decoupling capacitor (C5).

The ground reference for the high-side (HGND) is derived from the terminal of the shunt resistor which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace to make this connection instead of shorting HGND to INN directly at the device input. The high-side DC/DC ground terminal (DCDC_HGND) is shorted to HGND directly at the device pins.

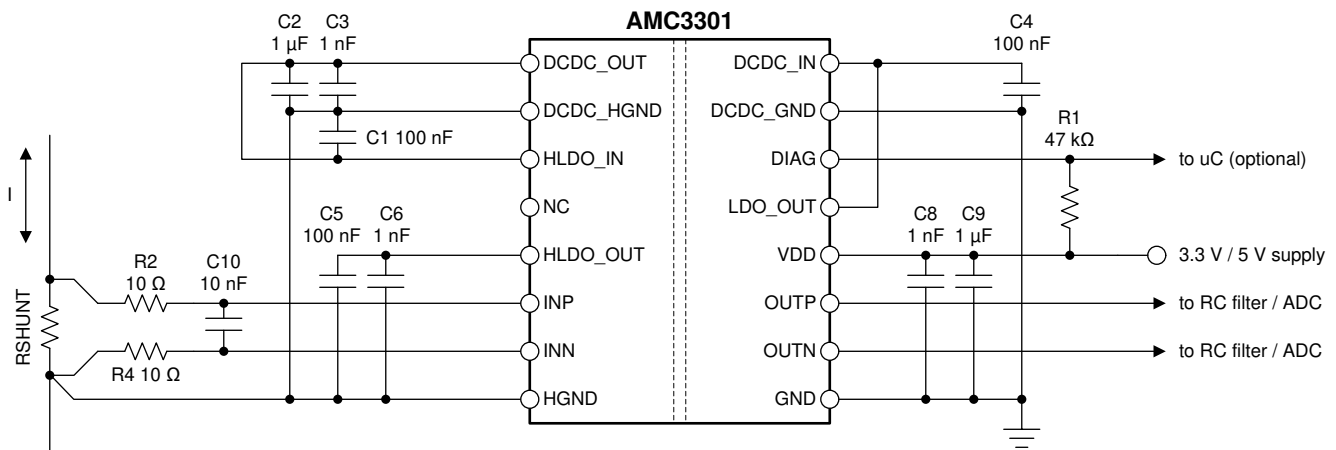


Figure 9-1. Decoupling the AMC3301

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

Table 9-1 lists components suitable for use with the AMC3301. This list is not exhaustive. Other components may exist that are equally suitable (or better), however these listed components have been validated during the development of the AMC3301.

Table 9-1. Recommended External Components

| DESCRIPTION | PART NUMBER | MANUFACTURER | SIZE (EIA, L x W) | |
|------------------------|-------------------------|----------------------|-------------------|-----------------------|
| VDD | | | | |
| C8 | 1 nF ± 10%, X7R, 50 V | 12065C102KAT2A | AVX | 1206, 3.2 mm x 1.6 mm |
| C9 | 1 µF ± 10%, X7R, 25 V | 12063C105KAT2A | AVX | 1206, 3.2 mm x 1.6 mm |
| DC/DC CONVERTER | | | | |
| C4 | 100 nF ± 10%, X7R, 50 V | C0603C104K5RACAUTO | Kemet | 0603, 1.6 mm x 0.8 mm |
| C3 | 1 nF ± 10%, X7R, 50 V | C0603C102K5RACTU | Kemet | 0603, 1.6 mm x 0.8 mm |
| C2 | 1 µF ± 10%, X7R, 25 V | CGA3E1X7R1E105K080AC | TDK | 0603, 1.6 mm x 0.8 mm |
| HLDO | | | | |
| C1 | 100 nF ± 10%, X7R, 50 V | C0603C104K5RACAUTO | Kemet | 0603, 1.6 mm x 0.8 mm |
| C5 | 100 nF ± 5%, NP0, 50 V | C3216NP01H104J160AA | TDK | 1206, 3.2 mm x 1.6 mm |
| C6 | 1 nF ± 10%, X7R, 50 V | 12065C102KAT2A | AVX | 1206, 3.2 mm x 1.6 mm |

10 Layout

10.1 Layout Guidelines

Figure 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors. The same component reference designators are used as in the *Power Supply Recommendations* section. Decoupling capacitors are placed as close as possible to the AMC3301 supply pins. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC3301 and keep the layout of both connections symmetrical.

To avoid causing errors in the measurement by the input bias currents of the AMC3301, connect the high-side ground pin (HGND) to the INN-side of the shunt resistor. Use a separate trace in the layout to make this connection to maintain equal currents in the INN and INP traces.

10.2 Layout Example

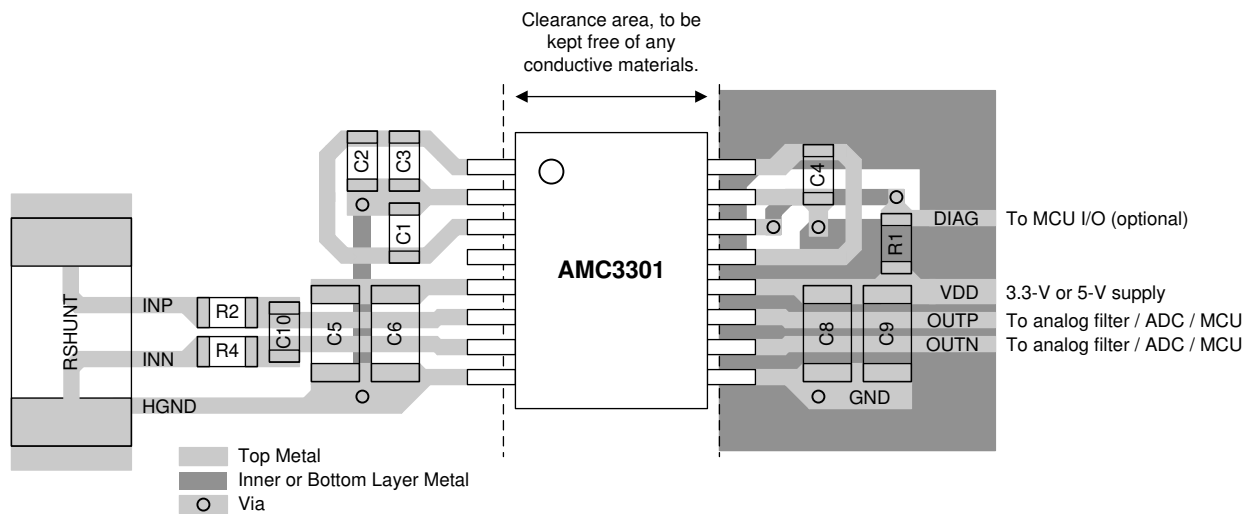


Figure 10-1. Recommended Layout of the AMC3301

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Texas Instruments, [Isolation Glossary](#)

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity](#) application report
- Texas Instruments, [AMC3330 Precision, \$\pm 1\$ -V Input, Reinforced Isolated Amplifier](#) data sheet
- Texas Instruments, [TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems](#) data sheet
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) reference guide
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#) reference guide

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| AMC3301DWE | ACTIVE | SOIC | DWE | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3301 | Samples |
| AMC3301DWER | ACTIVE | SOIC | DWE | 16 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3301 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

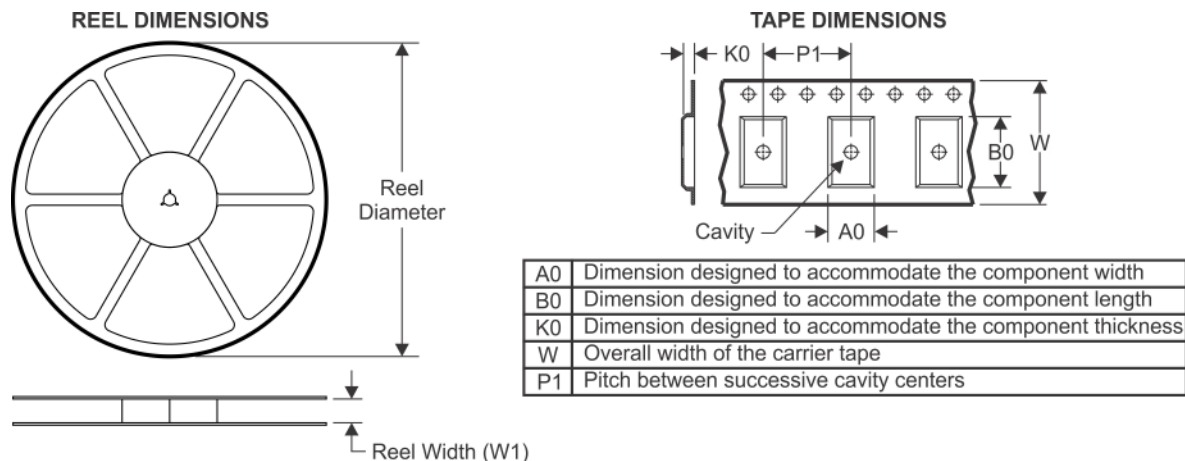
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AMC3301 :

- Automotive: [AMC3301-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

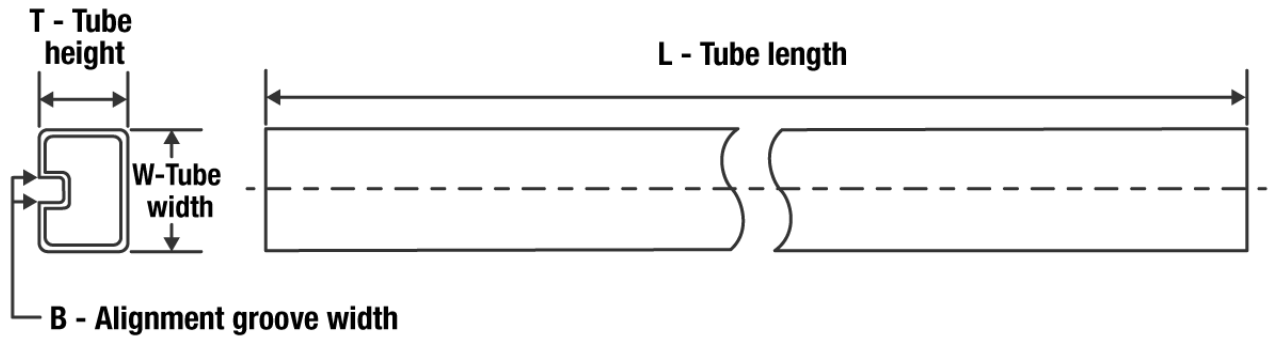

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AMC3301DWER | SOIC | DWE | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| AMC3301DWER | SOIC | DWE | 16 | 2000 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

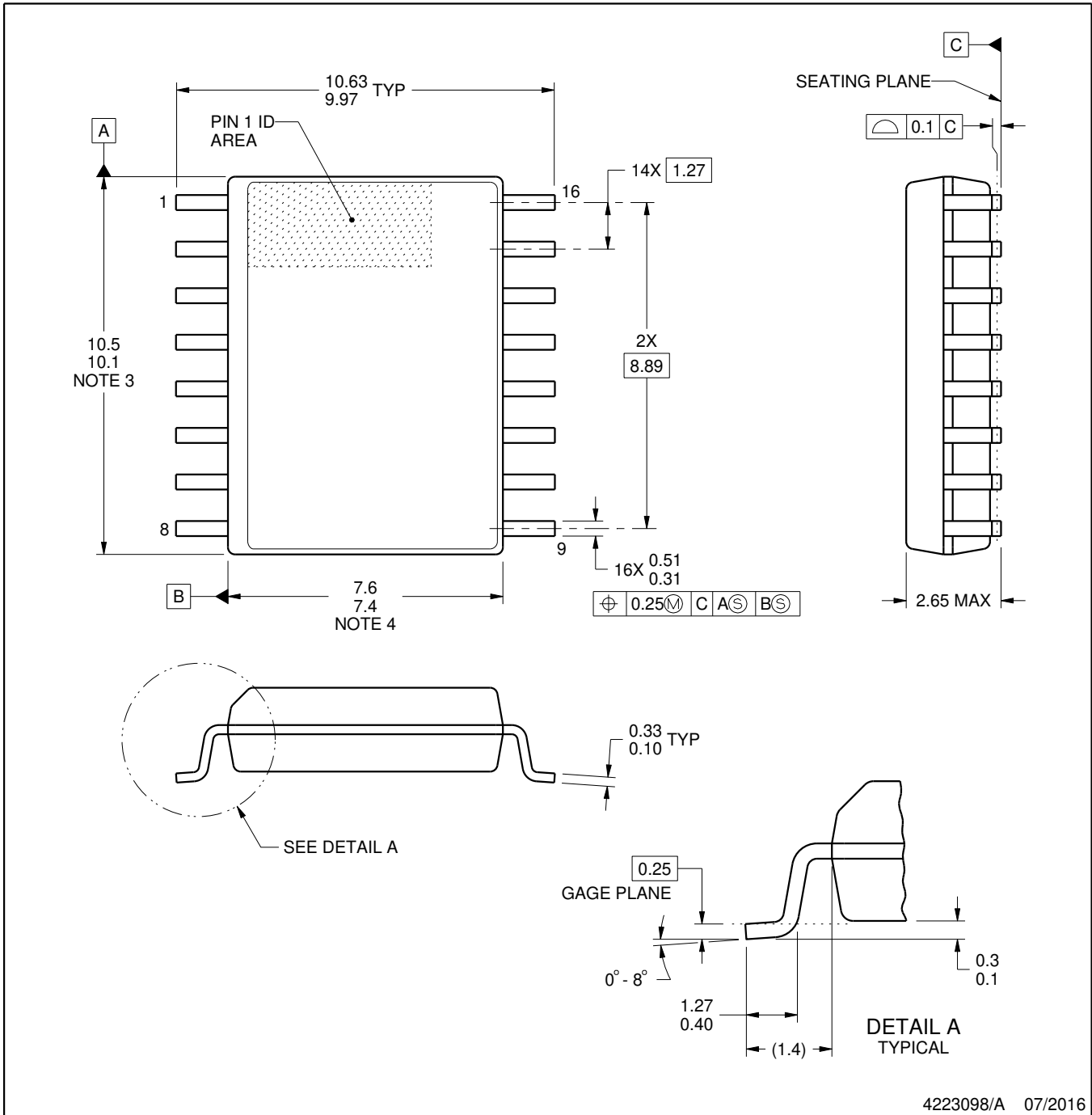
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| AMC3301DWE | DWE | SO-MOD | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |



DWE0016A

PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4223098/A 07/2016

NOTES:

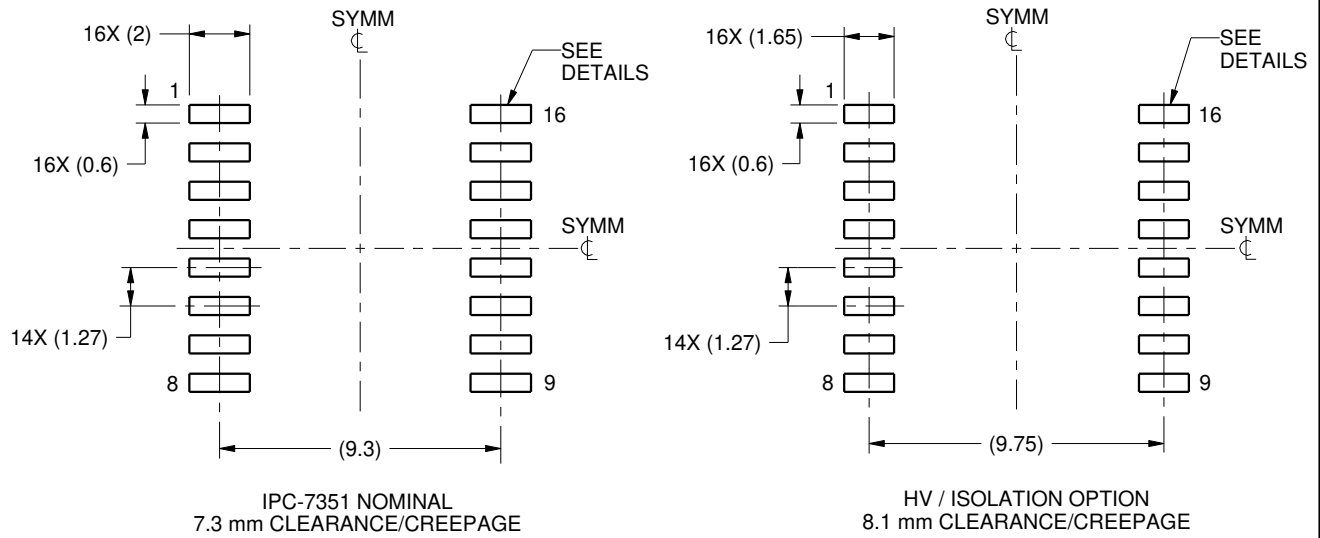
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

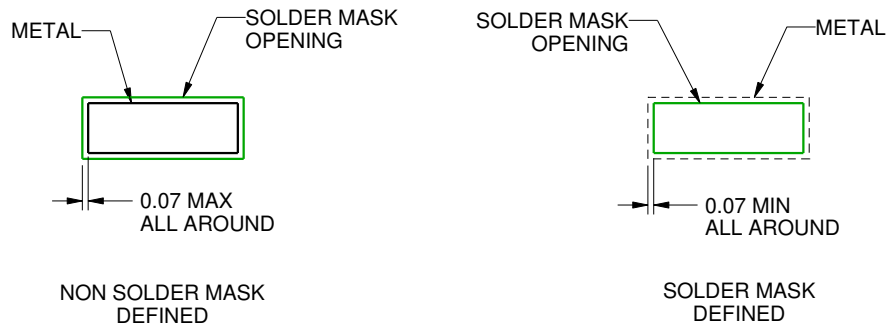
DWE0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4223098/A 07/2016

NOTES: (continued)

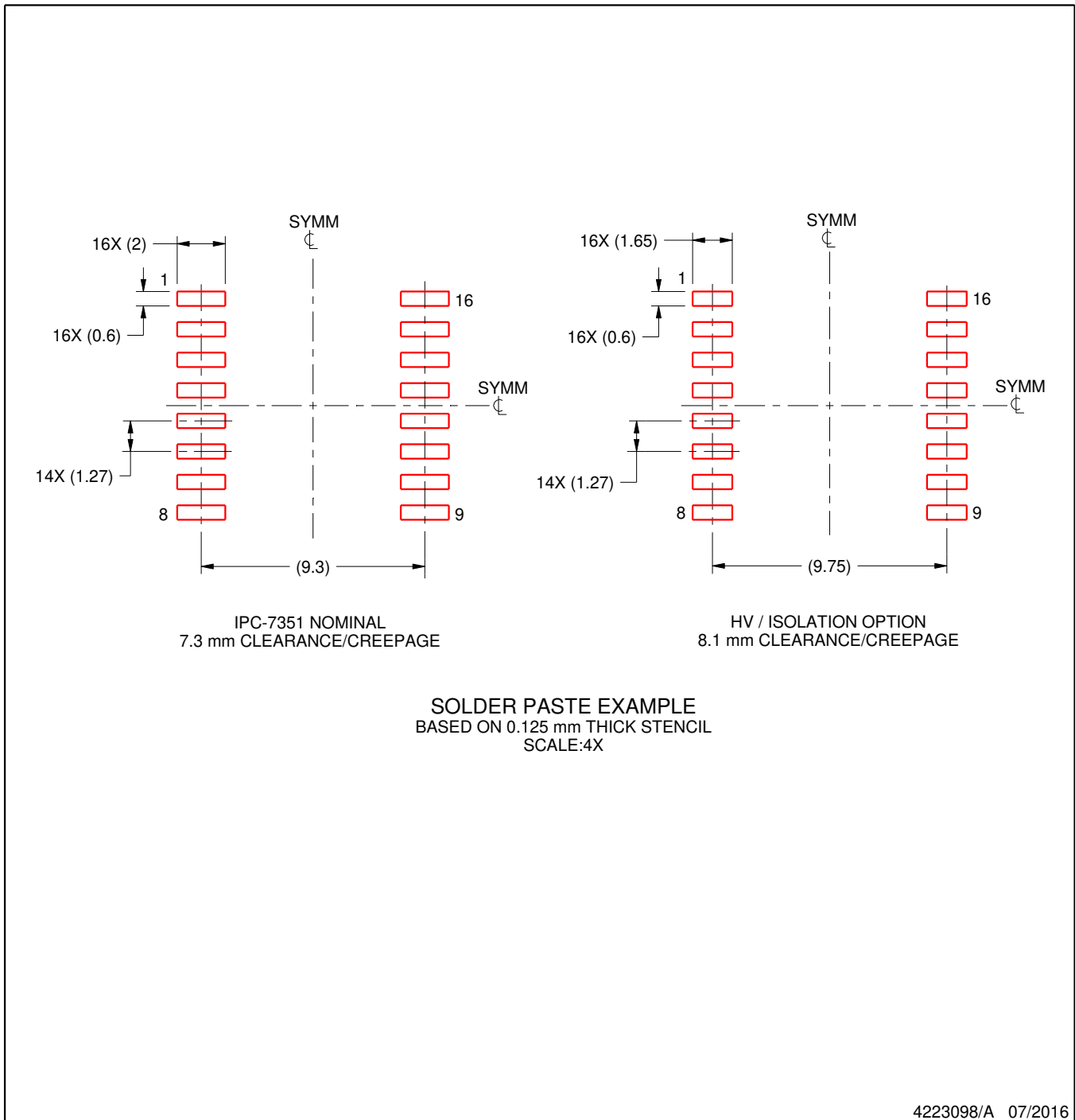
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DWE0016A

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated