User's Guide for bq25570 Battery Charger Evaluation Module for Energy Harvesting

This user's guide describes the bq25570 evaluation module (EVM), how to perform a stand-alone evaluation and how to allow the EVM to interface with the system and host. The boost charger output is configured to deliver up to 4.2-V maximum voltage to its output, VSTOR, using external resistors. This voltage will be applied to the storage element as long as the storage element voltage at VBAT is above the internally programmed undervoltage of 2.0 V. The integrated buck converter provides up to 1.8 V and 100 mA at VOUT. The VBAT_OK indicator toggles high when VSTOR ramps up to 3.0 V and toggles low when VSTOR ramps down to 2.8 V.

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1.1 EVM Features

- Evaluation module for bq25570
- Ultra-low power boost charger and buck converter with battery management for energy harvester applications
- Resistor-programmable settings for over voltage providing flexible battery management
- Programmable push-pull output indicator for battery status (VBAT_OK)
- Test points for key signals available for testing purpose – easy probe hook-up.
- Jumpers available – easy to change settings

1.2 General Description

The bq25570 is an integrated energy harvesting Nano-Power management solution that is well suited for meeting the special needs of ultra-low power applications. The product is specifically designed to efficiently acquire and manage the microwatts (µW) to miliwatts (mW) of power generated from a variety of high output impedance (HiZ) DC sources like photovoltaic (solar) or thermal electric generators; or with an AC/DC rectifier, a piezoelectric generator. The bq25570 implements a highly efficient, pulse-frequency modulated (PFM) boost converter/charger targeted toward products and systems, such as wireless sensor networks (WSN) which have stringent power and operational demands. Assuming a depleted storage element has been attached, the bq25570 DC-DC boost converter/charger that requires only microwatts of power to begin operating in cold start mode. Once the boost converter output, VSTOR, reaches ~1.8 V and can now power the converter, the main boost converter can now more efficiently extract power from low voltage output harvesters such as thermoelectric generators (TEGs) or single and dual cell solar panels. For example, assuming the HiZ input source can provide at least 5 µW typical and the load on VSTOR (including the storage element leakage current) is less than 1 µA of leakage current, the boost converter can be started with VIN_DC as low as 330 mV typical, and once VSTOR reaches 1.8 V, can continue to harvest energy down to VIN_DC ≈ 120 mV. The integrated PFM buck converter is also powered from VSTOR and, assuming enough input power is available, provides up to 100 mA from the VOUT pin. The VOUT voltage is externally programmed to slightly less than the VSTOR voltage.

HiZ DC sources have a maximum output power point (MPP) that varies with ambient conditions. For example, a solar panel's MPP varies with the amount of light on the panel and with temperature. The MPP is listed by the harvesting source manufacturer as a percentage of its open circuit (OC) voltage. Therefore, the bq25570 implements a programmable maximum power point tracking (MPPT) sampling network to optimize the transfer of power into the device. The bq25570 periodically samples the open circuit input voltage every 16 seconds by disabling the boost converter for 256 ms and stores the programmed MPP ratio of the OC voltage on the external reference capacitor (C2) at VREF_SAMP. Typically solar cells are at their MPP when loaded to ~70–80% of their OC voltage and TEGs at ~50%. While the storage element is less than the user programmed maximum voltage (VBAT_OV), the boost charger loads the harvesting source until VIN_DC reaches the MPP (voltage at VREF_SAMP). This results in the boost charger regulating the input voltage of the converter until the output reaches VBAT_OV, thus transferring the maximum amount of power currently available per ambient conditions to the output.

The battery undervoltage, VBAT_UV, threshold is checked continuously to ensure that the internal battery FET, connecting VSTOR to VBAT, does not turn on until VSTOR is above the VBAT_UV threshold (2.0 V).The over voltage (VBAT_OV) setting initially is lower than the programmed value at startup (varies on conditions) and is updated after the first ~32 ms. Subsequent updates are every ~64 ms. The VBAT_OV threshold sets maximum voltage on VSTOR and the boost converter stops switching when the voltage on VSTOR reaches the VBAT_OV threshold. The open circuit input voltage (VIN_OC) is measured every ~16 seconds in order for the Maximum Power Point Tracking (MPPT) circuit to sample and hold the input regulation voltage. This periodic update continually optimizes maximum power delivery based on the harvesting conditions.

The bq25570 was designed with the flexibility to support a variety of energy storage elements. The availability of the sources from which harvesters extract their energy can often be sporadic or time-varying. Systems will typically need some type of energy storage element, such as a re-chargeable battery, super capacitor, or conventional capacitor. The storage element will make certain constant power is available when needed for the systems. In general, the storage element also allows the system to handle any peak currents that can not directly come from the input source. It is important to remember that batteries and super capacitors can have significant leakage currents that need to be included with determining the loading on VSTOR.

To prevent damage to a customer's storage element, both maximum and minimum voltages are monitored against the internally programmed under-voltage (VBAT_UV) and user programmed over-voltage (VBAT_OV) levels.

To further assist users in the strict management of their energy budgets, the bq25570 toggles a user programmable battery good flag (VBAT_OK), checked every 64 ms, to signal the microprocessor when the voltage on an energy storage element or capacitor has risen above (OK_HYST threshold) or dropped below (OK_PROG threshold) a pre-set critical level. To prevent the system from entering an undervoltage condition or if starting up into a depleted storage element, it is highly recommended to isolate the system load from VSTOR by 1) setting VBAT_OK equal to the buck converter's enable signal VOUT_EN and 2) using an NFET to invert the BAT_OK signal so that it drives the gate of PFET, which isolates the system load from VSTOR.

For details, see the bq25570 data sheet (SLUSBH2).

1.3 Design and Evaluation Considerations

This user's guide is not a replacement for the data sheet. Reading the data sheet first will help in understanding the operations and features of this IC. In this document, "battery" or "VBAT" will be used but one could substitute any appropriate storage element.

System Design Tips

Compared to designing systems powered from an AC/DC converter or large battery (for example, low impedance sources), designing systems powered by HiZ sources requires that the system load-per-unit time (for example, per day for solar panel) be compared to the expected loading per the same time unit. Often there is not enough real time input harvested power (for example, at night for a solar panel) to run the system in full operation. Therefore, the energy harvesting circuit collects more energy than being drawn by the system when ambient conditions allow and stores that energy in a storage element for later use to power the system. See SLUC461 for an example spreadsheet on how to design a real solar-panel-powered system in three easy steps:

1. Referring the system rail power back to VSTOR
2. Referring the required VSTOR power back to bq255xx input power
3. Computing the minimum solar panel area from the input power requirement

As demonstrated in the spreadsheet, for any boost converter, you must perform a power balance, P_{OUT} / P_{IN} = (V_{STOR} × I_{STOR}) / (V_{IN} × I_{IN})= η where η is the estimated efficiency for the same or very similar configuration in order to determine the minimum input power needed to supply the desired output power.

This IC is a highly efficient charger for a storage element such as a battery or super capacitor. The main difference between a battery and a super capacitor is the capacity curve. The battery typically has little or no capacity below a certain voltage, where as the capacitor does have capacity at lower voltages. Both can have significant leakage currents that will appear as a DC load on VSTOR/VBAT.

1.4 EVM Schematic

Figure 1 is the schematic for this EVM.

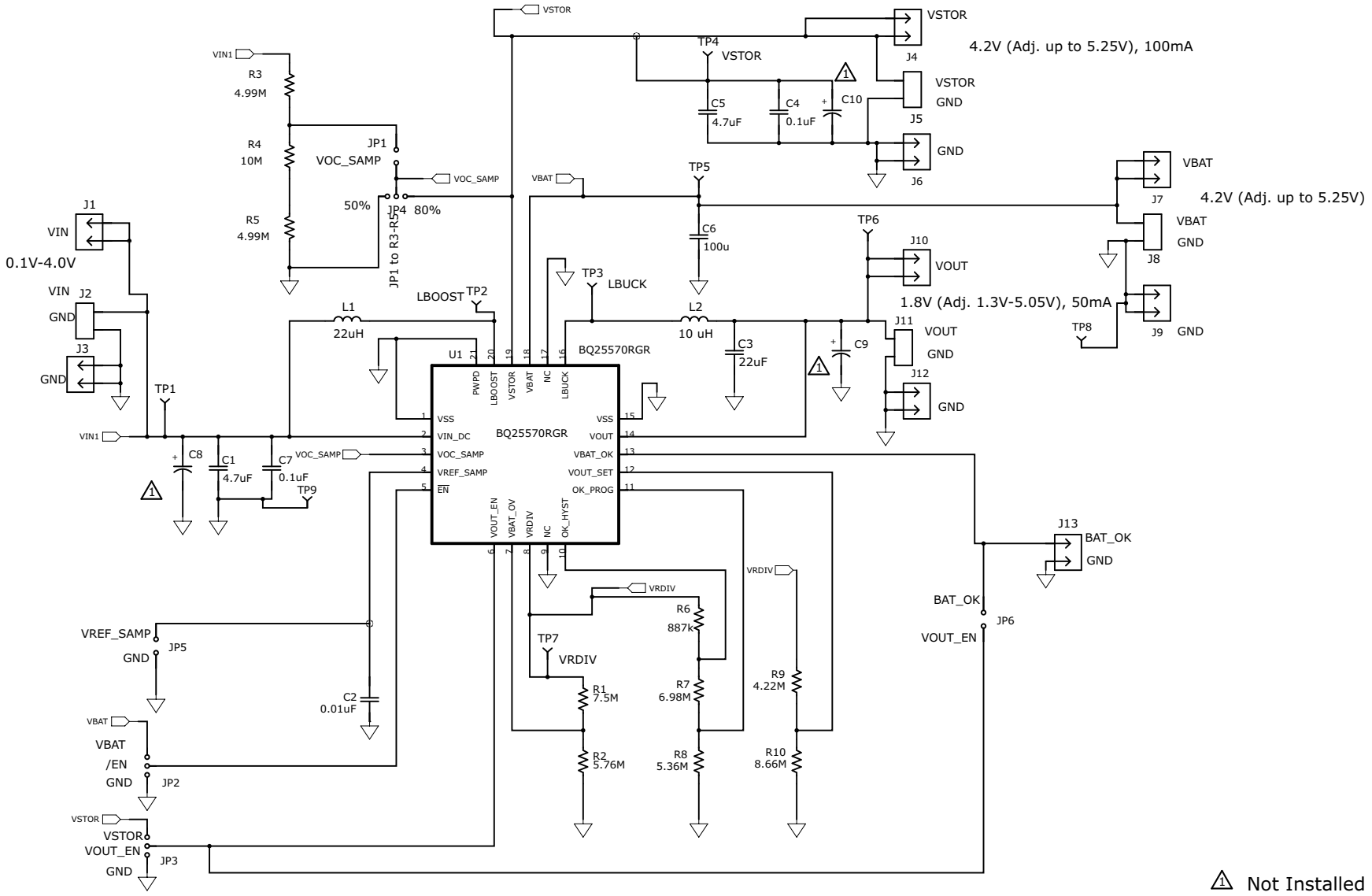


Figure 1. EVM Schematic

1.5 EVM I/O Connections

Table 1. I/O Connections and Configuration for Evaluation of bq25570 EVM

Headers and Terminals	Description	Comments/Recommended Setting
J1–VIN	Input source (+)	If VIN_DC is higher than VSTOR and VSTOR is equal to VBAT_OV, the input VIN_DC is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to VIN_DC be higher than 20 Ω and not a low impedance source.
J2 - VIN/GND	Input source terminal block	
J3–GND	Input source return (–)	
J4 - VSTOR	Boost charger output (+)	Buck converter input
J5 - VSTOR/GND	Boost charger output terminal block	
J6 - GND	Boost charger return (-)	
J7– VBAT	Rechargeable storage element connection (+)	
J8 - VBAT/GND	Rechargeable storage element terminal block	
J9–GND	Rechargeable storage element connection return (–)	
J10 – VOUT	Buck converter output (+)	
J11 - VOUT/GND	Buck converter output terminal block	
J12 -GND	Buck converter output (-)	
J13 – BAT_OK	Battery Status Indicator (+/-)	
Test Points		
TP1	Input source (+)	
TP2	Boost charger switching node	
TP3	Buck converter switching node	
TP4	Boost charger output, VSTOR (+)	
TP5	Rechargeable storage element connection, BAT_SEC (+)	
TP6	Buck converter output, VOUT (+)	
TP7	VRDIV node	CAUTION Providing an additional low impedance current path in parallel with the feedback resistors , for example, with a 10 MΩ scope probe attached, will degrade regulation accuracy.
TP8	Output return (-)	
TP9	Input return (-)	
Jumpers		
JP1 – VOC_SAMP	VOC_SAMP = external resistors sized to configure the IC to regulate VIN to 75% of VOC_SAMP.	Uninstalled (NOTE: Do not install if JP4 shunt is installed)
JP2 - /EN	/EN = GND enables the IC. /EN=VSTOR disables the IC.	/EN=GND
JP3 - VOUT_EN	VOUT_EN = VSTOR enables the buck converter when VSTOR is up VOUT_EN = GND disables the buck converter	VOUT_EN=VSTOR (NOTE: Do not install if JP6 shunt is installed)

Table 1. I/O Connections and Configuration for Evaluation of bq25570 EVM (continued)

Headers and Terminals	Description	Comments/Recommended Setting
JP4 - VOC_SAMP	VOC_SAMP = 80% configures the IC to regulate VIN to 80% of OCV. VOC_SAMP = 50% configures the IC to regulate VIN to 50% of OCV.	JP4 = 80% (NOTE: Do not install if JP1 shunt is installed)
JP5 - VREF_SAMP to GND	VREF_SAMP = GND	Uninstalled (NOTE: Providing an additional leakage path for the VREF_SAMP capacitor for example, through a 10 MΩ scope probe attached to VREF_SAMP, will degrade input voltage regulation performance).
JP6 - VBAT_OK to VOUT_EN	BAT_OK=VOUT_EN configures the buck converter to be enabled only when VSTOR is greater than the VBAT_OK threshold per the resistors (2.786V on the EVM)	Uninstalled (NOTE: Do not install if JP3 shunt is installed)

2 EVM Performance Specification Summary

See Data Sheet “Recommended Operating Conditions” for component adjustments. For details about the resistor programmable settings, see bq25570 data sheet (SLUSBH2).

		MIN	NOM	MAX	UNIT
V_{IN}(DC)	DC input voltage into VIN_DC	0.13		4.0	V
$V_{IN\_Start\text{-}up}$(DC)	DC minimum start-up voltage into depleted storage element, no load attached to VSTOR or VOUT and $IBAT_{LEAK}$ <=1uA		330		mV
V_{BAT_OV}	Battery Over Voltage Threshold –min and max values include +/- 2% set point accuracy and +/-1% resistor tolerance but excludes effects of output ripple	4.04	4.18	4.32	V
V_{OUT}	Buck Converter Output Voltage for I_{VOUT} < 95 mA - min and max values include +/- 2% set point regulation accuracy and +/-1% resistor tolerance but excludes effects of output voltage ripple, line regulation and load regulation	1.75	1.8	1.85	V
V_{BAT_OK}	OK_HYST indication toggles high when VSTOR ramps up - min and max values include +/- 2% set point accuracy and +/-1% resistor tolerance	2.70	2.79	2.88	V
	OK_PROG indication toggles low when VSTOR ramps down - min and max values include +/- 2% set point accuracy and +/-1% resistor tolerance	2.89	2.99	3.09	V
MPPT	Maximum Power Point Tracking, Resistor Programmed % of Open Circuit Voltage		80%		
C_{BAT}	A 100 µF low leakage ceramic capacitor is installed on the EVM as the minimum recommended equivalent battery capacitance.	100			µF

See SLUC484 spreadsheet tool to assist with modifying the MPPT, VBAT_OV, VBAT_OK and VOUT resistors for your application.

CAUTION

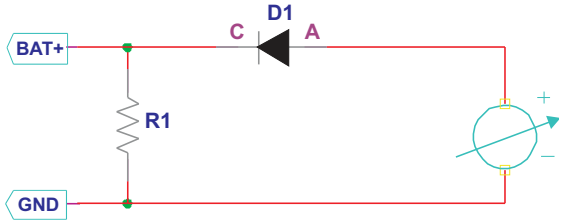
If changing the board resistors or the capacitor on VREF_SAMP (C2), it is important to remember that residual solder flux on a board has a resistivity in the 1-20 MΩ range. Therefore, flux remaining in parallel with changed 1-20 MΩ resistors can result in a lower effective resistances, which will produce different operating thresholds than expected. Similarly flux remaining in parallel with the VREF_SAMP capacitor provides an additional leakage path, which results in the input voltage regulation set point drooping during the 16-s MPPT cycle. Therefore, it is highly recommended that boards be throughly cleaned twice, once after removing the old components and again after installing the new components. If possible, the boards should be cleaned until the wash solution measures ionic contamination greater than 50 MΩ.

3 Test and Measurment Summary

Test Setup Tips

Energy harvesting power sources are high impedance sources. A source-meter configured as a current source with voltage compliance set to the harvester's open circuit voltage is the best way to simulate the harvester. When simulating a HiZ energy harvester with low output impedance lab power supply, it is necessary to simulate the harvester's impedance with a physical resistor between the supply, V_{PS}, and V_{IN} of the EVM. When the MPPT sampling circuit is active, V_{IN} = V_{PS} = the harvester open circuit voltage (VOC) because there is no input current to create a drop across the simulated impedance (that is, open circuit); therefore, VPS should be set to the intended harvester's open circuit voltage. When the boost converter is running, it draws only enough current until the voltage at VIN_DC droops to the MPPT's sampled voltage that is stored at VREF_SAMP.

The battery (storage element) can be replaced with a simulated battery. Often electronic 4 quadrant loads give erratic results with a “battery charger” due to the charger changing states (fast-charge to termination and refresh) while the electronic load is changing loads to maintain the “battery” voltage. The charging and loading get out of phase and create a large signal oscillation which is due to the 4 quadrant meter. A simple circuit can be used to simulate a battery and works well and can quickly be adjusted for voltage. It consists of load resistor (~10 Ω, 2 W) to pull the output down to some minimum storage voltage (sinking current part of battery) and a lab supply connected to the BAT pin via a diode. The lab supply biases up the battery voltage to the desired level. It may be necessary to add more capacitance across R1.



3.1 Test Setups and Results

3.1.1 Boost Charger Efficiency

The test setup is shown in Figure 2. The specific equipment used for the test results in Figure 3 and Figure 4 is listed below:

1. VIN_DC was connected to a Keithley 2420 source-meter configured as a current source with voltage compliance (clamp) set to the open circuit voltage.
2. VSTOR was connected a Keithley 2420 source-meter configured as a voltage source set to the VSTOR voltage. The current sunk by the source-meter was the output current of the charger

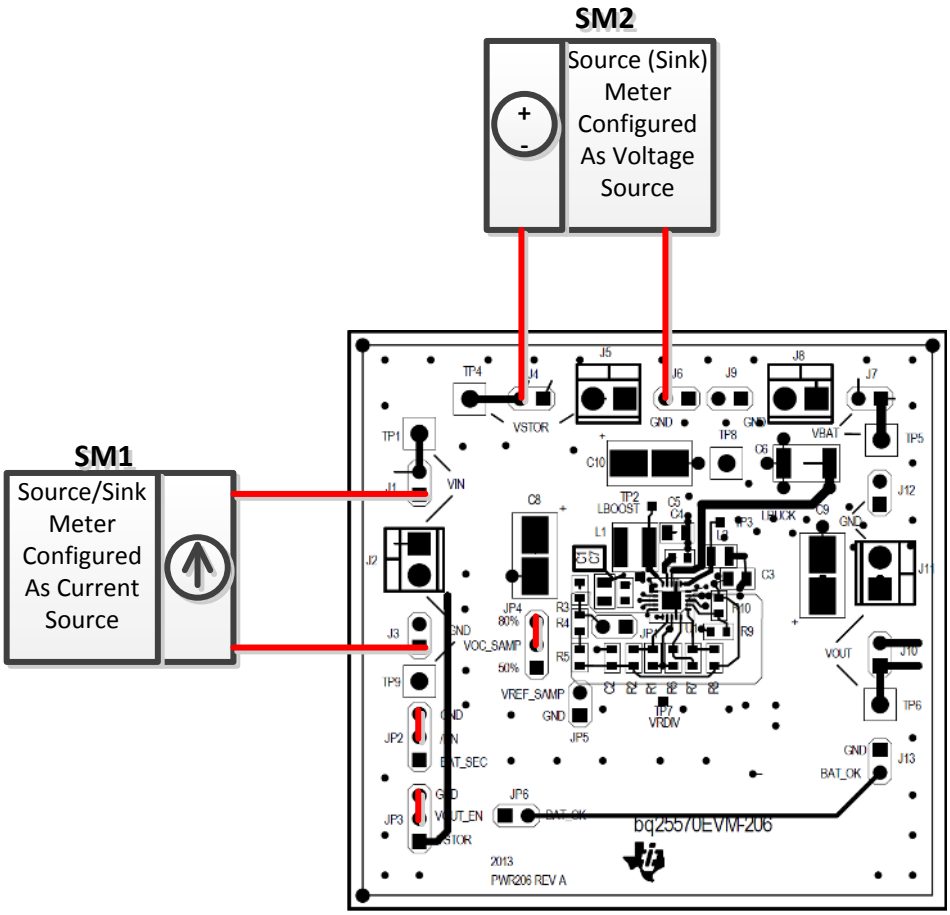


Figure 2. Test Setup for Measuring Boost Charger Efficiency

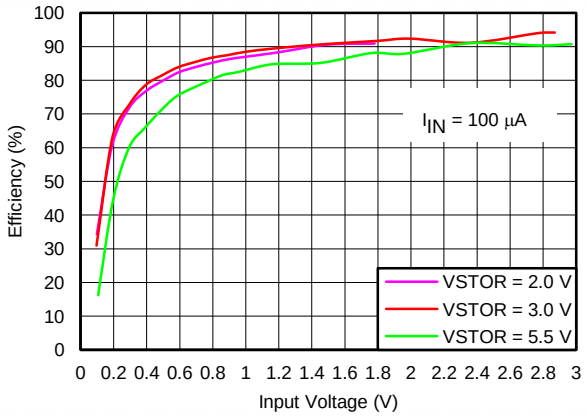


Figure 3. Charger Efficiency versus Input Voltage

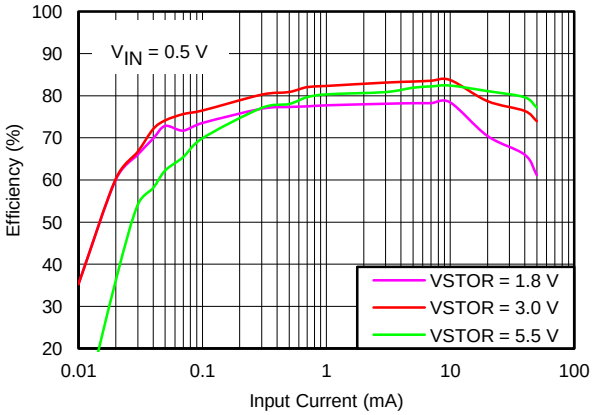


Figure 4. Charger Efficiency versus Input Current

Because the boost converter regulates input voltage instead of output voltage, uses PFM switching, operates at very low currents and has MPPT, efficiency cannot be measured using the same test setup as for an output regulating, higher power, fixed frequency PWM switching boost converter. The VSTOR output must be held at a fixed voltage (below VBAT_OV threshold) by an external source that is capable of sinking current, with that sunk current being the measured output current. In addition to filtering bursts of current due to PFM switching and the ripple voltage voltage on VIN_DC due to input voltage regulation, the series input current meter and input voltage meter must be set to filtering, or averaging, or both, which will result in longer than usual measurement times, but not longer than the 16 s MPPT sample time. Measurements for both VIN and IN will be most accurate when taken at the midpoint of the 16 s MPPT period. Remote sensing by the source-meters is possible but, on the input side, the source-meter output regulation loop and the charger MPPT input regulation loop may interfere with each other and cause the input voltage to oscillate. Adding a large capacitor across VIN_DC and GND will eliminate this oscillation but the capacitor's leakage current will inflate the input current measurement and result in lower efficiency.

See SLUA691 for a detailed explanation on how to take these and other measurements with source-meters.

3.1.2 Buck Converter Efficiency

The test setup is shown in Figure 5. The specific equipment used for the test results in Figure 6 is listed below:

1. VSTOR was connected to a low impedance power supply with a series current meter to measure current. The current meter must be able to measure currents in the nA range and may require manual range adjustments so that the range is always ≤ 10 X the expected current for best accuracy. The voltage meter measures the input voltage as close to the IC VSTOR pin as possible.
2. VOUT was connected to a resistor box with a series current meter to measure the current. (NOTE: The current meter must be able to measure currents in the nA range and may require manual range adjustments so that the range is always ≤ 10 X the expected current for best accuracy.) The voltage meter measured the VOUT voltage as close to the IC VOUT pin as possible

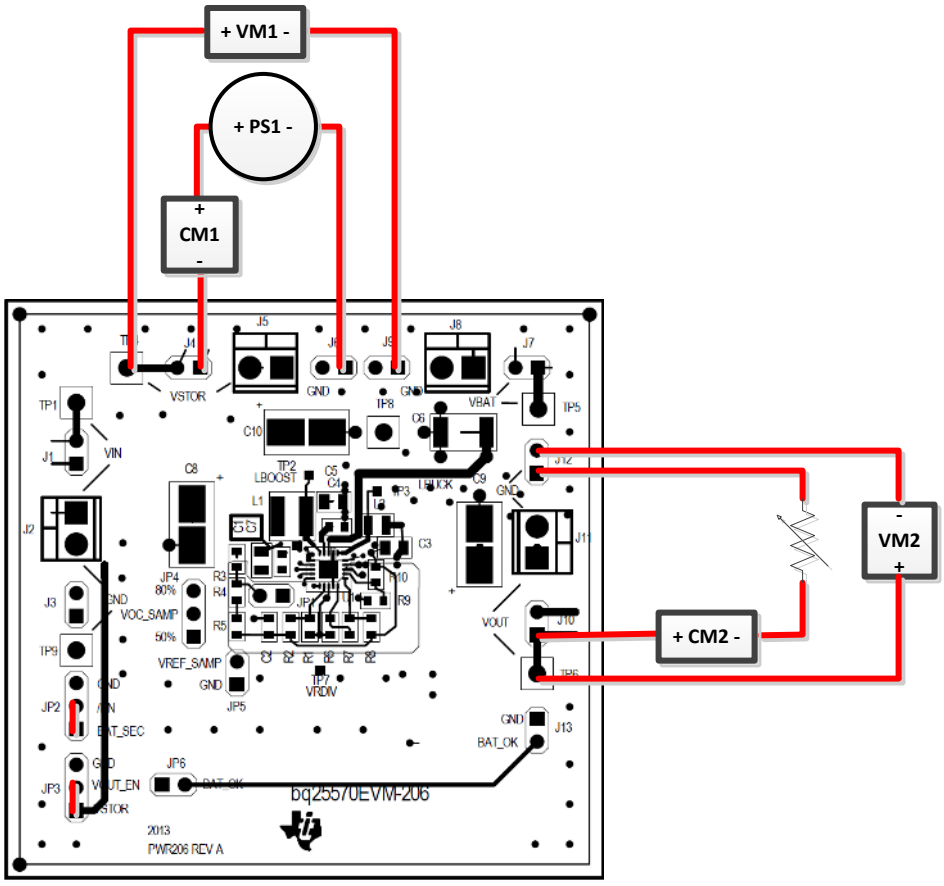


Figure 5. Test Setup for Measuring Buck Converter Efficiency

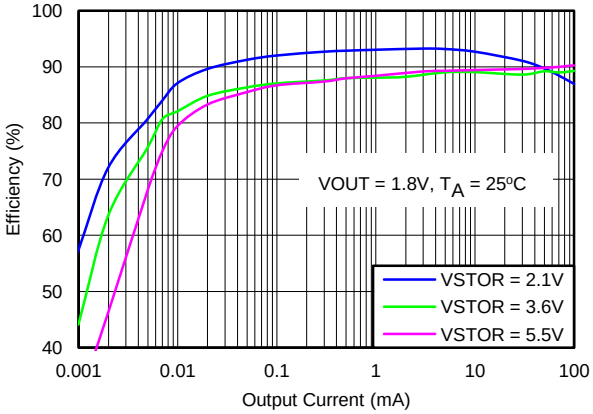


Figure 6. Buck Converter Efficiency versus Output Current

The buck converter is powered from VSTOR; therefore, to measure its efficiency alone, VIN_DC should be left floating, and the input power supply applied to VSTOR. To filter bursts of current due to PFM switching, the series input current meter from the VSTOR supply must be set to the highest level of filtering and/or averaging, which will result in longer than usual measurement times.

Alternatively, these measurements can be taken with source-meters instead of discrete power supply, resistor load box and meters. The source-meter on VSTOR is configured as a voltage source. The source-meter on OUT can be configured as either a current source that sinks current (i.e., negative current) or as a voltage source with voltage at least 100 mV below the lowest expected regulation voltage point.

3.1.3 Buck Converter Load Transient

The test setup is shown in Figure 7. The specific equipment used for the test results in Figure 8 is listed below:

1. VIN_DC was connected to a low impedance power supply by a series 100-Ω resistor. JP4 sets the MPPT voltage to 50% of VIN_OC.
2. VOUT was connected to a switch with a series resistor that switches in a 36 Ω resistor.
3. VBAT was connected a 3.2-V charged 4.2-V coin cell.
4. VSTOR, VOUT and VIN_DC was monitored by oscilloscope voltage scope probes attached to TP4, TP6, and TP1 respectively, and GND. IOUT was measured with a current probe.

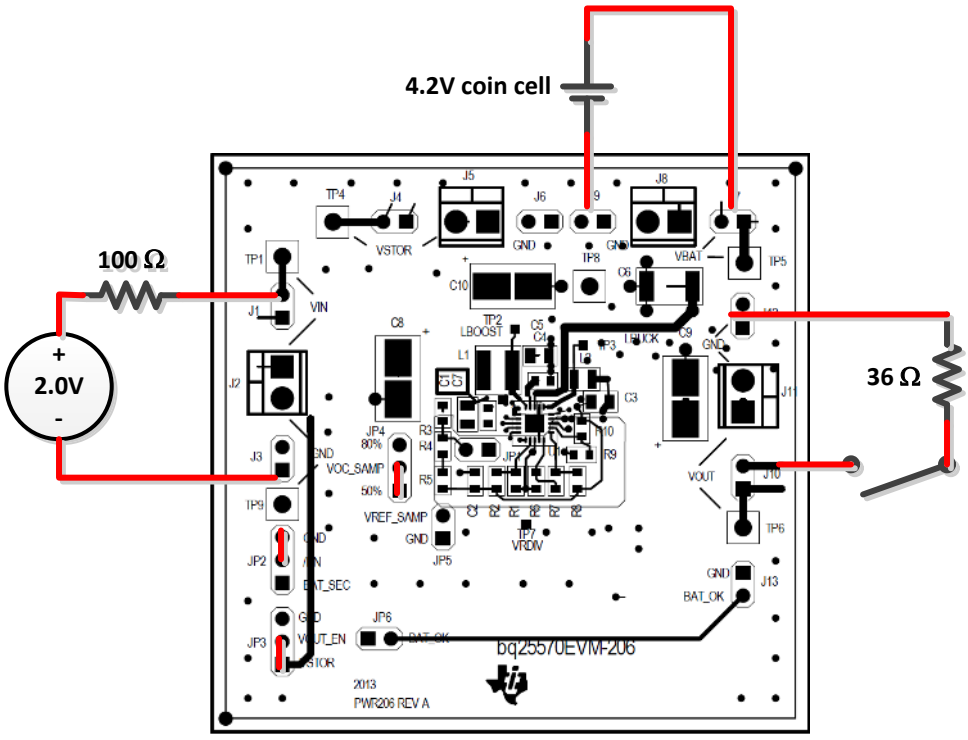


Figure 7. Test Setup for Performing Load Transient on Buck Output

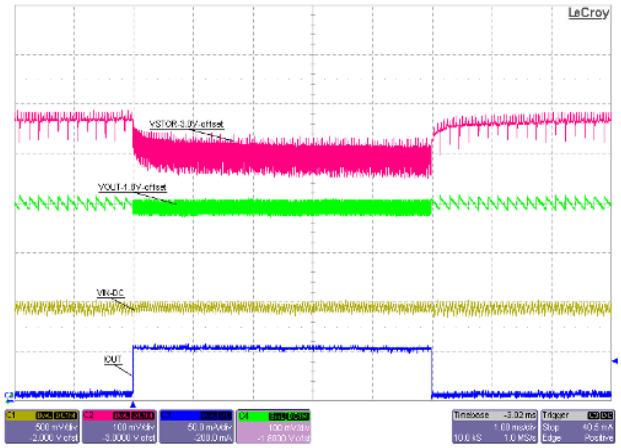


Figure 8. 50-mA Load Transient on V_{OUT}

3.1.4 Charger Operation During Load Transient

The test setup is shown in Figure 7. The specific equipment used for the test results in Figure 9 is listed below:

1. VIN_DC, VBAT and VOUT are configured as explained in Section 3.1.3.
2. The boost charger inductor current (IL) was measured by using an oscilloscope current probe across a current loop that was inserted in series with inductor L1.
3. VSTOR's ripple voltage was measured using an oscilloscope voltage probe placed directly across the VSTOR capacitor (C5). The scope probe's standard ground lead was replaced with very short lead.
4. VIN and the LBOOST pin (switching node of the boost charger) were measured by oscilloscope voltage probes connected to TP1 and TP2.

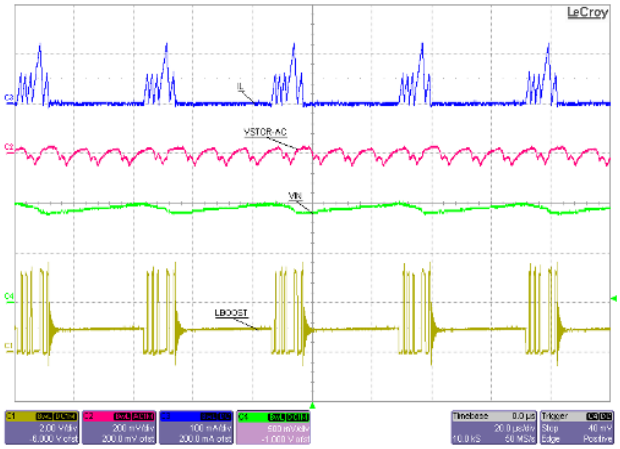


Figure 9. Charger Operational Waveforms During 50-mA Load Transient

3.1.5 Buck Converter Operation During Load Transient

The test setup is shown in Figure 7. The specific equipment used for the test results in Figure 10 is listed below:

1. VIN_DC, VBAT and VOUT are configured as explained in Section 3.1.3.
2. The buck converter inductor current (IL) was measured by using an oscilloscope current probe across a current loop that was inserted in series with inductor L2.
3. VSTOR's ripple voltage was measured using an oscilloscope voltage probe placed directly across the VSTOR capacitor (C5). VOUT's ripple voltage was measured using an oscilloscope voltage probe placed directly across the VOUT capacitor (C3). Both scope probes' standard ground leads were replaced with very short lead.
4. The LBUCK pin's ripple voltage (switching node of the buck converter) was measured by a oscilloscope voltage probe connected to TP3.

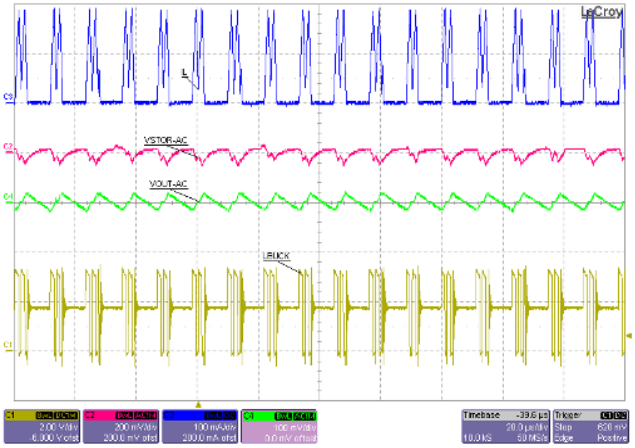


Figure 10. Buck Operational Waveforms During 50-mA Load Transient

Charging a Super Capacitor from Buck Converter Output

The test setup is shown in Figure 11. The specific equipment used for the test results in Figure 12 is listed below:

1. VIN_DC was connected to a Keithley 2420 source-meter configured as a 1.0-mA current source with 1.2-V voltage compliance.
2. VOUT was connected to a 120 mF super capacitor. There were no other loads on VSTOR, VBAT or VOUT.
3. VIN_DC, VSTOR and VOUT were measured with oscilloscope voltage probes connected at TP1, TP4 and TP6.

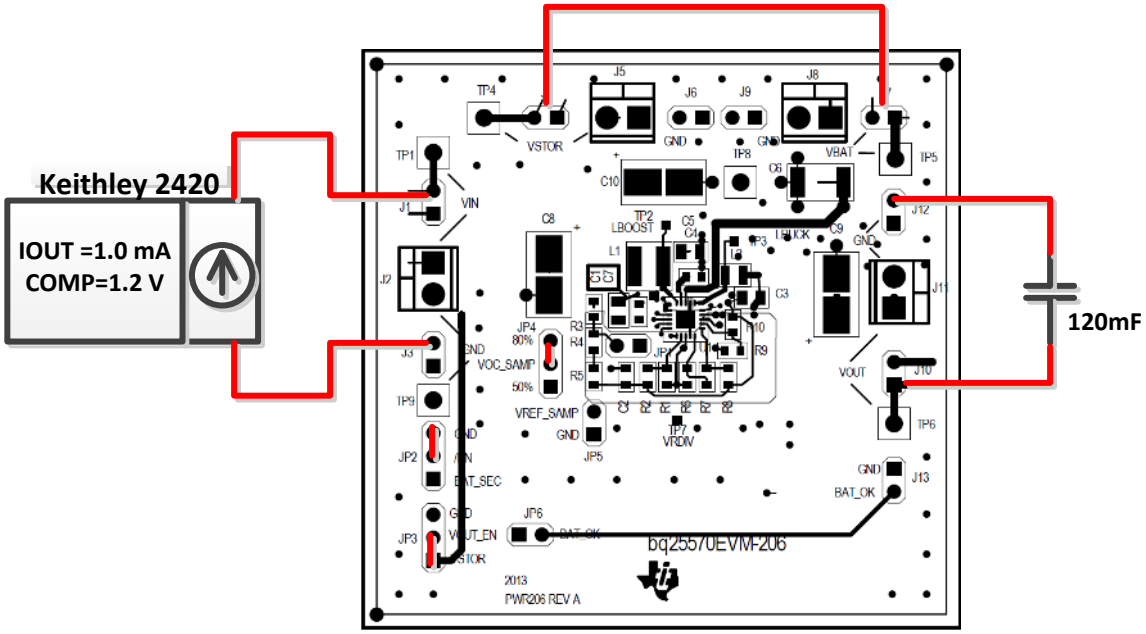


Figure 11. Test Setup for Charging a Super Capacitor from Buck Output

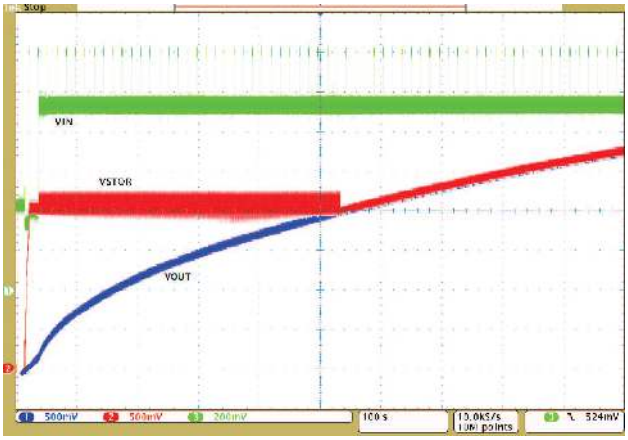


Figure 12. Charging a Super Cap from V_{OUT}

The benefit of charging of the super capacitor on VOUT instead of VBAT is faster charge time due to the charger spending less time in less efficient cold start mode.

Tips for other Tests and Measurements

The quiescent current during main boost operation, which is basically the current from the battery to the IC, is measured at the VSTOR pin. If a source-meter is not available to make the measruement, connect a 100-kΩ resistor to VSTOR and connect a 3-V supply from the other end of this resistor to the ground of the EVM. A 10-MΩ meter can be used to measure the voltage drop across the resistor and calculate the current. No other connections should be made to the EVM and the measurement should be taken after steady state conditions are reached (may take a few minutes). The reading should be much less than 100 nA.

4 Bill of Materials and Board Layout

This section contains the bill of materials (BOM) and the PCB board layouts for the bq25570 EVM.

4.1 Bill of Materials

Table 2 lists the BOM for the EVM.

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	4.7uF	Capacitor, Ceramic Chip, 6.3V, X7R, 10%	805	C0805C475K9RACTU	Kemet
1	C2**	0.01u**	Capacitor, Ceramic, 50V, X7R, 10%	0603	GRM188R71H103KA01D	Murata
1	C3	22uF	Capacitor, Ceramic Chip, 6.3V, X5R, 10%	805	JMK212BJ226MG-T	Taiyo Yuden
2	C4 C7	0.1uF	Capacitor, Ceramic Chip, 6.3V, X5R, 10%	603	06036D104KAT2A	AVX
1	C5	4.7uF	Capacitor, Ceramic Chip, 10V, X7R, 10%	805	LMK212B7475KG-T	Taiyo Yuden
1	C6	100uF	Capacitor, Ceramic Chip, 6.3V, X5R, 20%	1812	GRM43SR60J107ME20L	Murata
0	C8-10	DNP	Capacitor, Electrolytic, Snap Mt., vvV	7343 (D)	n/a	n/a
9	J1 J3-4 J6-7 J9-10 J12-13	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
4	J2 J5 J8 J11	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
3	JP1 JP5 JP6	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
3	JP2-4	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
1	L1	22uH	Inductor, SMT, 0.65A, 360mΩ Inductor SMT, 0.36A, 410mΩ	4.0mmx4.0mmx1.80mm 3.8mmx3.8mmx1.65mm	LPS4018-223M 744031220	Coilcraft
1	L2	10 uH	Inductor, SMT, 1.4A, 216mΩ Inductor SMT, 250mA, 500mΩ Inductor SMT, 500mA, 390mΩ Inductor SMT, 500mA, 500mΩ	2.0mm x 2.5 mm 2.5mm x 2.0mm x 1.00mm 2.8mm x 2.8mm x 1.35mm 2.5mm x 2.0mm x 1.2mm	1239AS-H-100N 74479888310 744029100 74479889310	Toko Wurth Elektronik Wurth Elektronik Wurth Elektronik
1	R1	7.5M	Resistor, Chip, 1/16W, 1%	603	CRCW06037M50FKEA	Vishay Dale
1	R10	8.66M	Resistor, Chip, 1/16W, 1%	603	CRCW06038M66FKEA	Vishay Dale
1	R2	5.76M	Resistor, Chip, 1/16W, 1%	603	CRCW06035M76FKEA	Vishay Dale
2	R3 R5	4.99M	Resistor, Chip, 1/16W, 1%	603	CRCW06034M99FKEA	Vishay Dale
1	R4	10M	Resistor, Chip, 1/16W, 1%	603	CRCW060310M0FKEA	Vishay Dale
1	R6	887k	Resistor, Chip, 1/16W, 1%	603	CRCW0603887KFKEA	Vishay Dale
1	R7	6.98M	Resistor, Chip, 1/16W, 1%	603	CRCW06036M98FKEA	Vishay Dale
1	R8	5.36M	Resistor, Chip, 1/16W, 1%	603	CRCW06035M36FKEA	Vishay Dale
1	R9	4.22M	Resistor, Chip, 1/16W, 1%	603	CRCW06034M22FKEA	Vishay Dale
4	TP1 TP4-6	5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
0	TP2-3 TP7	DNP	Test Point, 0.020 Hole	0.100 x 0.100 inch	STD	STD
2	TP8-9	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	BQ25570RGR	IC, Ultra Low Power Harvester Charger + Buck IC	VQFN	BQ25570RGR	TI
4			Shunt, 100-mil, Black	0.1	929950-00	3M
1	--		PCB, 2.5212 in x 2.6039 in		PWR206	Any

4.2 EVM Board Layout

Figure 13 through Figure 15 are the board layouts for this EVM.

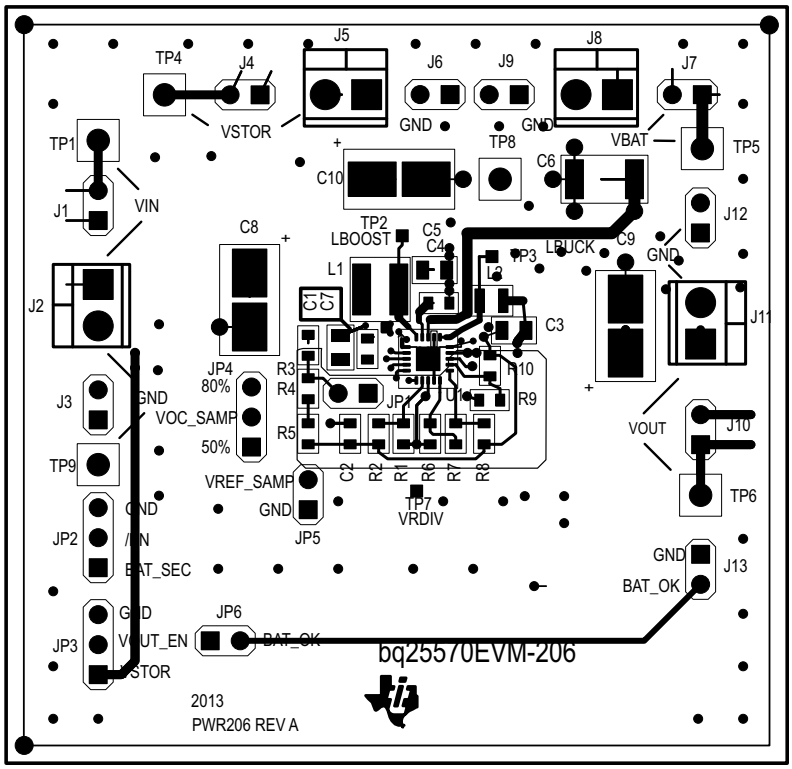


Figure 13. EVM PCB Top Assembly

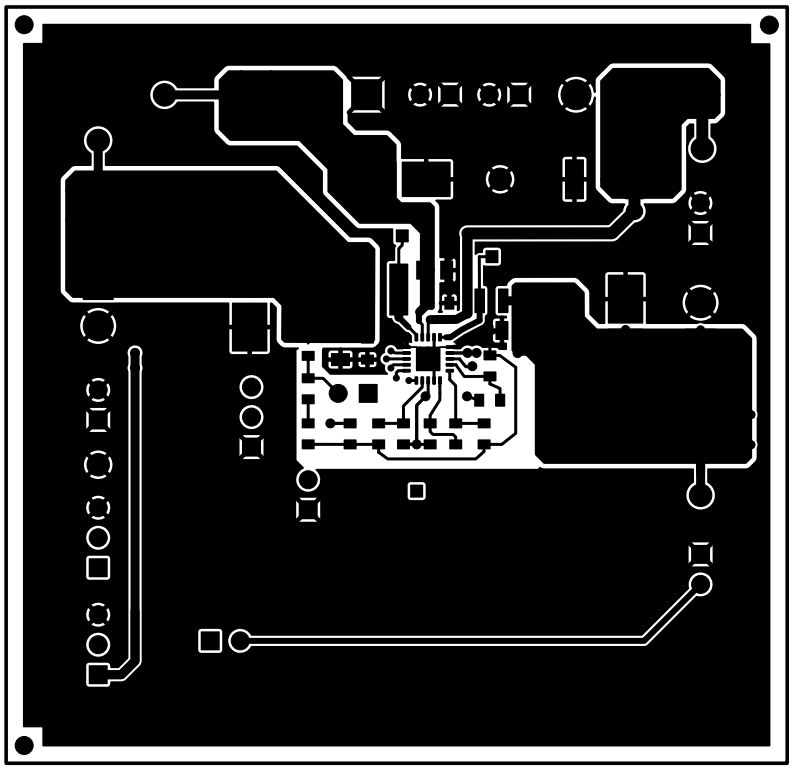


Figure 14. EVM PCB Top Layer

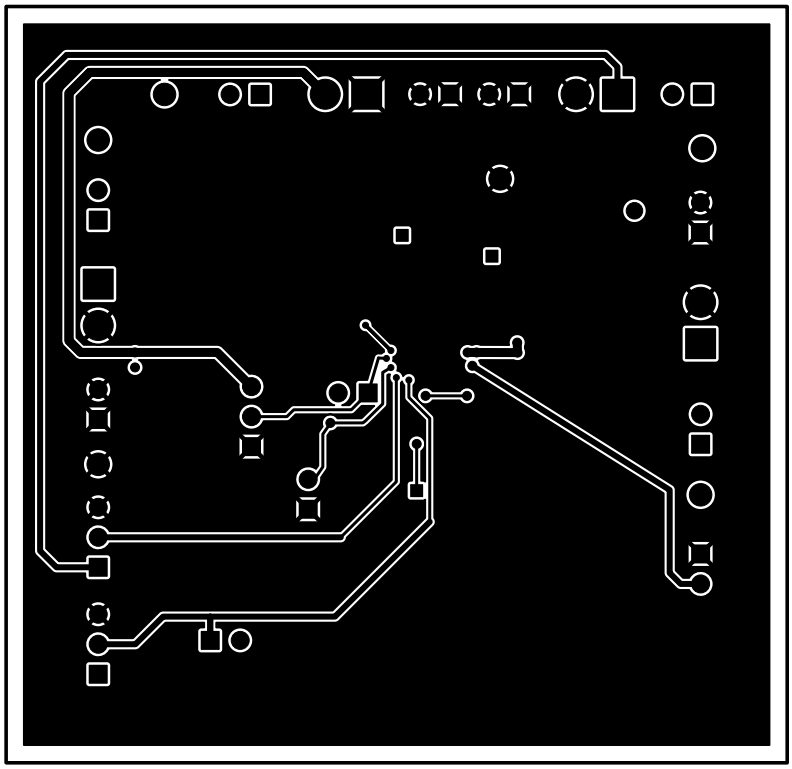


Figure 15. EVM PCB Bottom Layer

5 PCB Layout Guideline

As for all switching power supplies, the PCB layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost converter/charger and buck converter could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors as well as the inductors should be placed as close as possible to the IC. For the boost converter / charger, first priority are the output capacitors, including the 0.1uF bypass capacitor (CBYP), followed by CSTOR, which should be placed as close as possible between VSTOR, pin 19, and VSS, pin 1. Next, the input capacitor, CIN, should be placed as close as possible between VIN_DC, pin 2, and VSS, pin 1. Last in priority is the boost converter inductor, L1, which should be placed close to LBOOST, pin 20, and VIN_DC, pin 2. For the buck converter, the output capacitor COUT should be placed as close as possible between VOUT, pin 14, and VSS, pin 15. The buck converter inductor (L2) should be placed as close as possible beween the switching node LBUCK, pin 16, and VOUT, pin 14. It is best to use vias and bottom traces for connecting the inductors to their respective pins instead of the capacitors.

To minimize noise pickup by the high impedance voltage setting nodes (VBAT_OV, OK_PROG, OK_HYST, VOUT_SET), the external resistors should be placed so that the traces connecting the midpoints of each divider to their respective pins are as short as possible. When laying out the non-power ground return paths (for example from resistors and CREF), it is recommended to use short traces as well, separated from the power ground traces and connected to VSS pin 15. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. The PowerPad should not be used as a power ground return path.

The remaining pins are either NC pins, that should be connected to the PowerPad as shown below, or digital signals with minimal layout restrictions.

In order to maximize efficiency at light load, the use of voltage level setting resistors > 1MΩ is recommended. However, during board assembly, contaminants such as solder flux and even some board cleaning agents can leave residue that may form parasitic resistors across the physical resistors and/or from one end of a resistor to ground, especially in humid, fast airflow environments. This can result in the voltage regulation and threshold levels changing significantly from those expected per the installed resistor values. Therefore, it is highly recommended that no ground planes be poured near the voltage setting resistors. In addition, the boards must be carefully cleaned, possibly rotated at least once during cleaning, and then rinsed with de-ionized water until the ionic contamination of that water is well above 50 MOhm. If this is not feasible, then it is recommended that the sum of the voltage setting resistors be reduced to at least 5X below the measured ionic contamination.

Revision History

Changes from Original (July 2013) to A Revision	Page
• Changed contents in the bill of materials	17

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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Caution

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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