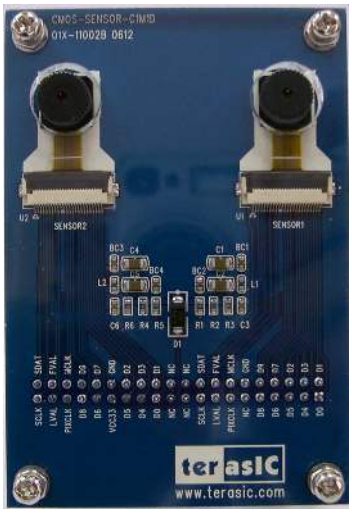
TRDB_DC2



1.3Mega Pixel Digital Camera Development Kit

Frame grabber with VGA display reference design
For Altera DE2/DE1 and Terasic T-Rex C1 Boards

TRDB_DC2

Document Version 1.2 OCT. 17, 2006 by Terasic

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Chapter 1

About the Kit

The TRDB_DC2 Kit provides everything you need to develop a 1.3Mega Pixel Digital Camera on the Altera DE2/DE1 and Terasic TREX C1 boards (**TR1**). The kit contains hardware design (in Verilog) and software to load the picture taken into a PC and save it as a BMP file. The Getting Started User Guide enables users to exercise the digital camera functions. This chapter provides users key information about the kit.

Kit Contents

Figure 1.1 shows the photo of the TRDB_DC2 package. The package includes:

1. The TRDB_DC2 (**DC2**) board with one CMOS sensor.
2. An IDE Cable.
3. A reference design CD-ROM.

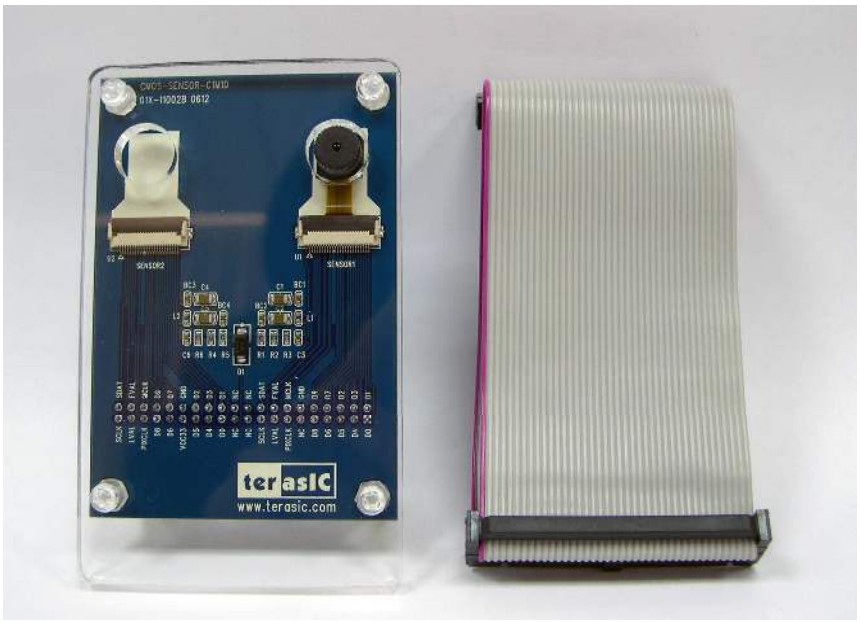


Figure 1.1. The TRDB_DC2 (**DC2**) Package Content (not including CD-ROM)

Assemble the Camera

Please follow the four steps below to assemble your camera:

1. For Altera DE2/DE1 board users, assemble the CMOS sensor lens into the 1st Sensor Connector (Sensor1-U1) on the **DC2** board, as shown in Figure 1.2.
2. For TREX-C1 users, assemble the CMOS sensor lens into the 2nd Sensor Connector (Sensor2-U2) on the **DC2** board. **NEVER use connector U1 for TREX-C1**. The CMOS Sensor will be permanently damaged if you connect the CMOS sensor to U1 for TREX-C1.
3. Connect the IDE cable to the back of the **DC2** board, as shown in Figure 1.3.
4. Connect the other end of the IDE cable to your DE2/DE1 or TREX C1 board as shown in Figure 1.4 and Figure 1.5, respectively.

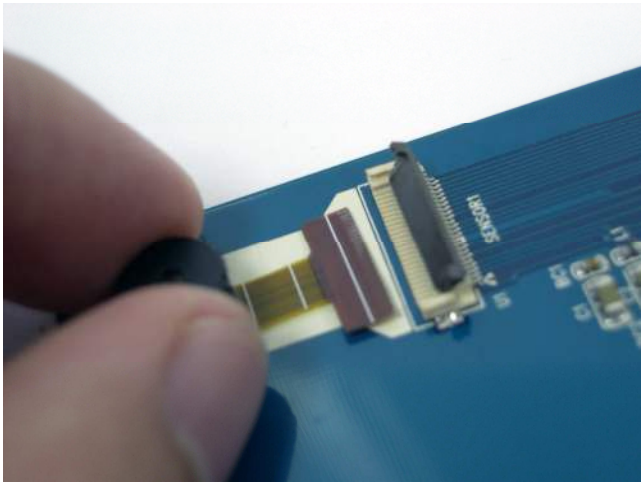


Figure 1.2 Connect the Sensor to “SENSOR1 U1” (For **DE2/DE2** Users ONLY)

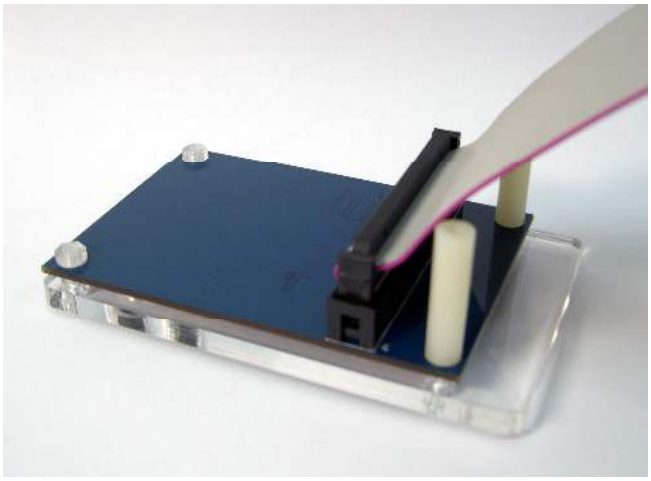


Figure 1.3 Connect the IDE cable to the back of **DC2** board

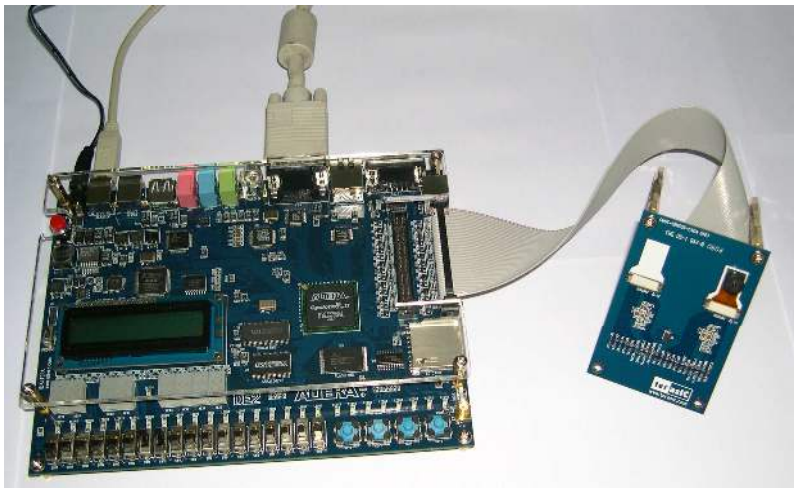


Figure 1.4 Connect the other end of IDE cable to the DE2/DE1 board's expansion port (**outermost port**).

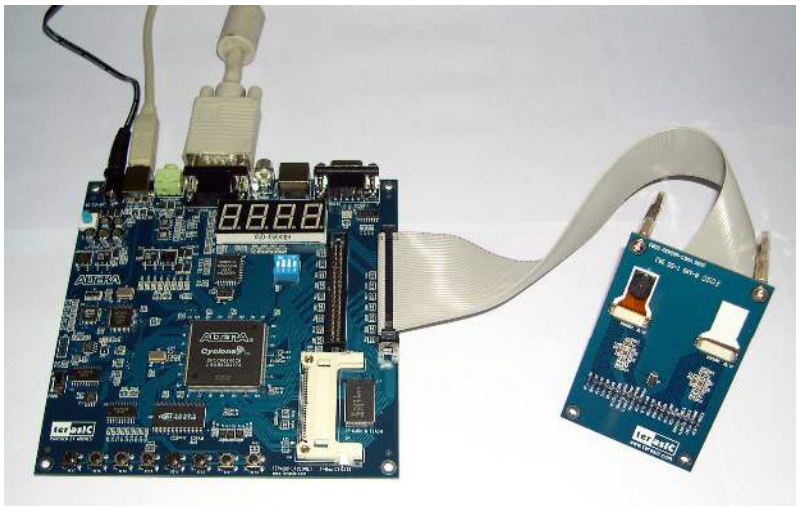


Figure 1.5 Connect the other end of the IDE cable to the TREX C1's expansion port (**outermost**).

Getting Help

Here are some places to get help if you encounter any problem:

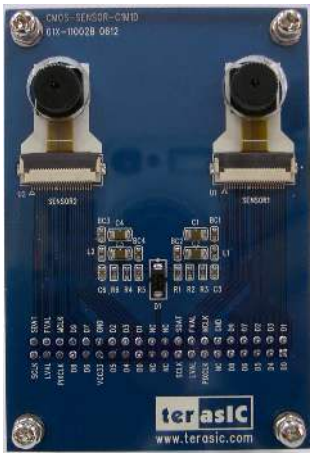
- ✓ Email to support@terasic.com
- ✓ Taiwan & China: +886-3-550-8800
- ✓ Korea : +82-2-512-7661
- ✓ Japan: +81-428-77-7000
- ✓ English Support Line: +1-408-512-1336

Chapter 2

TRDB_DC2

This chapter will illustrate the technical details users need to know to modify the reference design for their own purpose.

Features



The DC2 kit is designed using the same strict design and layout practices used in high-end consumer products. The feature set is listed below:

1. Support exposure time controlling – users can adjust the exposure according to the light of the surrounding area.
2. Support motion capture mode.
3. Software allows users to upload the picture captured into a PC and save the picture into bitmap format for viewing.
4. Equipped with iMagic C1M1D compact camera module.
5. Provide users entire reference design (Frame Grabber, high-performance multi-port SDRAM frame buffer, image processing IPs).
6. Support both Altera DE2/DE1 board and Terasic TREX-C1 Boards with the following camera locations:

Board	Sensor 1	Sensor 2
Altera DE2	Supported	Supported
Altera DE1 (aks Altera Cyclone II Starter Kit)	Supported**(1)**	Supported(1)
Terasic T-Rex C1	**Not Supported**	Supported(1)

Note (1): Unlike DE2 boards which have SXGA output, DE1 and TREX-C1 boards, with only 4-bit VGA output, should use **TRDB_LCM** (3.6”Digital LCD Panel) as output device if high-quality image displaying is desired.

Schematic of the Board

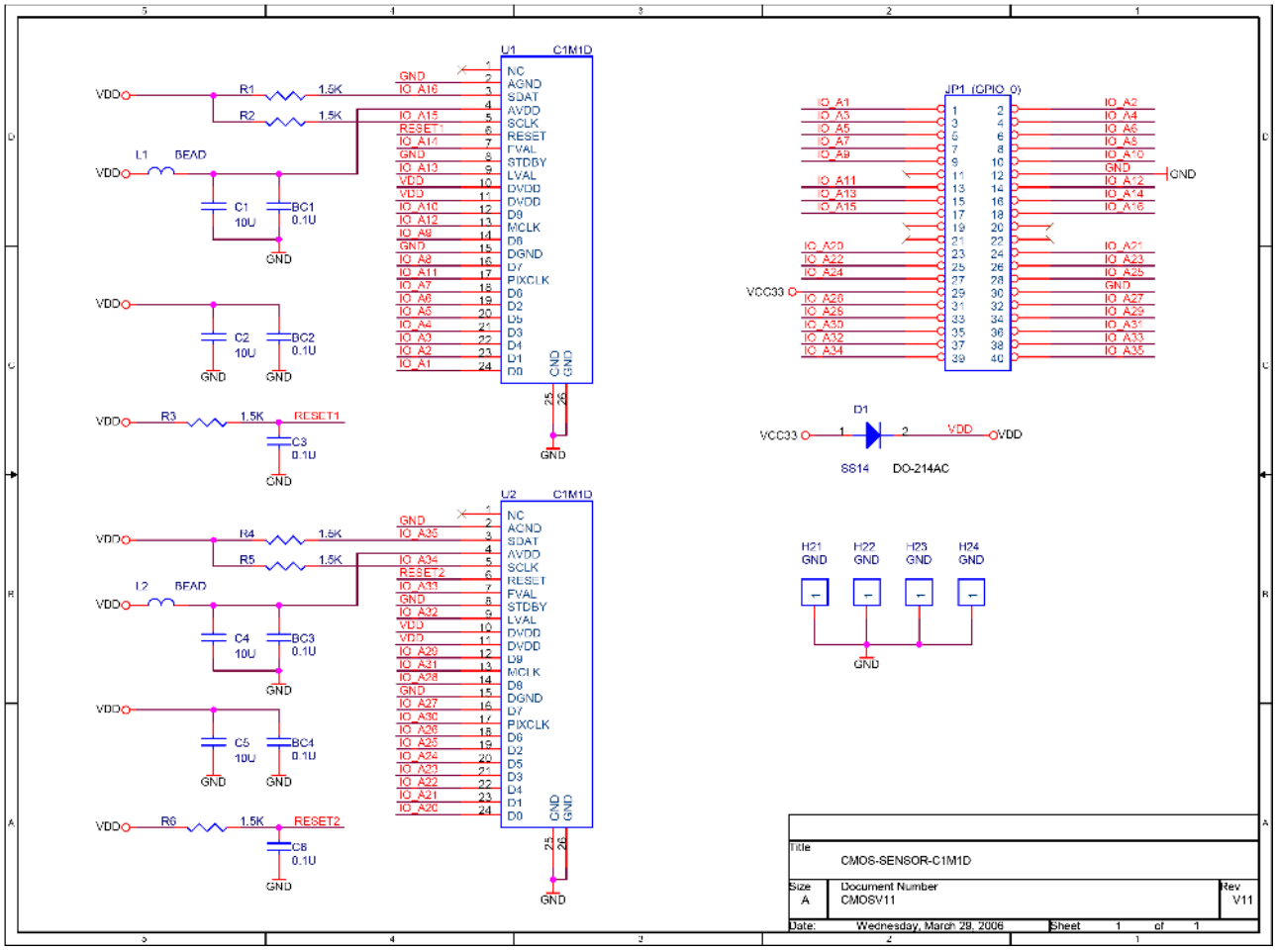


Figure 2.1. Schematic of the TRDB_DC2

Pin Description of the 40-pin Interface of TRDB_DC2

The TRDB_DC2 has a 40-pin connector on the back of the board. The pin description of the 40-pin connector follows:

Pin Numbers	Name	Direction	Description
1	DATA1[0]	Output	Sensor 1 Data Bit 0
2	DATA1[1]	Output	Sensor 1 Data Bit 1
3	DATA1[4]	Output	Sensor 1 Data Bit 4
4	DATA1[3]	Output	Sensor 1 Data Bit 3
5	DATA1[5]	Output	Sensor 1 Data Bit 5
6	DATA1[2]	Output	Sensor 1 Data Bit 2
7	DATA1[6]	Output	Sensor 1 Data Bit 6
8	DATA1[7]	Output	Sensor 1 Data Bit 7
9	DATA1[8]	Output	Sensor 1 Data Bit 8
10	DATA1[9]	Output	Sensor 1 Data Bit 9
11	NC	N/A	Not Connect
12	GND	N/A	Ground
13	PIXCLK1	Output	Sensor 1 Pixel Clock
14	MCLK1	Input	Sensor 1 Master Clock
15	LVAL1	Output	Sensor 1 Line Valid
16	FVAL1	Output	Sensor 1 Frame Valid
17	SCLK1	input	Sensor 1 I^2C Clock
18	SDATA1	I/O	Sensor 1 I^2C Data
19	N/C	N/A	Not Connect
20	N/C	N/A	Not Connect
21	N/C	N/A	Not Connect
22	N/C	N/A	Not Connect
23	DATA2[0]	Output	Sensor 2 Data Bit 0
24	DATA2[1]	Output	Sensor 2 Data Bit 1
25	DATA2[4]	Output	Sensor 2 Data Bit 4
26	DATA2[3]	Output	Sensor 2 Data Bit 3
27	DATA2[5]	Output	Sensor 2 Data Bit 5
28	DATA2[2]	Output	Sensor 2 Data Bit 2
29	VCC33	N/A	Power 3.3V
30	GND	N/A	Ground
31	DATA2[6]	Output	Sensor 2 Data Bit 6
32	DATA2[7]	Output	Sensor 2 Data Bit 7
33	DATA2[8]	Output	Sensor 2 Data Bit 8
34	DATA2[9]	Output	Sensor 2 Data Bit 9
35	PIXCLK2	Output	Sensor 2 Pixel Clock
36	MCLK2	Input	Sensor 2 Master Clock
37	LVAL2	Output	Sensor 2 Line Valid
38	FVAL2	Output	Sensor 2 Frame Valid
39	SCLK2	input	Sensor 2 I^2C Clock
40	SDATA2	I/O	Sensor 2 I^2C Data

Chapter 3

Digital Camera Design Demonstration

This chapter illustrates how to exercise the digital camera reference design provided with the kit. Users can follow the instructions in this chapter to build a 1.3Mega Pixel camera using their DE2/DE1/TREX-C1 in 5 mins.

Demonstration Setup

The Demonstration configuration is illustrated in Figure 3.1. The image raw data is sent from TRDB_DC2 to the DE2/DE1/TR1(TREX-C1) boards. The FPGA on the DE2/DE1/TR1 board is handling image processing part and converts the data to RGB format to display on the VGA monitor. The image captured at SDRAM can be taken at anytime (snapshot) and uploaded to a PC as a bitmap file.

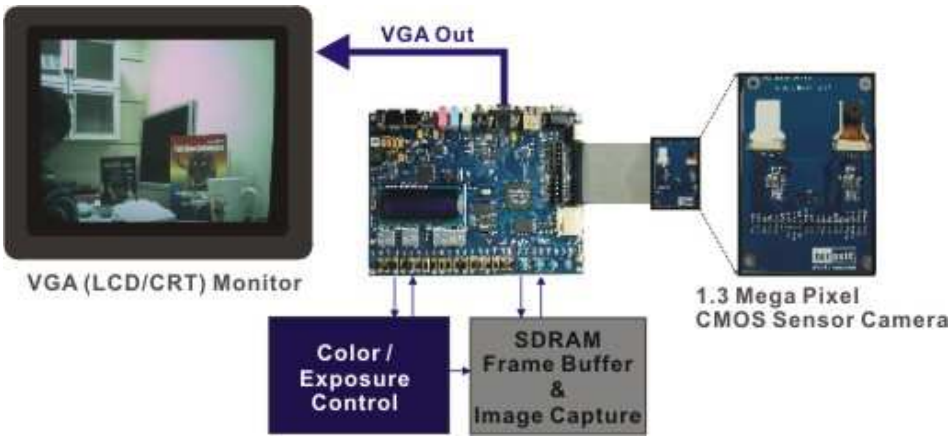


Figure 3.1. The Digital Camera Demo configuration setup

Configuring the Camera (DE2 Board Users)

Locate the project directory from the CD-ROM included and follow the steps below:

Quartus II Project Directory: DE2_CCD

FPGA Bitstream Used: DE2_CCD.sof or DE2_CCD.pof

1. Ensure the connection is made correctly as shown in Figure 3.2. Make sure the IDE cable is connected to **JP2** of the DE2 board.
2. Download the bitstream (**DE2_CCD.sof/pof**) to the DE2 board.
3. Connect the VGA output of the DE2 board to a VGA monitor.
4. Set toggle switches **SW10 and SW9 to ON**(UP position); set the other switches to OFF(DOWN position)
5. Press **KEY0** on the DE2 board to reset the circuit.
6. You can press **KEY3** to switch to the FREE RUN mode and you should be able to see whatever the camera sees on the VGA display.
7. Press **KEY2** to take a shot of the photo; you can press **KEY3** again to switch back to **FREE RUN** mode.
8. **If you find the image shown on the display is too dark, you can increase the exposure time by changing the SW[15:0] to a larger binary number – you should start from changing SW8 to ONE. Remember to press KEY1 to reload the new exposure value defined by SW[15:0]**
9. **If the room is very dark, you might need to set SW11 to ONE (very long exposure time).**
10. The following table summarize the functional keys of the digital camera.

Component	Function Description
KEY[0]	Reset circuit
KEY[1]	Set the new exposure time (load the binary value defined by SW[15:0])
KEY[2]	Trigger the Image Capture (take a shot)
KEY[3]	Switch to Free Run mode
SW[15:0]	16-bit exposure time; For normal indoor lighting, set SW11 and SW10 to ONE(UP).
LEDG[8:0]	Line counter (Display ONLY)
HEX[7:0]	Frame counter (Display ONLY)

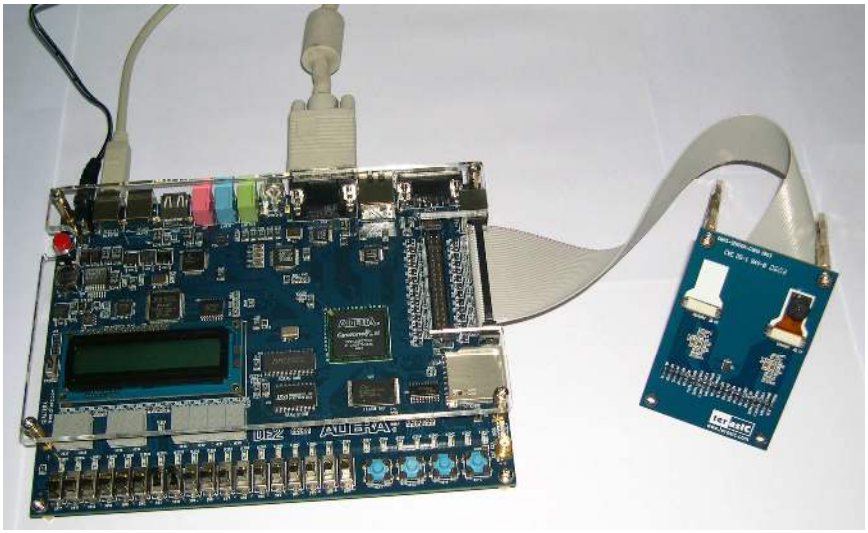


Figure 3.2. The Connection Setup for DE2 users

Configuring the Camera
(DE1 Board / Altera Cyclone II Starter Kit Users)

Locate the project directory from the CD-ROM included and follow the steps below:

A: If VGA Monitor is used for displaying image.

Quartus II Project Directory: DE1_CCD

FPGA Bitstream Used: DE1_CCD.sof or DE1_CCD.pof

B: If TRDB_LCM (3.6" Digital LCD Panel) is used for displaying image.

Quartus II Project Directory: DE1_LCM_CCD

FPGA Bitstream Used: DE1_LCM_CCD.sof or DE1_LCM_CCD.pof

1. Ensure the connection is made correctly as shown in Figure 3.3. Make sure the IDE cable is connected to **JP2** of the DE1 board.
2. Download the bitstream (**DE2_CCD.sof/DE2_LCM_CCD.sof**) to the DE1 board.
3. Connect the **VGA** output of the DE1 board to a VGA monitor.

   Or

   Connect the **TRDB_LCM** (3.6" Digital LCD Panel) to the DE1 board.
4. Set toggle switches **SW4 and SW3 to ON**(UP position); set the other switches to OFF(DOWN position)
5. Press **KEY0** on the DE2 board to reset the circuit.
6. You can press **KEY3** to switch to the FREE RUN mode and you should be able to see whatever the camera sees on the VGA display.
7. Press **KEY2** to take a shot of the photo; you can press **KEY3** again to switch back to **FREE RUN** mode.
8. **If you find the image shown on the display is too dark, you can increase the exposure time by changing the SW[9:0] to a larger binary number – you should start from changing SW5 to ONE. Remember to press KEY1 to reload the new exposure value defined by SW[9:0]**
9. **If the room is very dark, you might need to set SW8 to ONE (very long exposure time).**
10. The following table summarize the functional keys of the digital camera.

Component	Function Description
KEY[0]	Reset circuit
KEY[1]	Set the new exposure time (load the binary value defined by SW[9:0])
KEY[2]	Trigger the Image Capture (take a shot)
KEY[3]	Switch to Free Run mode
SW[9:0]	10-bit exposure time; For normal indoor lighting, set SW4 and SW3 to ONE(UP).
LEDG[8:0]	Line counter (Display ONLY)
HEX[3:0]	Frame counter (Display ONLY)

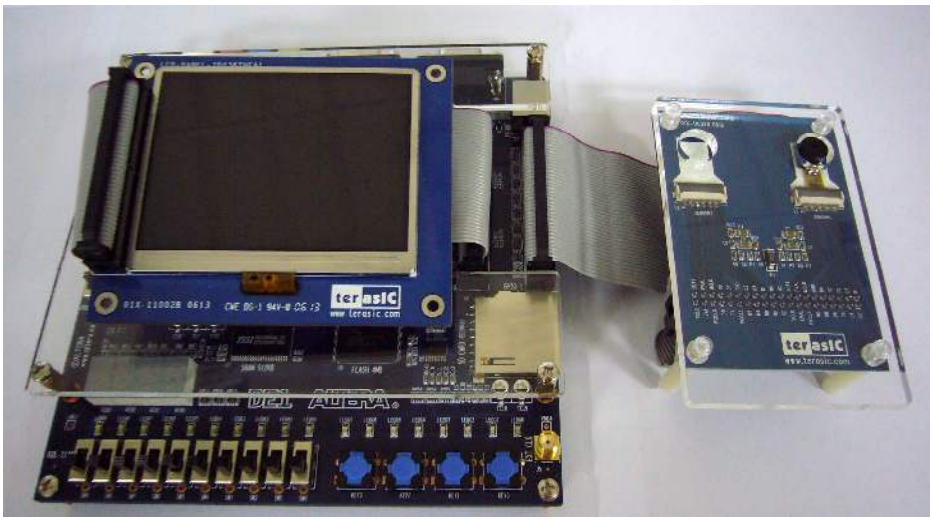


Figure 3.3. The Connection Setup for DE1 users (DC2 module is connected to JP2)

Configuring the Camera (TREX C1 Board Users)

Locate the project directory from the CD-ROM included and follow the steps below:

Quartus II Project Directory: TR1_CCD

FPGA Bitstream Used: TR1_CCD.sof or TR1_CCD.pof

1. Ensure the connection is made correctly as shown in Figure 3.2. Make sure the IDE cable is connected to **JP2** of the TR1 board and the CMOS sensor module is connected to the U2 connector.
2. Download the bitstream (**TR1_CCD.sof/pof**) to the TR1 board.
3. Connect the VGA output of the TR1 board to a VGA monitor.
4. Set toggle switches **SW2 and SW1 to ON**(UP position); set the other switches to OFF(DOWN position)
5. Press KEY0 on the DE2 board to reset the circuit.
6. You can press KEY3 to switch to the FREE RUN mode and you should be able to see whatever the camera sees on the VGA display.
7. Press KEY2 to take a shot of the photo; you can press KEY3 again to switch back to FREE RUN mode.
8. **If you find the image shown on the display is too dark, you can increase the exposure time by changing the SW[3:0] to a larger binary number – Remember to press KEY1 to reload the new value defined by SW[3:0]**
9. The following table summarize the functional keys of the digital camera.

Component	Function Description
KEY[0]	Reset circuit
KEY[1]	Set new exposure time
KEY[2]	Trigger the image capture (take a shot)
KEY[3]	Switch to the Free Run mode
SW[3:0]	4-bit exposure time
LED[7:0]	Line counter (Display ONLY)
HEX[7:0]	Frame counter (Display ONLY)

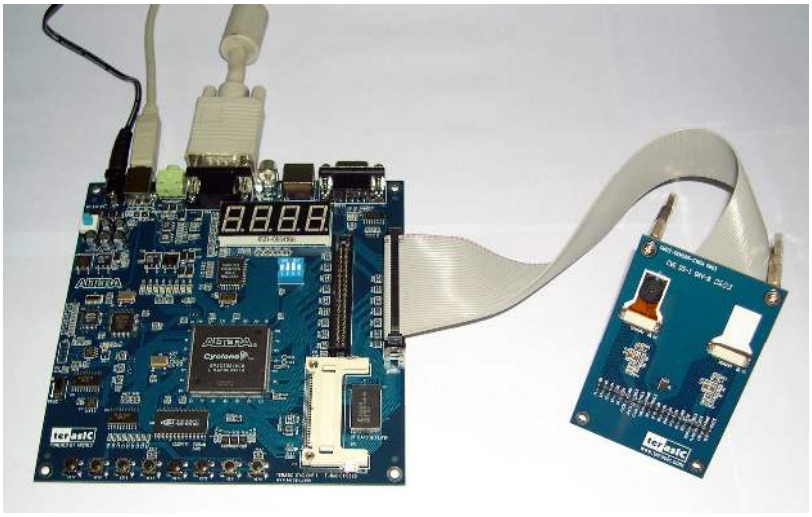
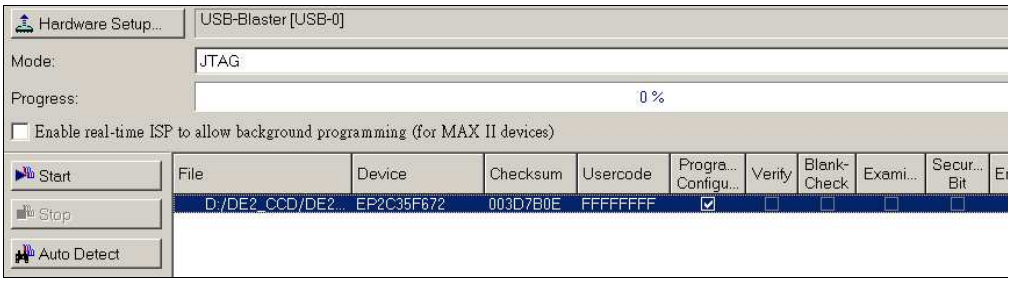


Figure 3.4. The Connection Setup for TR1 users

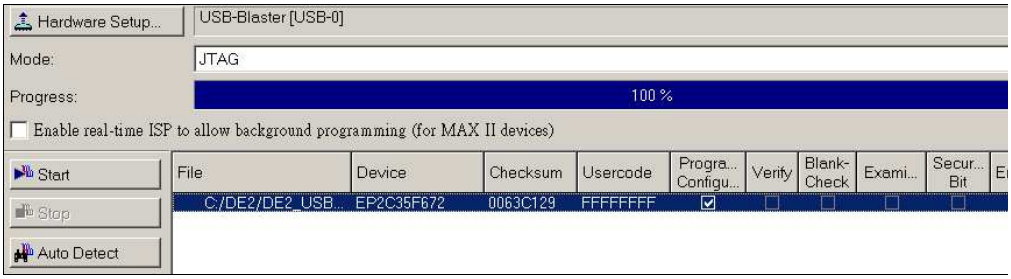
Load the Image Captured to your PC

The TRDB_DC2 package also provides users a software tool for uploading the image taken to your PC and save the data as a bitmap file. Follow the steps below to exercise this feature: Please also refer to Chapter 3 **DE2/DE1 Control Panel** in the **Altera DE2/DE1 User Manual** for more details in the **Control Panel Software**.

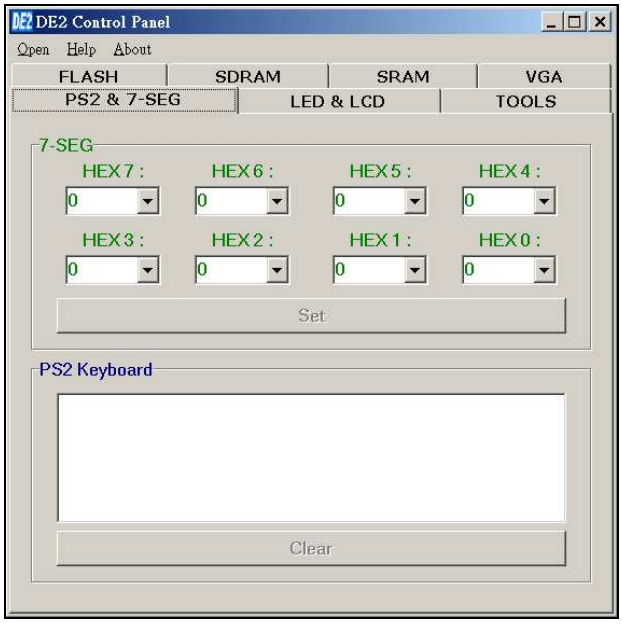
1. Load the CMOS reference design bit stream (**DE2_CCD/DE1_CCD**) into FPGA.



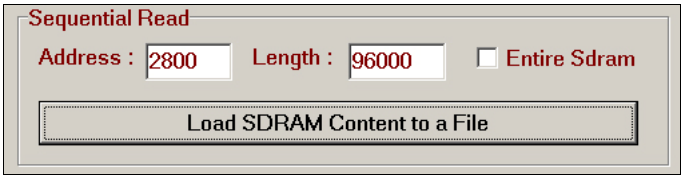
2. Press KEY3 to switch to the Free Run mode.
3. Press KEY2 to capture an image into the SDRAM.
4. Load the Control Panel bit stream (**DE2_USB_API/ DE1_USB_API**) into the FPGA. Please also refer to **Chapter 3 DE2/DE1 Control Panel** in the **Altera DE2/DE1 User Manual** for more details in the **Control Panel Software**.



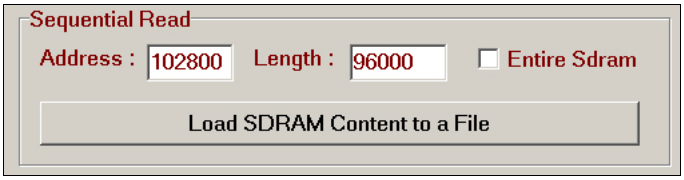
5. Execute the Control Panel application software.



6. Switch to SDRAM page; load the SDRAM content to a file starting from address **2800H** and length is **96000H**. Please save the result to a file ***filename*_GB.DAT**. You can change the *filename* to another name.



7. Load SDRAM content to another file starting from address **102800H** and length is **96000H**. Please save it to ***filename*_GR.DAT.**



8. Execute Terasic image converter v1.1 application software (located in the CD-ROM).
9. Choosing the **"To Bitmap"** tab.
10. Select the format field to **"CCM to Bitmap**".
11. Click on the **"Open GB Data "** button and select the *filename*_GB.DAT file.
12. Click on the **"Open GR Data "** button and select the *filename*_GR.DAT file.

13. You can see the image captured shown in your windows.

14. Click on the **"Save Bitmap"** button to save this bitmap file in your computer.

Block Diagram of the Reference Design

The complete reference design is also located in the CD-ROM attached. Please refer to the following diagram to help you in reading the code provided.

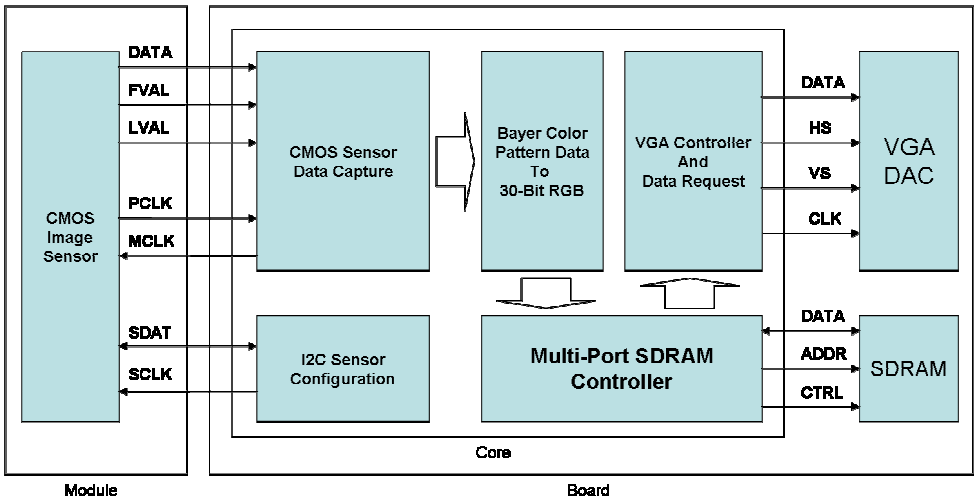


Figure 3.4. The block diagram of the digital camera design

Chapter 4

Appendix

Revision History

Date	Change Log
JAN 20, 2006	Initial Version (Preliminary)
JAN 25, 2006	Release ready for production lot
MAR 29, 2006	For iMagic C1M1D sensor.
OCT. 17, 2006	Added Labs for Altera DE1 Board (Cyclone II Starter Kit)

Always Visit TRDB_DC2 Webpage for New Applications

We will be continuing providing interesting examples and labs on our TRDB_DC2 webpage. Please visit www.altera.com or **dc2.terasic.com** for more information.