

BUK766R0-60E

N-channel TrenchMOS standard level FET

28 July 2016

Product data sheet

1. General description

Standard level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with VGS(th) rating of greater than 1V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	60	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>	[1]	-	-	75	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	182	W
Static characte	eristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ Fig. 11		_	4.58	6	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 48 V; V _{GS} = 10 V; Fig. 13; Fig. 14		-	20	-	nC

^[1] Continuous current is limited by package.



Pinning information

Table 2. **Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D I
2	D	drain		
3	S	source		G TITA
mb	D	mounting base; connected to drain	1 3	mbb076 S
			D2PAK (SOT404)	

Ordering information

Table 3. **Ordering information**

Type number	Package				
	Name	Description	Version		
BUK766R0-60E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404		

Marking

Table 4. **Marking codes**

Type number	Marking code
BUK766R0-60E	BUK766R0-60E

Limiting values

Table 5. **Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	60	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 k Ω		-	60	V
V_{GS}	gate-source voltage	T _j ≤ 175 °C; DC		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	182	W
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; <u>Fig. 2</u>	[1]	-	75	Α
		T _{mb} = 100 °C; V _{GS} = 10 V; <u>Fig. 2</u>	[1]	-	75	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 3		-	473	Α
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
Source-dra	nin diode	'				
Is	source current	T _{mb} = 25 °C	[1]	-	75	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	473	Α
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; V_{sup} ≤ 60 V; R_{GS} = 50 Ω; V_{GS} = 60 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[2][3]	-	196	mJ

- Continuous current is limited by package. Single-pulse avalanche rating limited by maximum junction temperature of 175 $^{\circ}\text{C}.$
- Refer to application note AN10273 for further information.

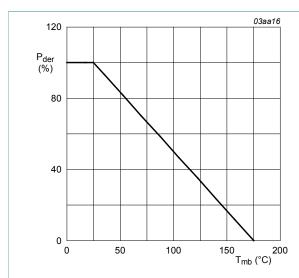
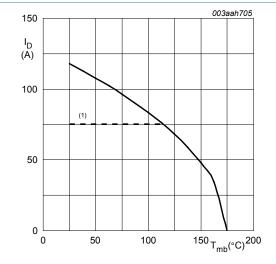


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



(1) Capped at 75A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 10V$$

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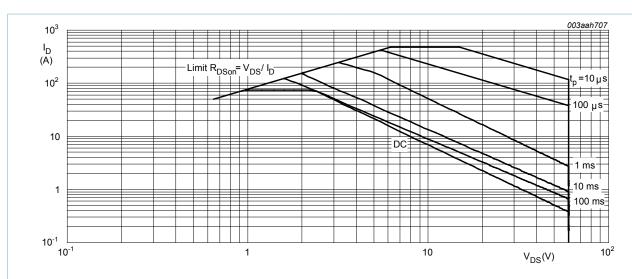
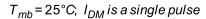


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



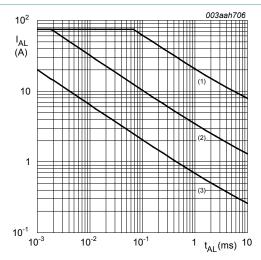


Fig. 4. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)
$$T_{j(init)} = 25$$
°C; (2) $T_{j(init)} = 150$ °C; (3) Repetitive Avalanche

9. Thermal characteristics

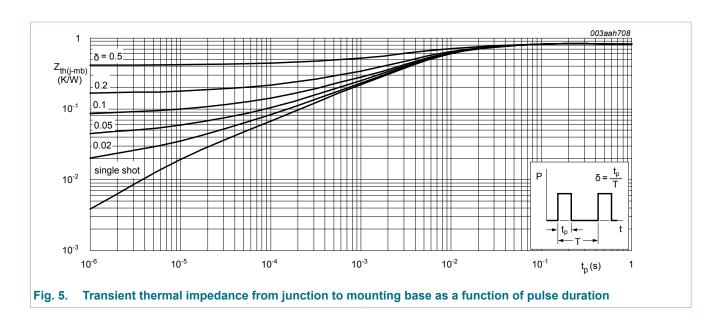
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	0.82	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		'			
V _{(BR)DSS} drain-source breakdown voltage		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	60	-	-	V
	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	54	-	-	V	
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ Fig. 9; Fig. 10	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9	-	-	4.5	V
I _{DSS} drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	1	μΑ	
	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μΑ	
I _{GSS} gate leakage of	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_{D} = 25 A; T_{j} = 25 °C; Fig. 11	-	4.58	6	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 11; Fig. 12	-	-	13	mΩ
Dynamic ch	naracteristics		'			
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 48 V; V _{GS} = 10 V;	-	62	-	nC
Q_{GS}	gate-source charge	Fig. 13; Fig. 14	-	16	-	nC
Q_{GD}	gate-drain charge	1	-	20	-	nC

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_{j} = 25 \text{ °C}; Fig. 15$	-	3390	4520	pF
C _{oss}	output capacitance		-	447	536	pF
C _{rss}	reverse transfer capacitance		-	272	372	pF
t _{d(on)}	turn-on delay time	V_{DS} = 45 V; R_{L} = 1.8 Ω ; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω	-	19	-	ns
t _r	rise time		-	36	-	ns
$t_{d(off)}$	turn-off delay time		-	38	-	ns
t _f	fall time		-	34	-	ns
L _D	internal drain inductance	from upper edge of mounting base to centre of die	-	2.5	-	nΗ
L _S	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
Source-dra	in diode			1		
V _{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$	-	0.84	1.2	V
t _{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/ μ s; V_{GS} = 0 V; V_{DS} = 25 V	-	35	-	ns
Q _r	recovered charge		-	43	-	nC

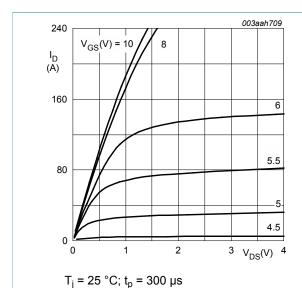


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

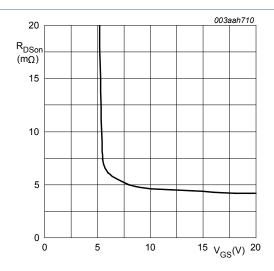


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25$$
°C; $I_D = 25A$

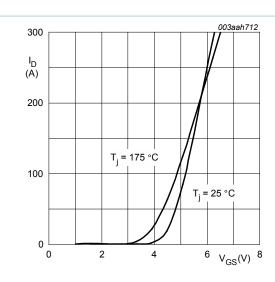


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



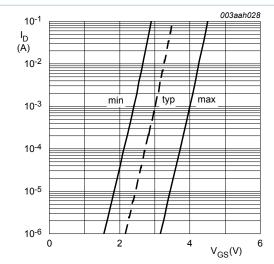


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^{\circ}C; \ V_{DS} = 5V$$

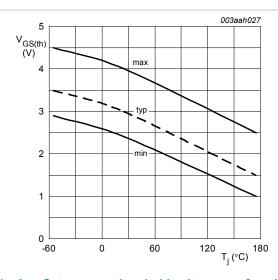
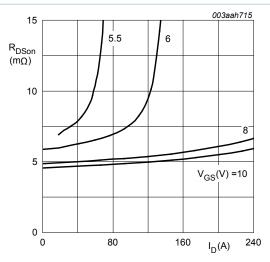


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D$$
 = 1 mA; V_{DS} = V_{GS}



 $T_i = 25 \,^{\circ}\text{C}; t_p = 300 \,\mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

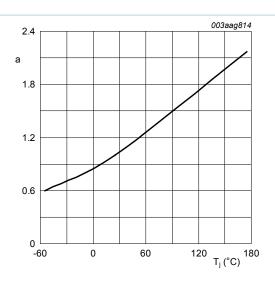


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25 \, ^{\circ}\text{C})}}$$

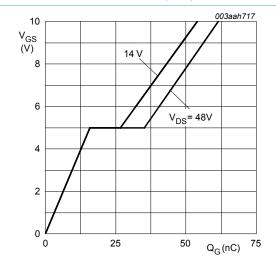


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_i = 25^{\circ}C; I_D = 25A$$

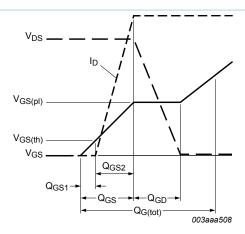


Fig. 13. Gate charge waveform definitions

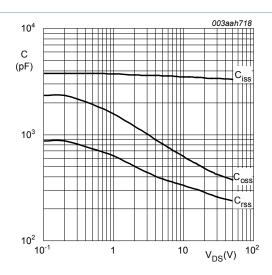


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V$$
; $f = 1MHz$

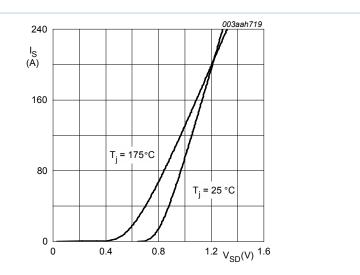


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values $V_{\rm GS} = 0V$

11. Package outline

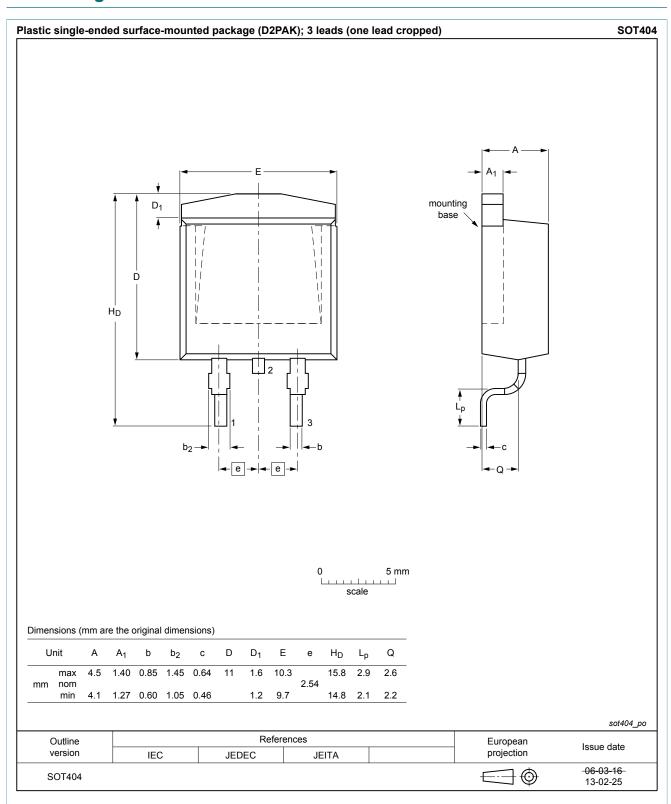


Fig. 17. Package outline D2PAK (SOT404)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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