



Preliminary 8Mb (256Kx36 & 512x18) and 4Mb (128Kx36 & 256Kx18) SRAM

Features

- 256K x 36 or 512K x 18 Organizations
- 128K x 36 or 256K x 18 Organizations
- 0.25 Micron CMOS Technology
- Synchronous Flow Thru Mode of Operation with Self-Timed Late Write
- Differential HSTL Input Clocks (K, \bar{K})
- Differential HSTL Output Clocks (C, \bar{C})
- +3.3V Power Supply, Ground, 1.6V V_{DDQ} , and 0.95V V_{REF}
- HSTL Input and Output levels
- Registered Addresses, Write Enables, Synchronous Select, and Data Ins.
- Common I/O
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability & Global Write Enable
- 7 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary Scan Order
- Programmable Impedance Output Drivers

Description

The 4Mb and 8Mb SRAMs are Synchronous Flowthru Mode, high-performance CMOS Static Random Access Memories that are versatile and wide I/O, and can achieve 3ns cycle times. Differential K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the K clock, all Addresses, Write-Enables, Sync Select, and Data Ins are registered

internally. Differential clocks C and \bar{C} are used to control the Output Data hold time by allowing output data to change after the rising edge of the C clock. An internal Write buffer allows write data to follow one cycle after addresses and controls. The chip is operated with a single +3.3V power supply and is compatible with HSTL I/O interface.

x36 BGA Pinout (Top View)

	1	2	3	4	5	6	7
A	V _{DDQ}	SA	SA	NC	SA	SA	V _{DDQ}
B	NC	NC	SA	NC	SA	NC,SA(8Mb)	NC
C	NC	SA	SA	V _{DD}	SA	SA	NC
D	DQ19	DQ18	V _{SS}	ZQ	V _{SS}	DQ9	DQ10
E	DQ22	DQ20	V _{SS}	\overline{SS}	V _{SS}	DQ11	DQb13
F	V _{DDQ}	DQ21	V _{SS}	\overline{G}	V _{SS}	DQ12	V _{DDQ}
G	DQ24	DQ23	\overline{SBWc}	\overline{C}	\overline{SBWb}	DQ14	DQb15
H	DQ25	DQ26	V _{SS}	C	V _{SS}	DQ17	DQb16
J	V _{DDQ}	V _{DD}	V _{REF}	V _{DD}	V _{REF}	V _{DD}	V _{DDQ}
K	DQ34	DQ35	V _{SS}	K	V _{SS}	DQ8	DQ7
L	DQ33	DQ32	\overline{SBWd}	\overline{K}	\overline{SBWa}	DQ5	DQ6
M	V _{DDQ}	DQ30	V _{SS}	\overline{SW}	V _{SS}	DQ3	V _{DDQ}
N	DQ31	DQ29	V _{SS}	SA	V _{SS}	DQ2	DQ4
P	DQ28	DQ27	V _{SS}	SA	V _{SS}	DQ0	DQ1
R	NC	SA	M1*	V _{DD}	M2*	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{DD}.

x18 BGA Pinout (Top View)

	1	2	3	4	5	6	7
A	V _{DDQ}	SA	SA	NC	SA	SA	V _{DDQ}
B	NC	NC	SA	NC	SA	NC,SA(8Mb)	NC
C	NC	SA	SA	V _{DD}	SA	SA	NC
D	DQ14	NC	V _{SS}	ZQ	V _{SS}	DQ0	NC
E	NC	DQ15	V _{SS}	\overline{SS}	V _{SS}	NC	DQ1
F	V _{DDQ}	NC	V _{SS}	\overline{G}	V _{SS}	DQ2	V _{DDQ}
G	NC	DQ16	\overline{SBWb}	\overline{C}	NC	NC	DQ3
H	DQ17	NC	V _{SS}	C	V _{SS}	DQ4	NC
J	V _{DDQ}	V _{DD}	V _{REF}	V _{DD}	V _{REF}	V _{DD}	V _{DDQ}
K	NC	DQ13	V _{SS}	K	V _{SS}	NC	DQ8
L	DQ12	NC	NC	\overline{K}	\overline{SBWa}	DQ7	NC
M	V _{DDQ}	DQ10	V _{SS}	\overline{SW}	V _{SS}	NC	V _{DDQ}
N	DQ11	NC	V _{SS}	SA	V _{SS}	DQ6	NC
P	NC	DQ9	V _{SS}	SA	V _{SS}	NC	DQ5
R	NC	SA	M1	V _{DD}	M2	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{DD}.



Pin Description

SA0-SA18	Address Input SA0-SA18 for 512Kx18 SA0-SA17 for 256Kx36 SA0-SA17 for 256Kx18 SA0-SA16 for 128Kx36	\bar{G}	Asynchronous Output Enable
DQ0-DQ35	Data I/O DQ0-DQ17 for 512Kx18 DQ0-DQ35 for 256Kx36	\bar{SS}	Synchronous Select
K, \bar{K}	Differential Input Register Clocks	M1, M2	Clock Mode Inputs.
C, \bar{C}	Differential Output Data Hold Control Clocks	$V_{REF(2)}$	HSTL Input Reference Voltage
\bar{SW}	Write Enable, Global	V_{DD}	Power Supply (+3.3V)
\bar{SBW}_a	Write Enable, Byte a (DQ0-DQ8)	V_{SS}	Ground
\bar{SBW}_b	Write Enable, Byte b (DQ9-DQ17)	V_{DDQ}	Output Power Supply
\bar{SBW}_c	Write Enable, Byte c (DQ18-DQ26)	ZZ	Asynchronous Sleep Mode
\bar{SBW}_d	Write Enable, Byte d (DQ27-DQ35)	ZQ	Output Driver Impedance Control
TMS,TDI,TCK	IEEE 1149.1 Test Inputs (LVTTTL levels)	NC	No Connect
TDO	IEEE 1149.1 Test Output (LVTTTL level)		

Ordering Information (These are all possible sorts; some may not be qualified.)

Part Number	Organization	Speed	Leads
IBM0418A40QLAB - 3T	256K x 18	4.2ns Access / 3.3ns Cycle	7 x 17 BGA
IBM0418A40QLAB - 3S		4.5ns Access / 3.6ns Cycle	
IBM0418A40QLAB - 3E		5.0ns Access / 3.8ns Cycle	
IBM0418A40QLAB - 4T		5.5ns Access / 4.2ns Cycle	
IBM0436A40QLAB - 3T	128K x 36	4.2ns Access / 3.3ns Cycle	
IBM0436A40QLAB - 3S		4.5ns Access / 3.6ns Cycle	
IBM0436A40QLAB - 3E		5.0ns Access / 3.8ns Cycle	
IBM0436A40QLAB - 4T		5.5ns Access / 4.2ns Cycle	
IBM0418A80QLAB - 3T	512K x 18	4.2ns Access / 3.3ns Cycle	
IBM0418A80QLAB - 3S		4.5ns Access / 3.6ns Cycle	
IBM0418A80QLAB - 3E		5.0ns Access / 3.8ns Cycle	
IBM0418A80QLAB - 4T		5.5ns Access / 4.2ns Cycle	
IBM0436A80QLAB -3T	256K x 36	4.2ns Access / 3.3ns Cycle	
IBM0436A80QLAB -3S		4.5ns Access / 3.6ns Cycle	
IBM0436A80QLAB -3E		5.0ns Access / 3.8ns Cycle	
IBM0436A80QLAB -4T		5.5ns Access / 4.2ns Cycle	



Revision Log

Revision	Contents of Modification
11/98	Initial release.
7/99	Corrected BGA Dimension on page 28

For a complete datasheet, please contact your IBM sale representative.



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