LM2902-Q1, LM2902B-Q1, and LM2902BA-Q1 Industry-Standard Quad Operational Amplifiers for Automotive Applications

1 Features

- AEC Q-100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C
  - Device HBM ESD classification 2
  - Device CDM ESD classification C5
- Wide supply range of:
  - 3 V to 36 V (LM2902B-Q1 and LM2902BA-Q1)
  - 3 V to 32 V (LM2902KV and LM2902KAV)
  - 3 V to 26 V (all other products)
- Input offset voltage maximum at 25°C of:
  - 2 mV (LM2902BA-Q1 and LM2902KAV)
  - 3 mV (LM2902B-Q1)
  - 7 mV (all other products)
- Internal RF and EMI filter (LM2902B-Q1 and LM2902BA-Q1)
- Supply-current of 175 µA per channel, typical
- Unity-gain bandwidth of 1.2 MHz
- Common-mode input voltage range includes V–
- Differential input voltage range equal to maximum-rated supply voltage

2 Applications

- Automotive lighting
- Body electronics
- Automotive head unit
- Telematics control unit
- Emergency call (eCall)
- Passive safety: brake system
- Electric vehicle / hybrid electric:
  - Inverter and motor control
  - On-board (OBC) and wireless charger
  - Battery management system (BMS)

3 Description

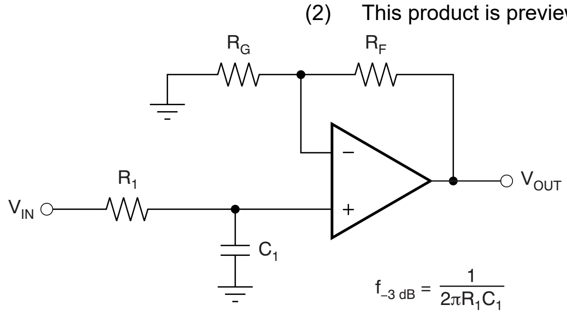
This device consists of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is possible when the difference between the two supplies is 3 V to 36 V (for B-version devices), 3 V to 32 V (for V-version devices) or 3 V to 26 V (for all other devices), and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational-amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM2902 can be operated directly from the standard 5-V supply that is used in digital systems and easily provides the required interface electronics without requiring additional ±15-V supplies.

Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
LM2902B-Q1	SOIC (2)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
LM2902BA-Q1	SOIC (14)(2)	8.65 mm × 3.91 mm
	TSSOP (14)(2)	5.00 mm × 4.40 mm
LM2902-Q1	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) This product is preview only.



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Single-Pole, Low-Pass Filter

Table of Contents

1 Features 1
2 Applications 1
3 Description 1
4 Revision History 2
5 Pin Configurations and Functions 3
6 Specifications 4
6.1 Absolute Maximum Ratings 4
6.2 ESD Ratings 4
6.3 Recommended Operating Conditions 4
6.4 Thermal Information 5
6.5 Electrical Characteristics - LM2902B-Q1 and LM2902BA-Q1 6
6.6 Electrical Characteristics: LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1 8
6.7 Operating Conditions: LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1 9
6.8 Typical Characteristics 10
7 Parameter Measurement Information 16
8 Detailed Description 17
8.1 Overview 17
8.2 Functional Block Diagram 17
8.3 Feature Description 17
8.4 Device Functional Modes 18
9 Application and Implementation 19
9.1 Application Information 19
9.2 Typical Application 19
9.3 Design Requirements 19
9.4 Detailed Design Procedure 19
9.5 Application Curve 20
10 Power Supply Recommendations 21
11 Layout 22
11.1 Layout Guidelines 22
11.2 Layout Example 22
12 Device and Documentation Support 23
12.1 Documentation Support 23
12.2 Receiving Notification of Documentation Updates 23
12.3 Support Resources 23
12.4 Trademarks 23
12.5 Electrostatic Discharge Caution 23
12.6 Glossary 23
13 Mechanical, Packaging, and Orderable Information 24

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (May 2022) to Revision G (February 2023) — **Page**

- Deleted the Preview note for the LM2902B-Q1 TSSOP-14 package in the *Device Information* table 1
- Changed the LM2902B-Q1 values in the *Thermal Information* section 5
- Added *Typical Characteristics* curves for LM2902B-Q1 and LM2902BA-Q1 10

Changes from Revision E (April 2008) to Revision F (May 2022) — **Page**

- Changed the name of the data sheet 1
- Revised *Features* section to include LM2902B-Q1 and LM2902BA-Q1 1
- Added *Applications* section 1
- Added LM2902B-Q1 and LM2902BA-Q1 to the *Device Information* table 1
- Added LM2902B-Q1 and LM2902BA-Q1 to the *Description* section 1
- Updated *Pin Configurations and Functions* section to include *Pin Functions* table 3
- Added LM2902B-Q1 and LM2902BA-Q1 to the *Absolute Maximum Ratings* table 4
- Added *ESD Ratings* table with LM2902B-Q1 and LM2902BA-Q1 4
- Added LM2902B-Q1 and LM2902B-Q1 to *Recommended Operating Conditions* section 4
- Added LM2902B-Q1 and LM2902BA-Q1 to *Thermal Information* section 5
- Added *Overview* section to the data sheet 17
- Added *Feature Description* section 17
- Added *Input Common Mode Range* section to *Feature Description* section 17
- Added *Device Functional Modes* information for LM2902B-Q1 and LM2902BA-Q1 18
- Added *Application and Implementation* section for LM2902B-Q1 and LM2902BA-Q1 19
- Added *Application Information* section for LM2902B-Q1 and LM2902BA-Q1 19
- Added *Typical Application* section for LM2902B-Q1 and LM2902BA-Q1 19
- Added *Power Supply Recommendations* section to data sheet 21
- Added *Layout* section to data sheet 22
- Added *Device and Documentation Support* section to data sheet 23
- Added *Mechanical, Packaging, and Orderable Information* section to data sheet 24

5 Pin Configurations and Functions

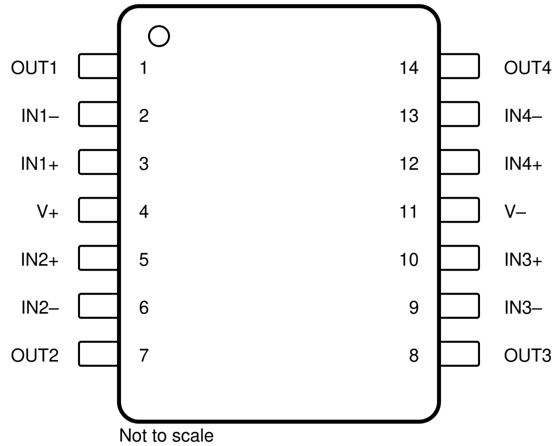


Figure 5-1. D and PW Package 14-Pin SOIC and TSSOP (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
NC	—	—	No internal connection
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

For T_A = 25°C (unless otherwise noted)[1]

	LM2902B-Q1, LM2902BA-Q1	LM2902-Q1	LM2902KV-Q1	UNIT
Supply voltage, V_{CC} [2]	40	26	32	V
Differential input voltage, V_{ID} [3]	±40	±26	±32	V
Input voltage, V_I	–0.3 to 40	–0.3 to 26	–0.3 to 32	V
Duration of output short circuit (one amplifier) to ground at (or below) T_A = 25°C, V_{CC} ≤ 15 V[4]	Unlimited	Unlimited	Unlimited	
Operating virtual junction temperature, T_J	150	142	142	°C
Storage temperature range, T_{stg}	–65 to 150	–65 to 150	–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) Differential voltages are at IN+ with respect to IN−.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
LM2902B-Q1 and LM2902BA-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	
LM2902KV-Q1 and LM2902KAV-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±2000	
LM2902-Q1				
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	±1500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = ([V+] – [V–])	LM2902B-Q1, LM2902BA-Q1	3	36	V
		LM2902KV-Q1, LM2902KAV-Q1	3	30	
		LM2902-Q1	3	26	
V_{CM}	Common-mode voltage		V–	(V+) – 2	V
T_A	Operating ambient temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1		LM2902B-Q1, LM2902BA-Q1		UNIT
		D (SOIC)	PW (TSSOP)	D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101	86	TBD	133.3	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	—	—	TBD	63.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	—	TBD	76.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	—	—	TBD	15.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	—	—	TBD	75.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics - LM2902B-Q1 and LM2902BA-Q1

For V_S = (V+) – (V–) = 5 V to 36 V (±2.5 V to ±18 V), at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10k connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	LM2902B-Q1				±0.3	±3.0	mV
				T_A = –40°C to 125°C			±4.0	
		LM2902BA-Q1				±0.3	±2	
				T_A = –40°C to 125°C			2.5	
dV_{OS}/dT	Input offset voltage drift	R_S = 0 Ω		T_A = –40°C to 125°C		±7		µV/°C
PSRR	Input offset voltage versus power supply				65	100		dB
	Channel separation	f = 1 kHz to 20 kHz				120		dB
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	V_S = 3 V to 36 V			V–		(V+) – 1.5	V
		V_S = 5 V to 36 V		T_A = –40°C to 125°C	V–		(V+) – 2	
CMRR	Common-mode rejection ratio	(V–) ≤ V_{CM} ≤ (V+) – 1.5 V	V_S = 3 V to 36 V		70	80		dB
		(V–) ≤ V_{CM} ≤ (V+) – 2 V	V_S = 5 V to 36 V	T_A = –40°C to 125°C	65	80		
INPUT BIAS CURRENT								
I_B	Input bias current					-10	-35	nA
				T_A = –40°C to 125°C			-50	
dI_{OS}/dT	Input offset current drift			T_A = –40°C to 125°C		10		pA/°C
I_{OS}	Input offset current					±0.5	±4	nA
				T_A = –40°C to 125°C			±5	
dI_{OS}/dT	Input offset current drift			T_A = –40°C to 125°C		10		pA/°C
NOISE								
E_N	Input voltage noise	f = 0.1 to 10 Hz				3		μV_{PP}
e_N	Input voltage noise density	R_S = 100 Ω, V_I = 0 V, f = 1 kHz (see Figure 8)				35		nV/√Hz
INPUT IMPEDANCE								
Z_{ID}	Differential					10 || 0.1		MΩ || pF
Z_{ICM}	Common-mode					4 || 1.5		GΩ || pF
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	V_S = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ, connected to (V-)			50	100		V/mV
				T_A = –40°C to 125°C	25			
FREQUENCY RESPONSE								
GBW	Gain-bandwidth product	R_L = 1 MΩ, C_L = 20 pF (see Figure 7)				1.2		MHz
SR	Slew rate	R_L = 1 MΩ, C_L = 30 pF, V_I = ±10 V (see Figure 7)				0.5		V/µs
Θ_m	Phase margin	G = + 1, R_L = 10kΩ, C_L = 20 pF				56		°
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V Step , G = +1, C_L = 100 pF				4		µs
	Overload recovery time	V_{IN} × gain > V_S				10		µs
THD+N	Total harmonic distortion + noise	G = + 1, f = 1 kHz, V_O = 3.53 V_{RMS}, V_S = 36V, R_L = 100k, I_{OUT} ≤ 50µA, BW = 80 kHz				0.001%		
OUTPUT								
V_O	Voltage output swing from rail	Positive Rail (V+)		I_{OUT} = -50 µA		1.35	1.5	V
V_O				I_{OUT} = -1 mA		1.4	1.6	V
V_O				I_{OUT} = -5 mA		1.5	1.75	V
V_O		Negative Rail (V-)		I_{OUT} = 50 µA		100	150	mV
V_O				I_{OUT} = 1 mA		0.75	1	V
V_O			V_S = 5 V, RL ≤ 10 kΩ connected to (V–)	T_A = –40°C to 125°C		5	20	mV
I_O	Output current	V_S = 15 V; V_O = V-; V_{ID} = 1 V	Source		-20	-30		mA
				T_A = –40°C to 125°C	-10			mA
		V_S = 15 V; V_O = V+; V_{ID} = -1 V	Sink		10	20		mA
				T_A = –40°C to 125°C	5			mA
		V_{ID} = -1 V; V_O = (V-) + 200 mV			50	85		µA
I_{SC}	Short-circuit current	V_S = 20 V, (V+) = 10 V, (V-) = -10 V, V_O = 0 V				±40	±60	mA
C_{LOAD}	Capacitive load drive					100		pF

6.5 Electrical Characteristics - LM2902B-Q1 and LM2902BA-Q1 (continued)

For V_S = (V+) – (V–) = 5 V to 36 V (±2.5 V to ±18 V), at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10k connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			300		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 5 V; I_O = 0 A	T_A = –40°C to 125°C		175	300	µA
		V_S = 36 V; I_O = 0 A	T_A = –40°C to 125°C		350	750	µA

6.6 Electrical Characteristics: LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1

For $V_S = (V_+) – (V_–) = 5$ V, at $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TA[1]	MIN	TYP[2]	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 26 V, V_{IC} = V_{ICR}min, V_O = 1.4 V		25°C		3	7	mV
				Full Range			10	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		2	50	nA
				Full Range			300	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–20	–250	nA
				Full Range			–500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to 26 V		25°C	V-		(V+) - 1.5	V
				Full Range	V-		(V+) - 2	
V_{OH}	High-level output voltage	R_L = 10 kΩ		25°C	(V+) – 1.5			V
		V_{CC} = 26 V,	R_L = 2 kΩ	Full Range	22			
		V_{CC} = 26 V	R_L ≥ 10 kΩ	Full Range	23	24		
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ		Full Range		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC}= 15 V, V_O= 1 V to 11 V, R_L ≥ 2 kΩ		25°C		100		V/mV
				Full Range	15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C	50	80		dB
k_{SVR}	Supply-voltage rejection ratio (ΔV_{CC} /ΔV_{IO})			25°C	50	100		dB
V_{O1}/ V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120		dB
I_O	Output current	V_{CC} = 15 V, V_O = 0	V_{ID} = 1 V,	25°C	–20	–30	–60	mA
				Full Range	–10			
		V_{CC} = 15 V, V_O = 15 V	V_{ID} = −1 V,	25°C	10	20		
				Full Range	5			
		V_{ID} = −1 V	V_O = 200 mV	25°C		30		µA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V	V_O = 0	25°C		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V	No load	Full Range		0.7	1.2	mA
		V_{CC} = 26 V, V_O = 0.5 V_{CC}	No load	Full Range		1.4	3	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 32 V, V_{IC} = V_{ICR}min V_O = 1.4 V	Non-A devices	25°C		3	7	mV
				Full Range			10	
			A-suffix devices	25°C		1	2	
				Full Range			4	
$\Delta V_{IO}/\Delta T$	Temperature drift	R_S = 0 Ω		Full Range		7		µV/°C
I_{IO}	Input offset current	V_O = 1.4 V		25°C		2	50	nA
				Full Range			150	
$\Delta I_{IO}/\Delta T$	Temperature drift			Full Range		10		pA/°C
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–20	–250	nA
				Full Range			–500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to 32 V		25°C	0 to V_{CC}– 1.5			V
				Full Range	0 to V_{CC} – 2			
V_{OH}	High-level output voltage	R_L = 10 kΩ		25°C	V_{CC} – 1.5			V
		V_{CC} = 32 V	R_L = 2 kΩ	Full Range	26			
		V_{CC} = 32 V	R_L ≥ 10 kΩ	Full Range	27			
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ		Full Range		5	20	mV

6.6 Electrical Characteristics: LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1 (continued)

For $V_S = (V_+) – (V_–) = 5$ V, at $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TA[(1)]	MIN	TYP[(2)]	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ		25°C	25	100		V/mV
				Full Range	15			
	Amplifier-to-amplifier coupling[(3)]	f = 1 kHz to 20 kHz, input referred		25°C		120		dB
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C	60	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC} / \Delta V_{IO}$)			25°C	60	100		dB
V_{O1}/ V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120		dB
I_O	Output current	V_{CC} = 15, V_O = 0	V_{ID} = 1 V	25°C	–20	–30	–60	mA
				Full Range	–10			
		V_{CC} = 15, V_O = 15 V	V_{ID} = −1 V	25°C	10	20		
				Full Range	5			
		V_{ID} = −1 V	V_O = 200 mV	25°C	12	40		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V	V_O = 0	25°C		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V	No load	Full Range		0.7	1.2	mA
		V_{CC} = 32 V, V_O = 0.5 V_{CC}	No load	Full Range		1.4	3	

(1) Full range is −40°C to 125°C.
(2) All typical values are at T_A = 25°C
(3) Due to proximity of external components, ensure that coupling is not originating via stray capacitance between these external parts. Typically, this can be detected, as this type of coupling increases at higher frequencies.

6.7 Operating Conditions: LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1

For $V_S = (V_+) – (V_–) = 15$ V, at $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 30 pF, V_I = ±10 V (see Figure 7-1)	0.5	V/μs
B_1	Unity-gain bandwidth	R_L = 1 MΩ, C_L = 20 pF (see Figure 7-1)	1.2	MHz
V_N	Equivalent input noise voltage	R_S = 100 Ω, V_I = 0 V, f = 1 kHz (see Figure 7-2)	35	nV/√Hz

6.8 Typical Characteristics

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).

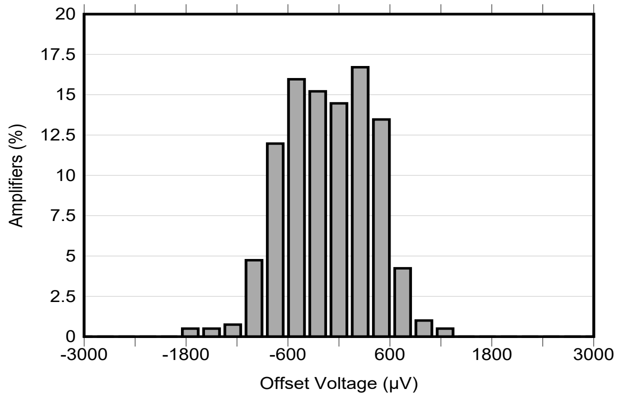


Figure 6-1. Offset Voltage Production Distribution

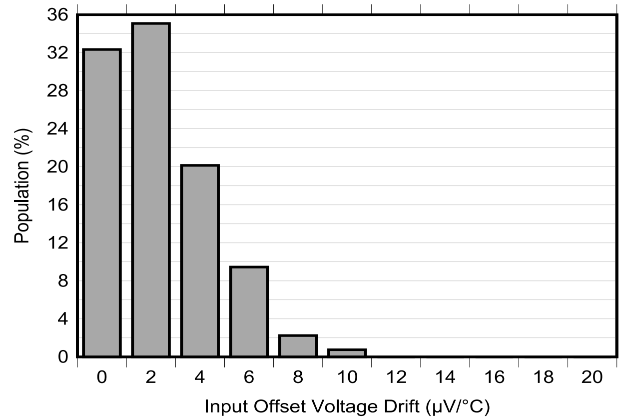


Figure 6-2. Offset Voltage Drift Distribution

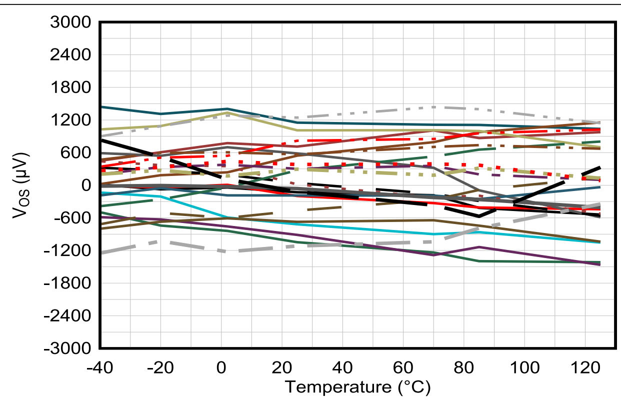


Figure 6-3. Offset Voltage vs Temperature

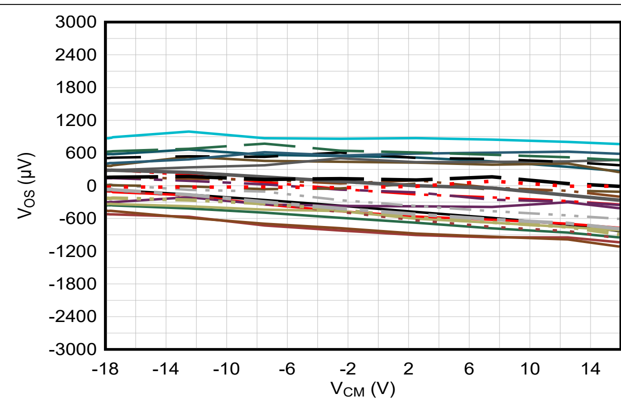


Figure 6-4. Offset Voltage vs Common-Mode Voltage

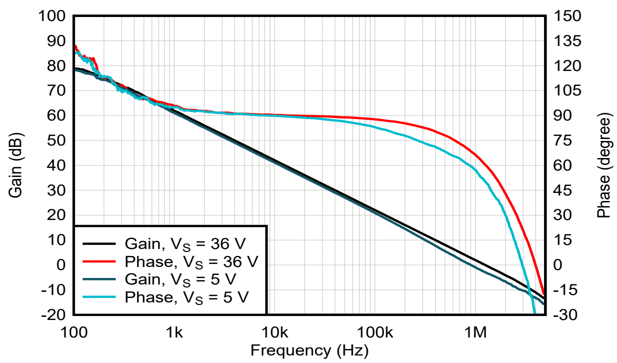


Figure 6-5. Open-Loop Gain and Phase vs Frequency

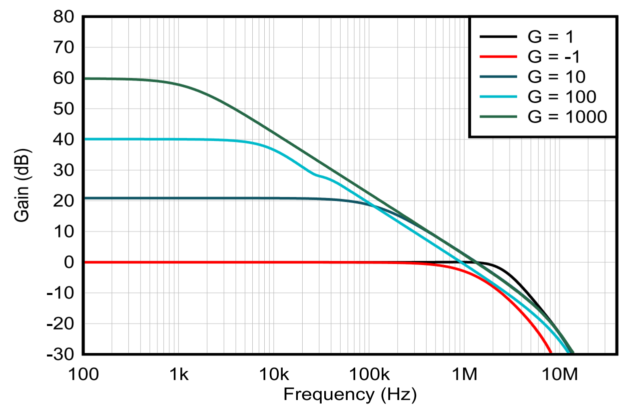


Figure 6-6. Closed-Loop Gain vs Frequency

6.8 Typical Characteristics (continued)

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).

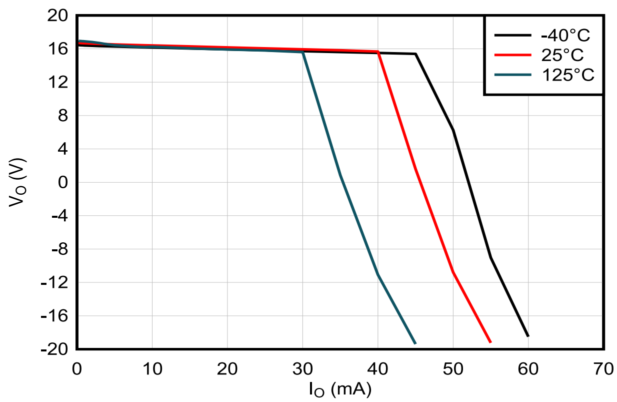


Figure 6-7. Output Voltage Swing vs Output Current (Sourcing)

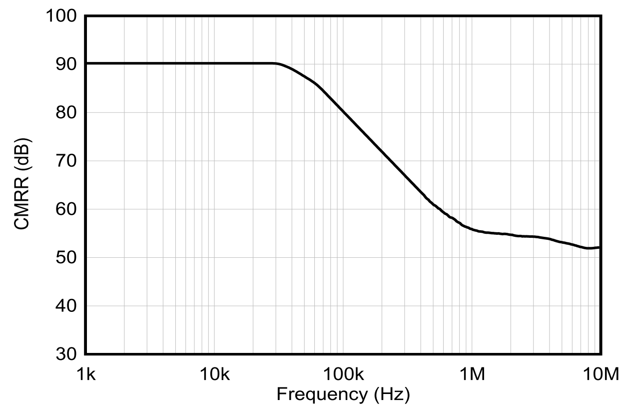


Figure 6-8. CMRR vs Frequency

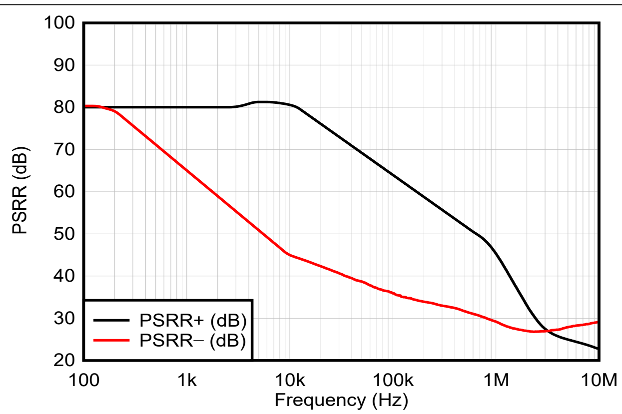


Figure 6-9. PSRR vs Frequency

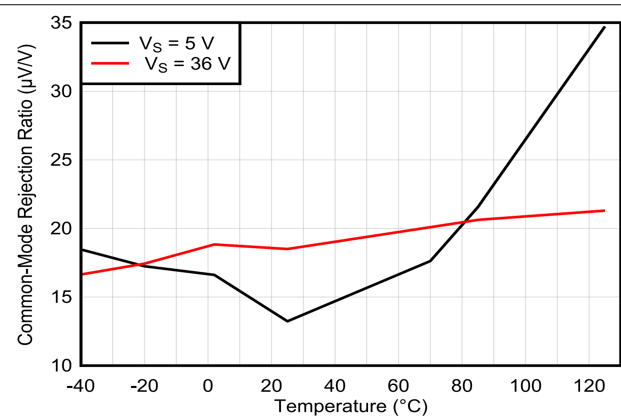
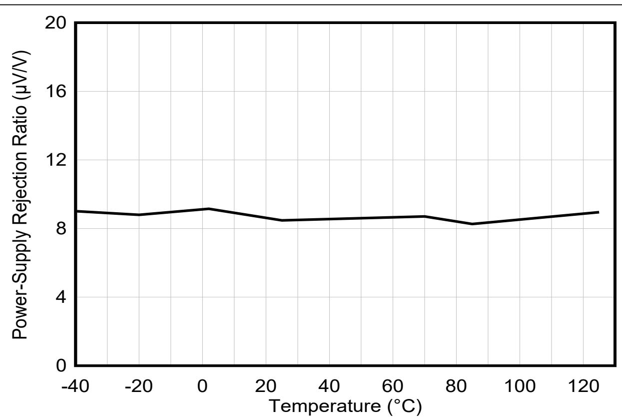


Figure 6-10. Common-Mode Rejection Ratio vs Temperature (dB)



V_S = 5 V to 36 V

Figure 6-11. Power Supply Rejection Ratio vs Temperature (dB)

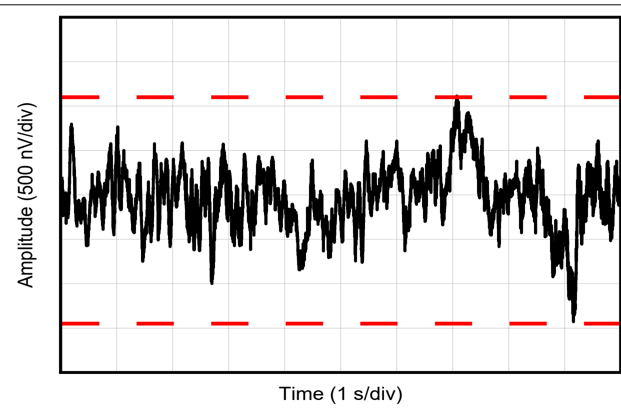


Figure 6-12. 0.1-Hz to 10-Hz Noise

6.8 Typical Characteristics (continued)

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).

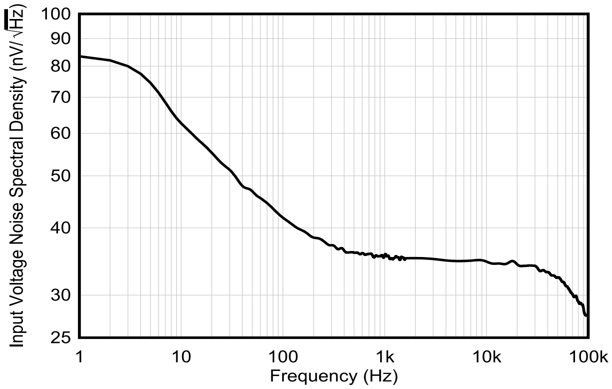
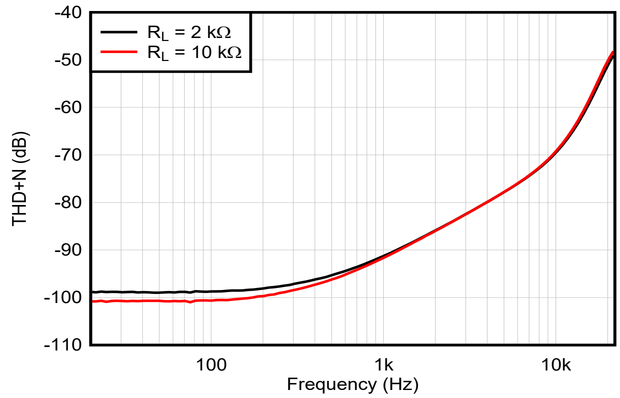


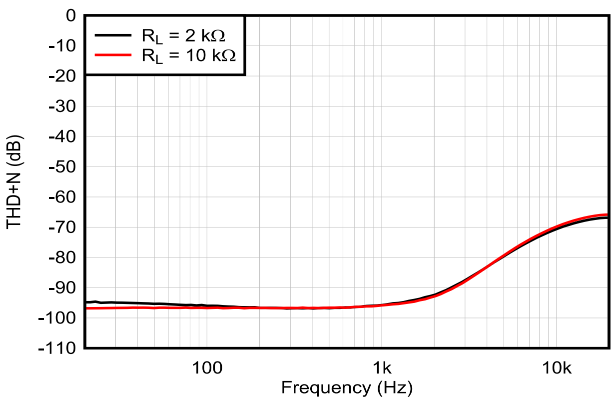
Figure 6-13. Input Voltage Noise Spectral Density vs Frequency



G = 1, f = 1 kHz, BW = 80 kHz,

V_{OUT} = 10 V_{PP}, R_L connected to V–

Figure 6-14. THD+N Ratio vs Frequency, G = 1

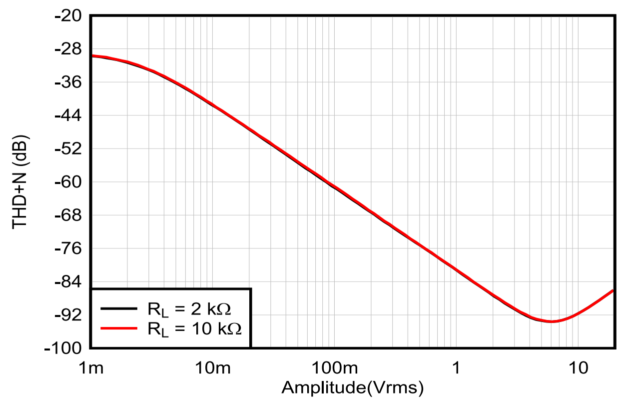


G = –1, f = 1 kHz, BW = 80 kHz,

V_{OUT} = 10 V_{PP}, R_L connected to V–

See Section 7

Figure 6-15. THD+N Ratio vs Frequency, G = –1



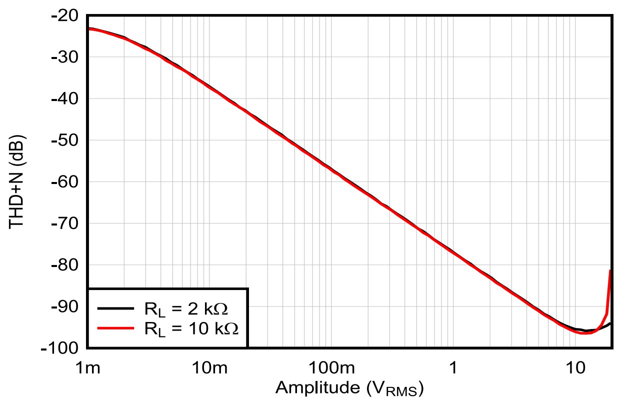
G = 1, f = 1 kHz, BW = 80 kHz,

R_L connected to V–

Figure 6-16. THD+N vs Output Amplitude, G = 1

6.8 Typical Characteristics (continued)

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).



G = –1, f = 1 kHz, BW = 80 kHz,

R_L connected to V–

See Section 7

Figure 6-17. THD+N vs Output Amplitude, G = –1

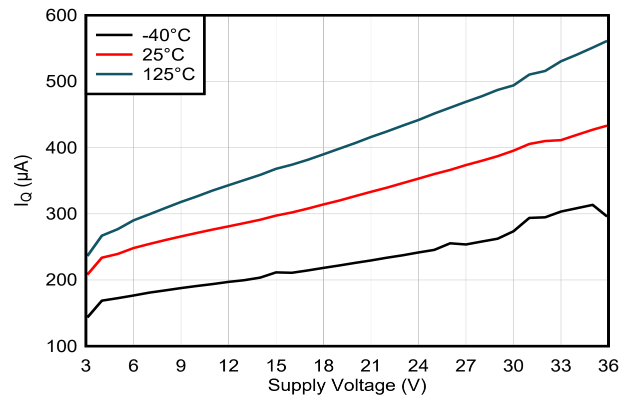


Figure 6-18. Quiescent Current vs Supply Voltage

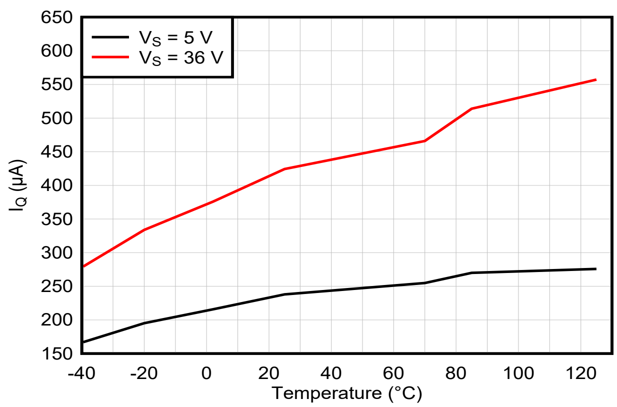


Figure 6-19. Quiescent Current vs Temperature

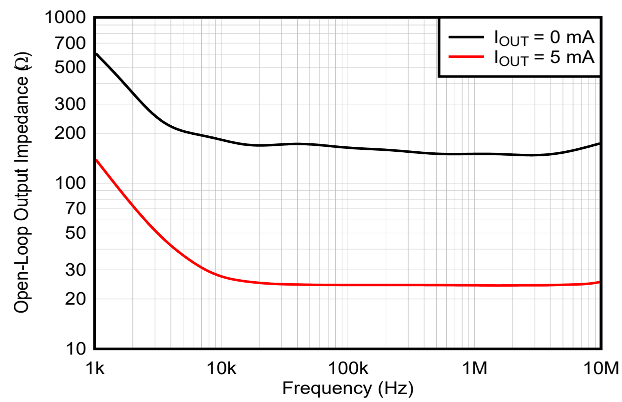
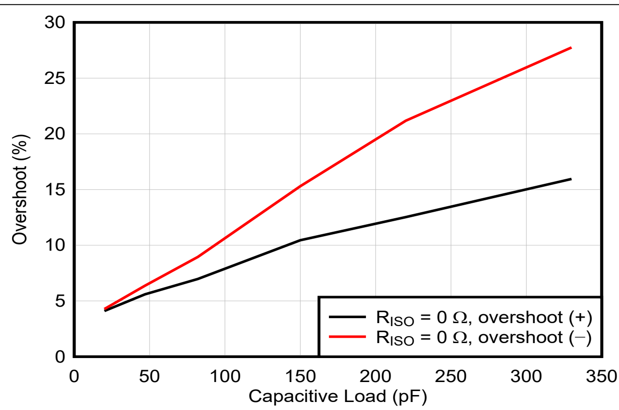
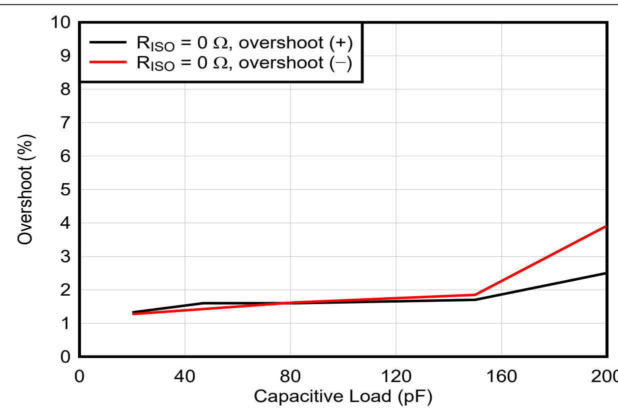


Figure 6-20. Open-Loop Output Impedance vs Frequency



G = 1, 100-mV output step, R_L = open

Figure 6-21. Small-Signal Overshoot vs Capacitive Load

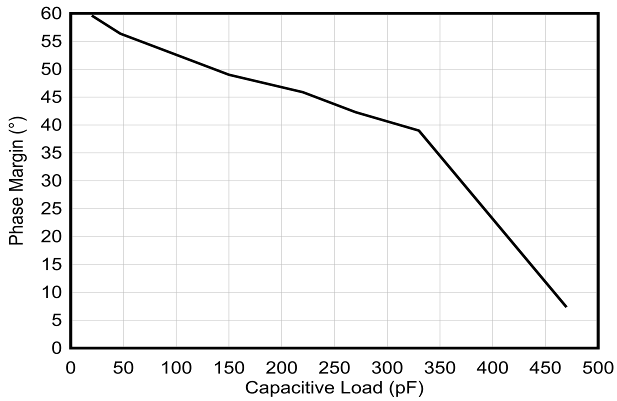


G = –1, 100-mV output step, R_L = open

Figure 6-22. Small-Signal Overshoot vs Capacitive Load

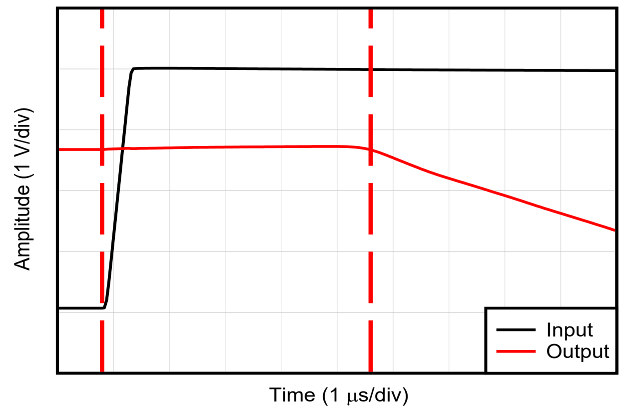
6.8 Typical Characteristics (continued)

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).



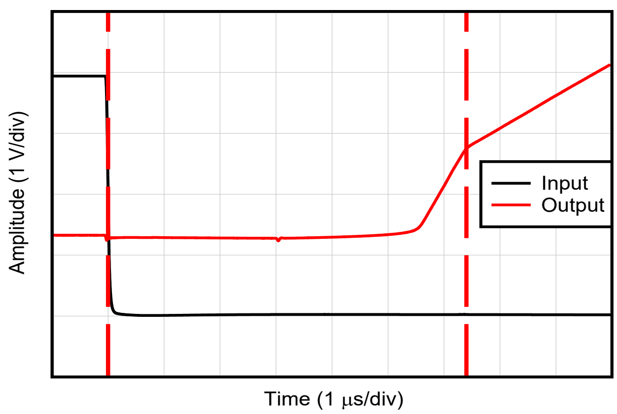
G = +1, R_L = 10 kΩ, C_L = 20 pF

Figure 6-23. Phase Margin vs Capacitive Load



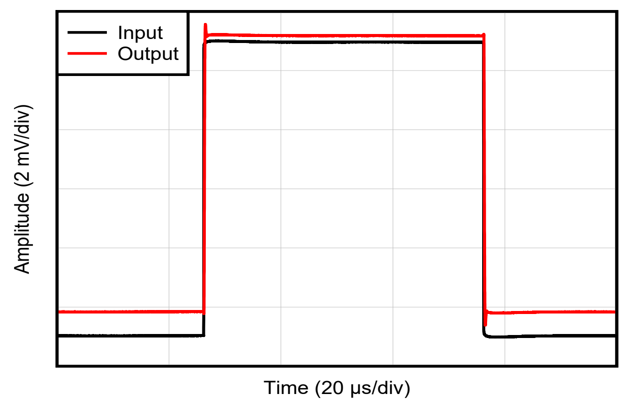
G = –10

Figure 6-24. Overload Recovery (Positive Rail)



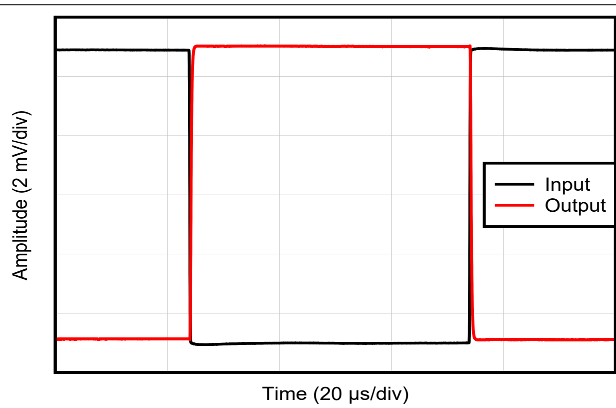
G = –10

Figure 6-25. Overload Recovery (Negative Rail)



G = 1, R_L = open

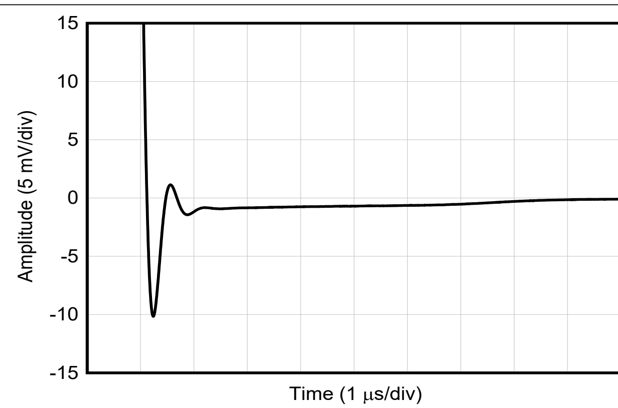
Figure 6-26. Small-Signal Step Response, G = 1



G = –1, R_L = open, R_{FB} = 10K

See Section 7

Figure 6-27. Small-Signal Step Response, G = –1

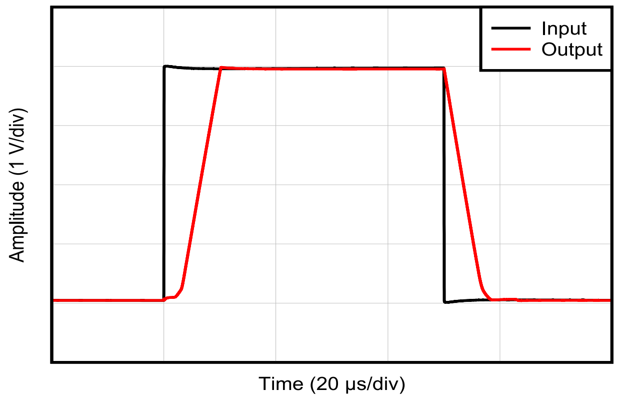


G = 1, R_L = open

Figure 6-28. Large-Signal Step Response (Falling)

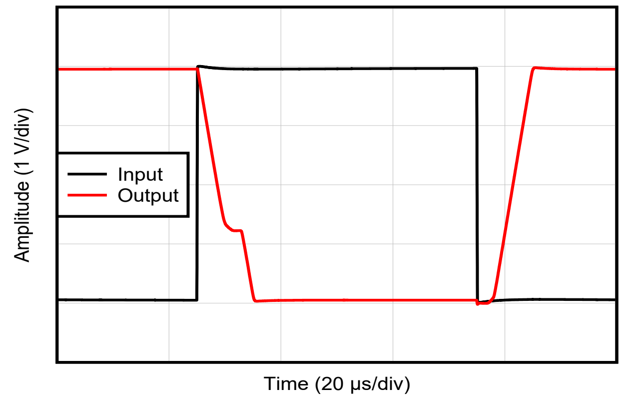
6.8 Typical Characteristics (continued)

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).



G = 1, R_L = open

Figure 6-29. Large-Signal Step Response, G = 1



G = –1, R_L = open

Figure 6-30. Large-Signal Step Response, G = –1

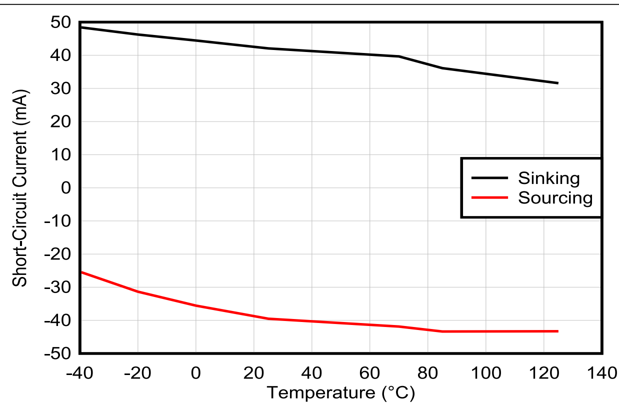
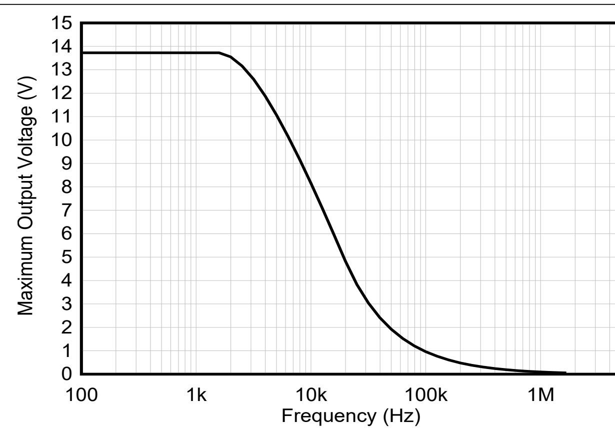


Figure 6-31. Short-Circuit Current vs Temperature



V_S = 15 V

Figure 6-32. Maximum Output Voltage vs Frequency

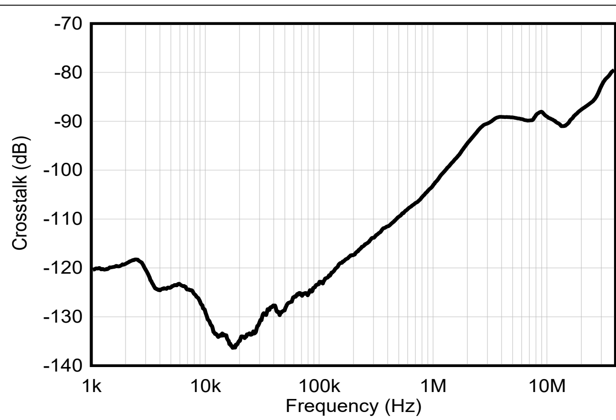


Figure 6-33. Channel Separation vs Frequency

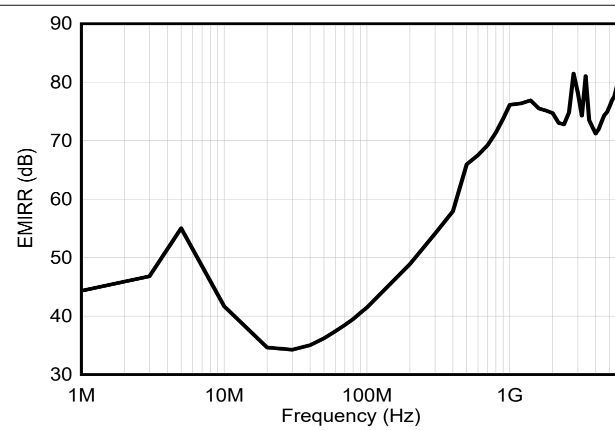


Figure 6-34. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

7 Parameter Measurement Information

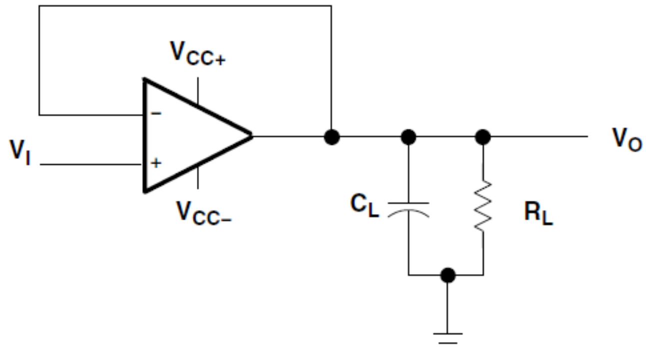


Figure 7-1. Unity-Gain Amplifier

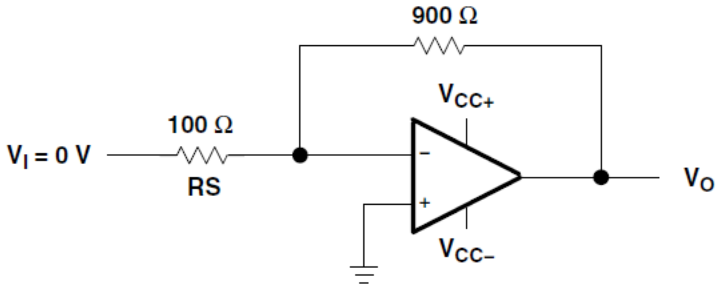


Figure 7-2. Noise-Test Circuit

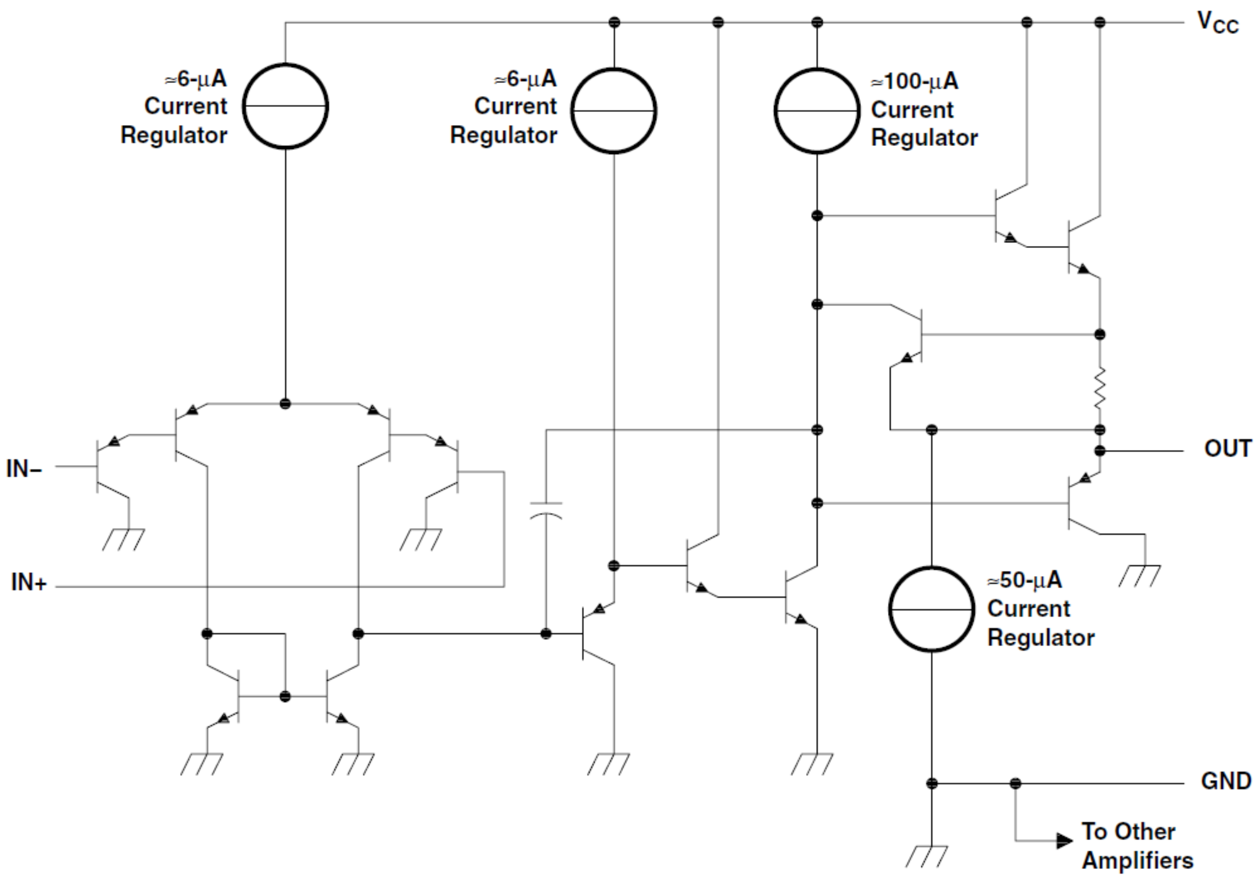
8 Detailed Description

8.1 Overview

The LM2902-Q1, LM2902B-Q1, and LM2902BA-Q1 devices consist of four independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is within the supply voltage range, and V_S is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, DC amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5-V supply used in digital systems and easily can provide the required interface electronics without additional ±5-V supplies.

8.2 Functional Block Diagram



Schematic (Each Amplifier)

8.3 Feature Description

8.3.1 Input Common Mode Range

The valid common mode range is from device ground to V_S – 1.5 V (V_S – 2 V across temperature). Inputs may exceed V_S up to the maximum V_S without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input more than 0.3 V below V– then input current should be limited to 1 mA and the output phase is undefined.

8.4 Device Functional Modes

The LM2902-Q1, LM2902B-Q1, and LM2902BA-Q1 devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier, depending on the application.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM2902-Q1, LM2902B-Q1, LM2902BA-Q1 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before V_S for flexibility in multiple supply circuits. For full application design guidelines related to this family of devices, please refer to the application report *Application design guidelines for LM324/LM358 devices*.

9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

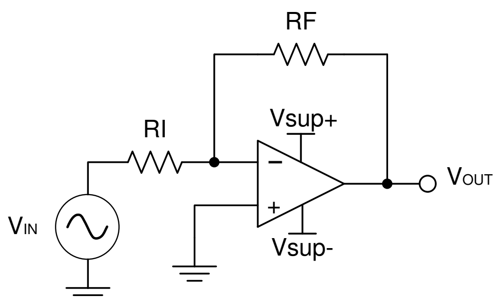


Figure 9-1. Application Schematic

9.3 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.4 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{VOUT}{VIN} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for R_I or R_F. Choosing a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliampere range. This ensures the part does not draw too much current. This example uses 10 kΩ for R_I which means 36 kΩ is used for R_F. This was determined by Equation 3.

$$A_V = -\frac{RF}{RI} \tag{3}$$

9.5 Application Curve

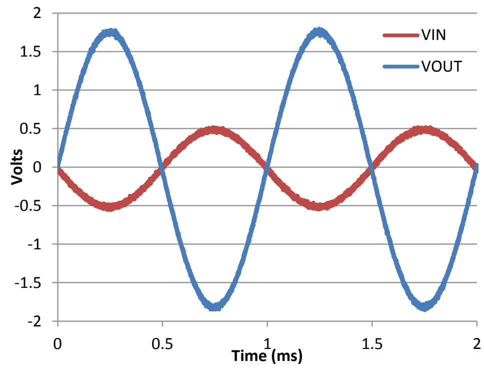


Figure 9-2. Input and Output Voltages of the Inverting Amplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than specified in the recommended operating region can permanently damage the device (see Section 6.1).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Section 11.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in Section 11.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

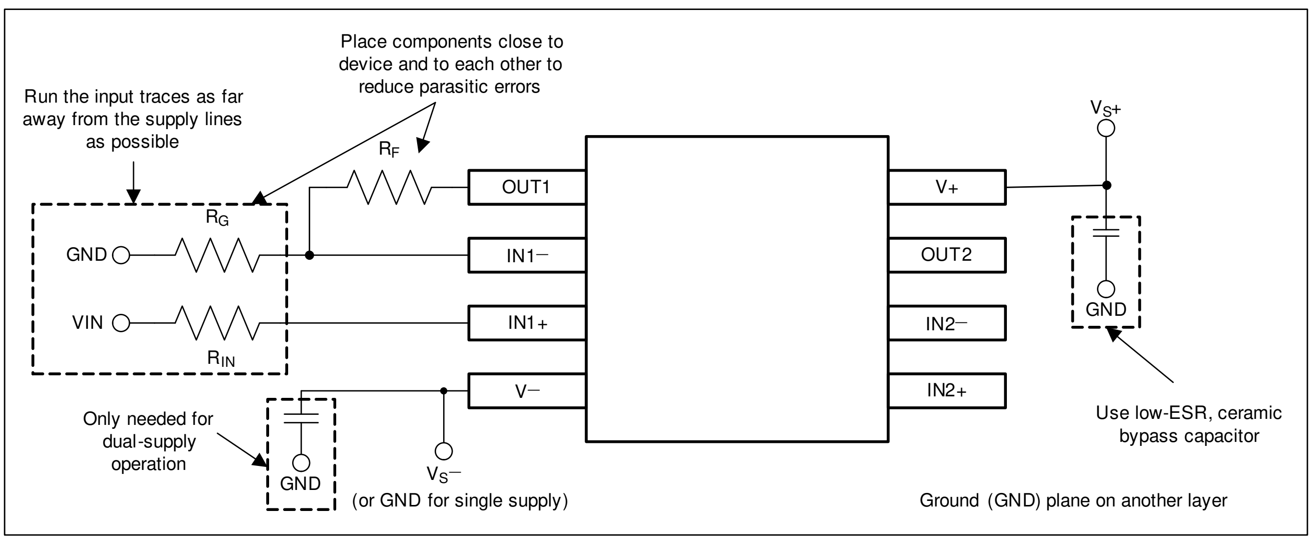


Figure 11-1. Operational Amplifier Board Layout for Noninverting Configuration

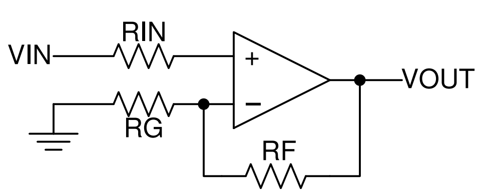


Figure 11-2. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Application Design Guidelines for LM324/LM358 Devices* application note

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2902BQPWRQ1	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902BQ	Samples
LM2902KAVQDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KAQ	Samples
LM2902KAVQPWRG4Q1	LIFEBUY	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KAQ	
LM2902KAVQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KAQ	Samples
LM2902KVQDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KVQ	Samples
LM2902KVQPWRG4Q1	LIFEBUY	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KVQ	
LM2902KVQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KVQ	Samples
LM2902QDRG4Q1	LIFEBUY	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902Q1	
LM2902QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902Q1	Samples
LM2902QPWRG4Q1	LIFEBUY	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902Q1	
LM2902QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM2902-Q1, LM2902B-Q1 :

- Catalog : LM2902, LM2902B

- Enhanced Product : LM2902-EP

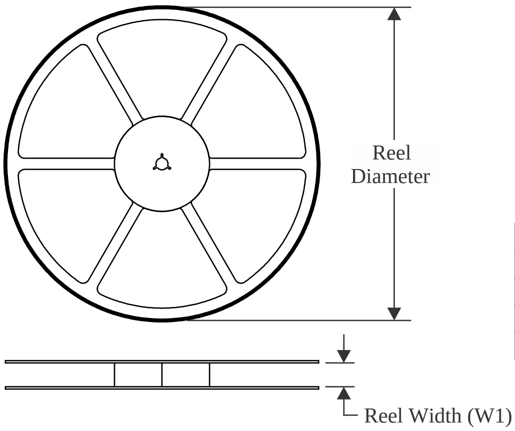
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

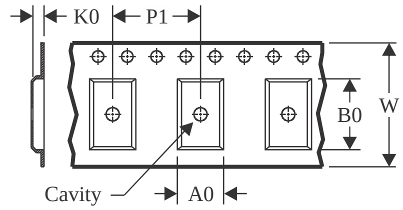
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

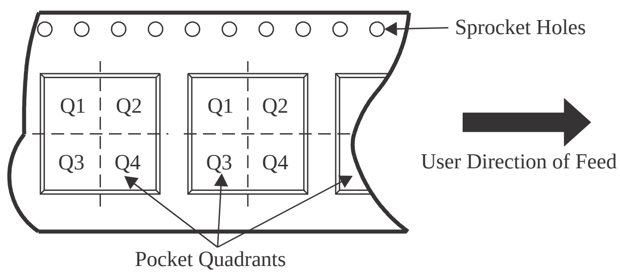


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

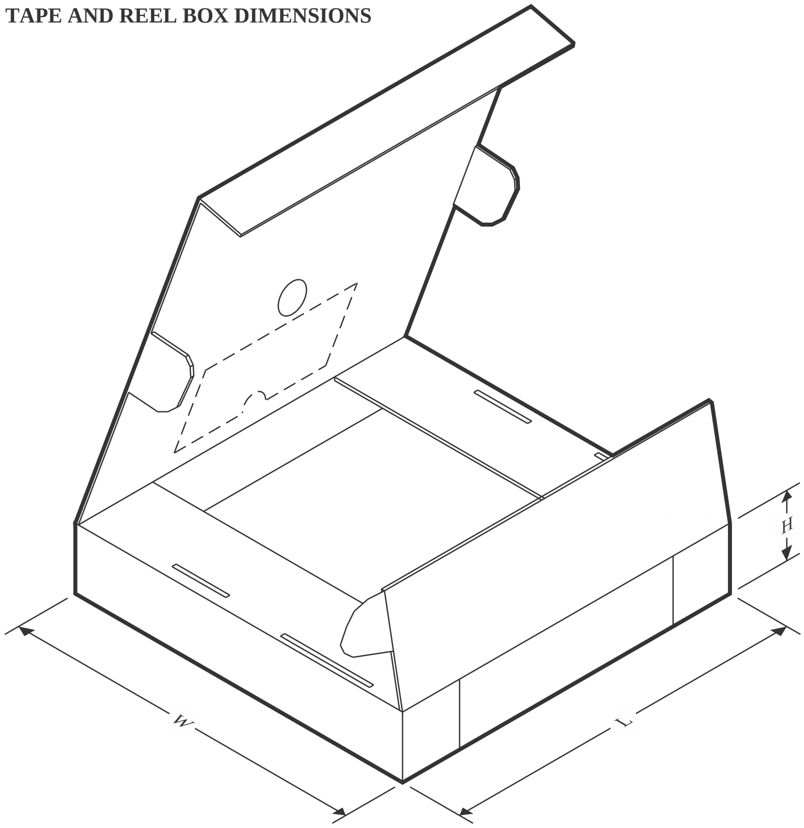
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2902BQPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KAVQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KAVQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KVQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KVQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

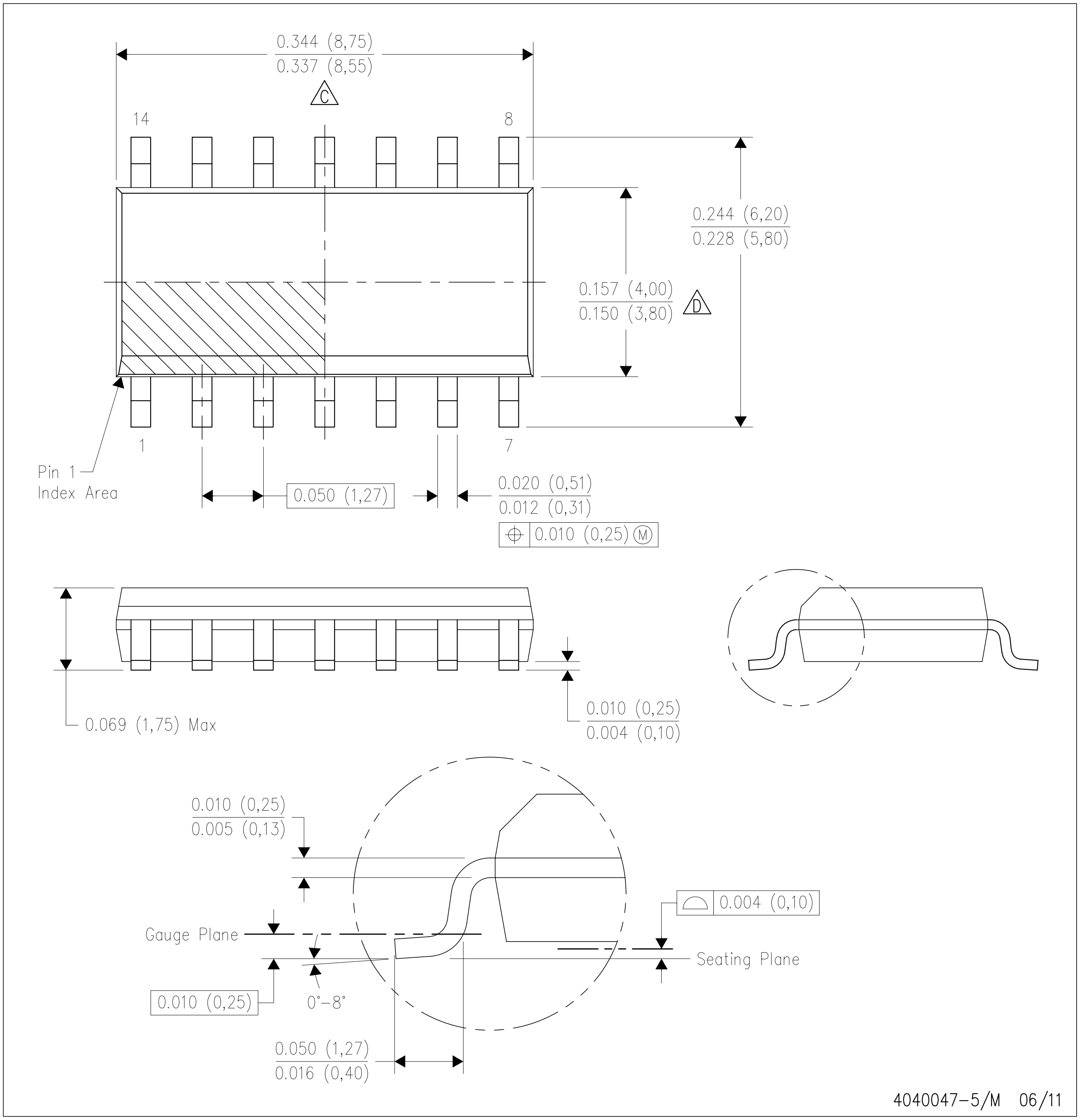
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

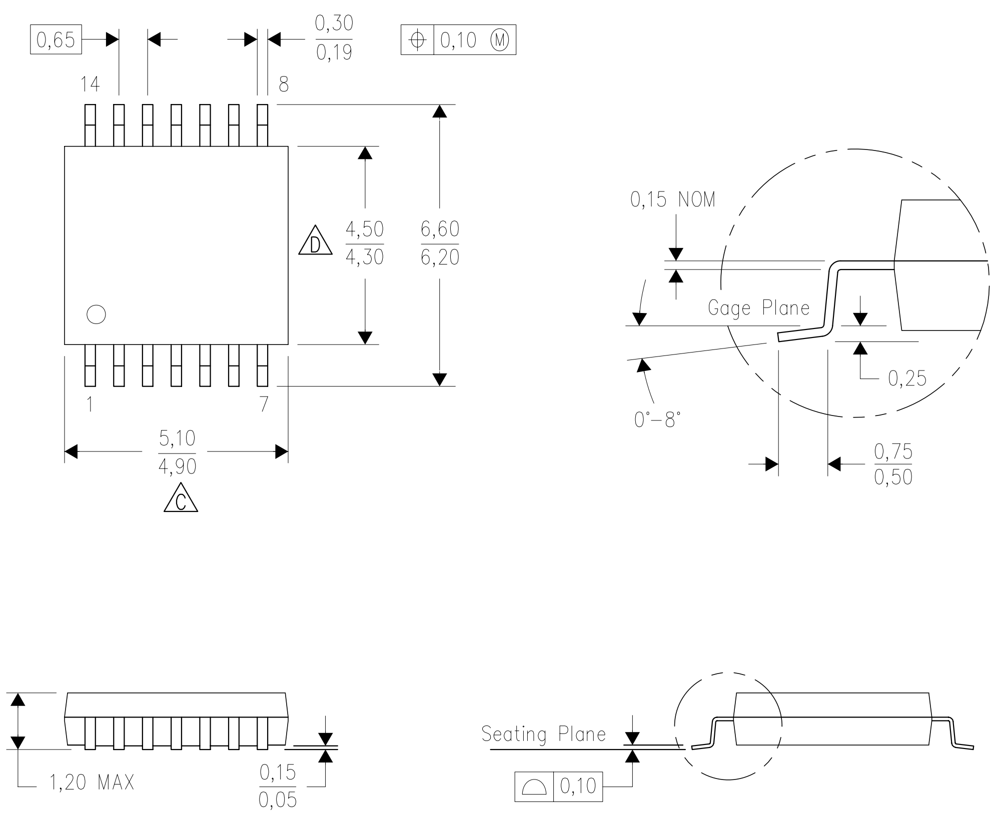
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2902BQPWRQ1	TSSOP	PW	14	3000	356.0	356.0	35.0
LM2902KAVQPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902KAVQPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902KVQPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902KVQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2902QPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2902QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153