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PRODUCT SPECIFICATION

TFT-LCD MODULE

Model No: WTIMV70E-01

For Customer's Acceptance	
Approved by	Comment

	Signature	Date
Prepared by		
Checked by		
Approved by		

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1.0 GENERAL DESCRIPTION

1.1 Introduction

The model WTIMV70E-01 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This TFT LCD has a 7.0 (9:16) inch diagonally measured active display area with HD (720 horizontal by 1280 vertical pixel) resolution.

1.2 Features

- 6.95 (16:9 diagonal) inch configuration
- 16.7M color by 8 bit mipi signal input
- RoHS Compliance & Halogen Free

1.3 Applications

- Mobile Smart Phone
- Personal Navigation Device
- Multimedia applications and AV system

1.4 General information

Item	Specification	Unit
Screen Size	7.0 inches	Diagonal
Number of Pixel	720 RGB (H) × 1280(V)	Pixels
Display area	86.94(H) x 154.56(V)	mm
Outline Dimension	95.0x163.3x2.6 (Typ)	mm
Display mode	Normally Black	--
Pixel arrangement	RGB Vertical stripe	--
Pixel pitch	0.1239 (H) × 0.119 (V)	mm
Optima View Direction	ALL VIEW	--
Surface treatment	HC	--
Interface	MIPI	

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1.5 Mechanical Information

Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal (H)	94.8	95.0	95.2	mm
	Vertical (V)	163.1	163.3	163.5	mm
	Depth (D)	2.45	2.6	2.75	mm
Weight		--	TBD	--	g

2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Absolute maximum ratings

Symbol	Parameter	Unit	Value	Note
VCCD/IOVCC	Interface Supply Voltage	V	-0.3 to +3.6	Note ^{(3),(4)}
VCI	Logic Supply Voltage	V	-0.3 to +6.6	Note ^{(3),(5)}
VCIP	Analog Supply Voltage	V	-0.3 to +6.6	Note ^{(3),(6)}
VCCH	High speed interface Supply Voltage	V	-0.3 to +3.6	Note ^{(3),(7)}
AVDD	Positive Voltage input	V	-0.3 to +6.6	Note ⁽⁸⁾
AVEE	Negative Voltage input	V	0 to -6.6	Note ⁽⁹⁾
VGH	Power Supply Voltage	V	-0.3 to +25	Note ⁽¹⁰⁾
VGL	Power Supply Voltage	V	0 to -16	Note ⁽¹¹⁾
Top	Operating Temperature	°C	-40 to +85	Note ⁽¹²⁾
Tstg	Storage Temperature	°C	-55 to +110	Note ⁽¹³⁾

Note: (1) Permanent device damage may occur if absolute maximum conditions are exceeded.

(2) Functional operation should be restricted to the conditions described under DC Characteristics.

(3) VCCD/IOVCC, VSSD must be maintained.

(4) To make sure $VCCD/IOVCC \geq VSSD$.

(5) To make sure $VCIP \geq AVSS$.

(6) To make sure $VCI \geq AVSS$.

(7) To make sure $VCCH \geq VSSH$.

(8) To make sure $AVDD \geq AVSS$.

(9) To make sure $AVSS \geq AVEE$

(10) To make sure $VGH \geq AVSS$.

(11) To make sure $AVSS \geq VGL$

$$VGH + |VGL| < 30V$$

(12) For die and wafer products, specified up to +85°C.

(13) This temperature specifications apply to the COG package.

2.2 Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit
Storage temperature	T _{STG}	-10	60	°C
	RH		90	%
Operating temperature	T _{OPR}	00	50	°C
	RH		90	%

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3.0 OPTICAL CHARACTERISTICS

3.1 Optical specification

Item	Symbol	Condition	Min	Type	Max	Unit	Note
White luminance (Center)	YL	$\Theta=0$ Normal Viewing Angle	250	300	TBD	nits	(1)(4)(6)
Response time	T_r		--	10	15	msec	(1)(3)
	T_f		--	20	25		
Contrast ratio	CR		600	800	--	--	(1)(2)
Color Chromaticity (CIE 1931)	white	W_x	0.260	0.310	0.360		(1)(4)
		W_y	0.280	0.330	0.380		
Viewing Angle	Hor.	Θ_L	70	80	--		(1)(4)
		Θ_R	70	80	--		
	Ver.	Θ_U	70	80	--		
		Θ_D	70	80	--		
Transmittance			3.65	4.05		%	
Brightness uniformity	BUNI	$\Theta=0$	--	50	--	%	(5)
Optima View Direction	ALL VIEW						

3.2 Measuring Condition

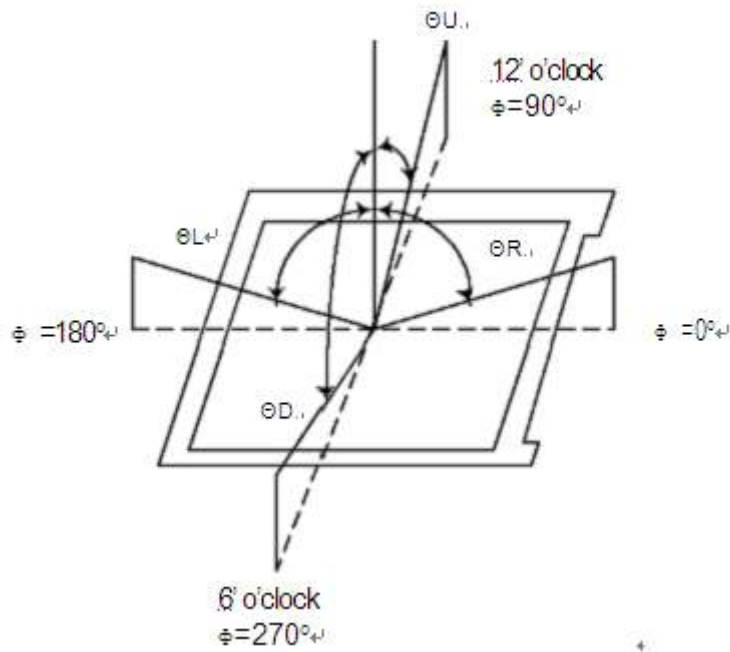
- Measuring surrounding: dark room
- LED current IL:60mA
- Ambient temperature: 25±2°C
- 30min. warm-up time

3.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1)

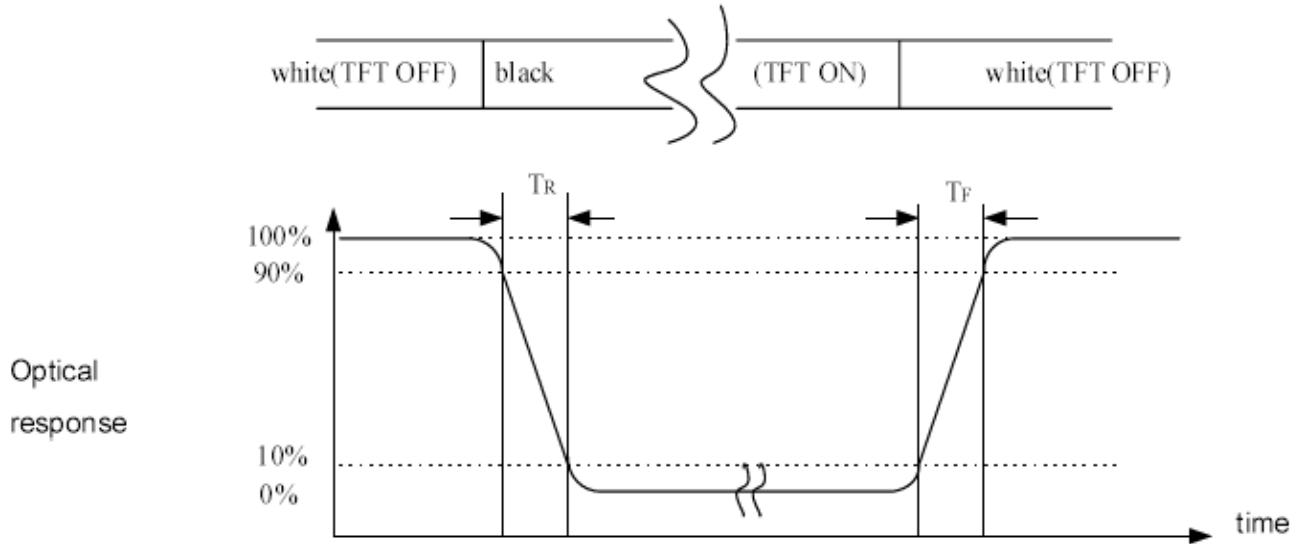
Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).


Note (2) Definition of Contrast Ratio(CR):
 Measured at the center point of panel

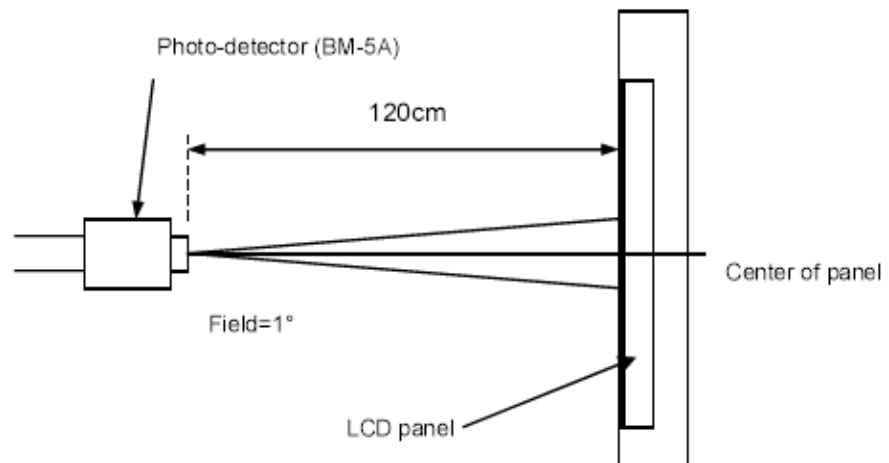
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

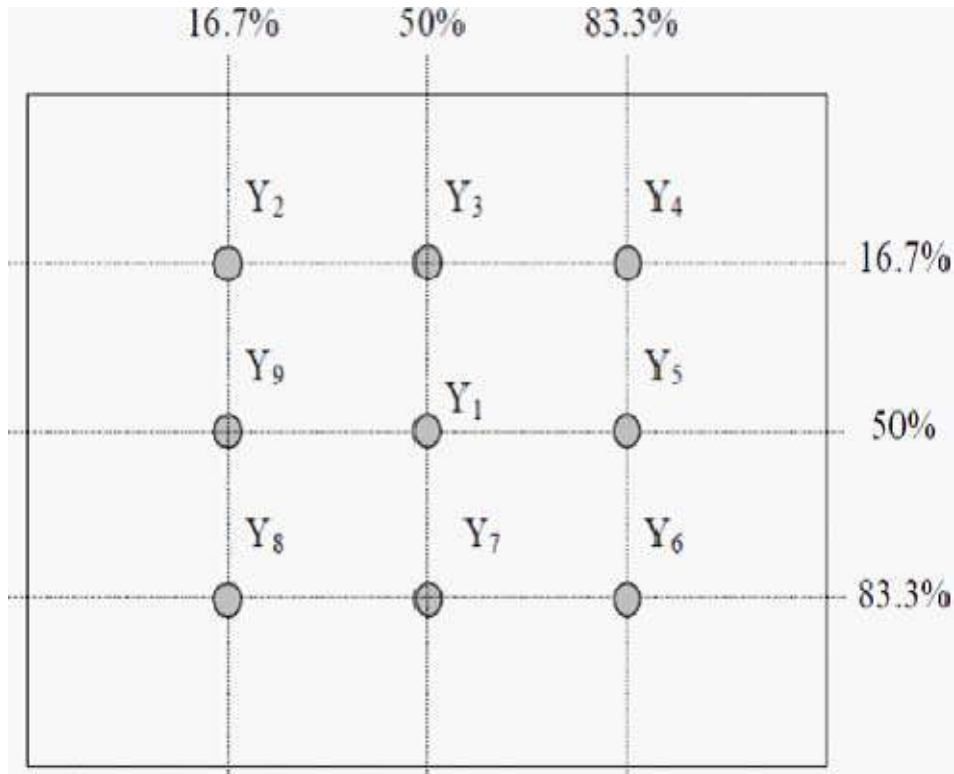
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Note (3) Definition of Response Time: Sum of T_R and T_F



Note (4) Definition of optical measurement setup



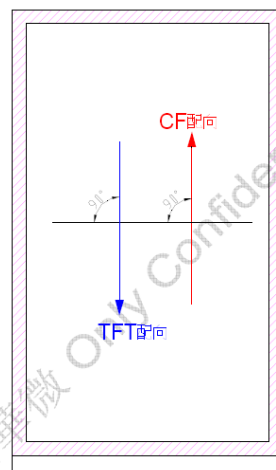
Note (5) Definition of brightness uniformity


(Min Luminance of 9 points)

$$\text{Luminance uniformity} = \frac{\text{Min Luminance of 9 points}}{\text{Max Luminance of 9 points}} \times 100 \%$$

(Max Luminance of 9 points)

Note (6) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)

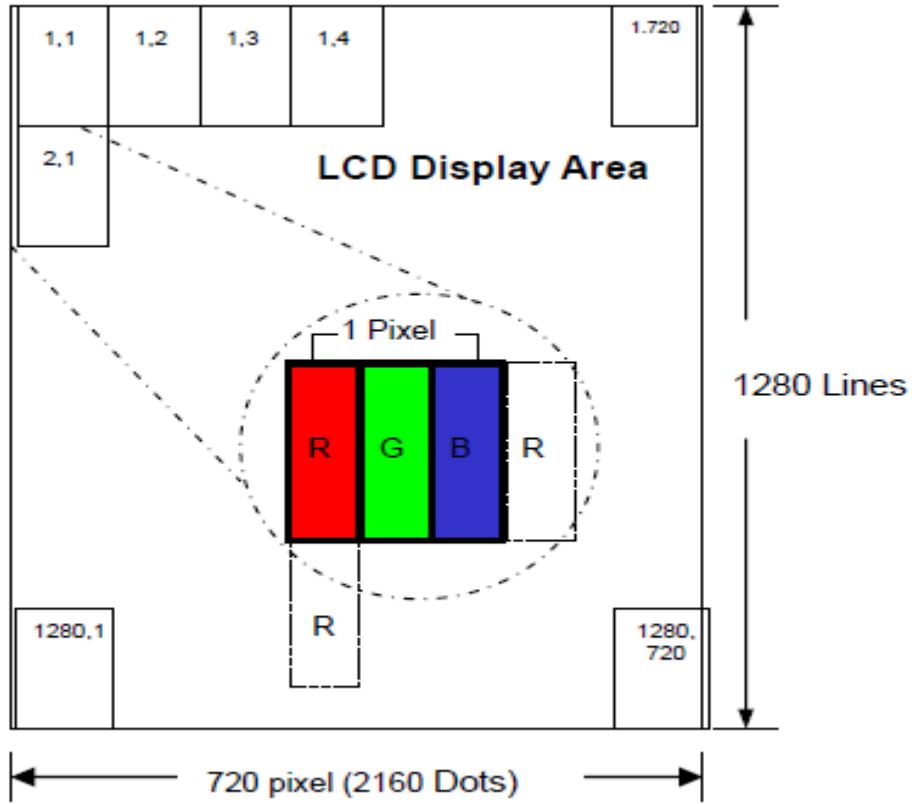


Viewing from CF Glass Side

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4.0 BLOCK DIAGRAM

4.1 TFT LCD Module



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5.0 INTERFACE PIN CONNECTION**5.1 PIN ASSIGNMENT****PIN DEFINITION**

NO.	TFT	
1	GND	
2	IOVCC1.8	
3	NC	
4	GND	
5	MIPI N2	
6	MIPI P2	
7	GND	
8	MIPI P0	
9	MIPI N0	
10	GND	
11	MIPI P1	
12	MIPI N1	
13	GND	
14	MIPI TCN	
15	MIPI TCP	
16	GND	
17	MIPI P3	
18	MIPI N3	
19	GND	
20	REST	
21	NC	
22	NC	
23	GND	
24	NC	
25	VDD3.3V	
26	NC	
27	NC	
28	LED K	
29	LED K	
30	LED A	
31	LED A	
32	GND	

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5.2 Back-Light Unit

The backlight system is an edge-lighting type with 18 LED.

The characteristics of the LED are shown in the following tables.

Item	Symbol	Min	Typ	Max	Unit	Note
LED current	IL	60	-	-	mA	
LED voltage	VL	-	21.0	-	V	
Operating LED life time	Hr	-	15000	-	Hour	(1)

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: $T_a=25\pm 3\text{ }^{\circ}\text{C}$, typical IL value indicated in the above table and the $f_L=50\text{k}$ Hz until the brightness becomes less than 50%.

6.0 ELECTRICAL CHARACTERISTICS**6.1 DC characteristics**

($T_A = -40 \sim 85^{\circ}\text{C}$, $V_{CIP}=2.5 \sim 4.8\text{V}$, $V_{CI}=2.5 \sim 4.8\text{V}$, $V_{CCD}/I_{OVCC}=1.65\sim 3.3\text{V}$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V _{CCD} /I _{OVCC}	V _{IN}	Interface Supply Voltage	1.65	-	3.6	
V _{CIP}	V _{IN}	Logic Supply Voltage	2.5	-	6.0	
V _{CI}	V _{IN}	Analog Supply Voltage	2.5	-	6.0	
V _{CCH}	V _{IN}	High speed interface Supply Voltage	1.65	-	3.6	
Input high voltage	V _{IH}	V _{CCD} /I _{OVCC} = 1.65 ~ 3.3V	0.7	-	V _{CCD} /I _{OVCC}	V
Input low voltage	V _{IL}	V _{CIP} = 2.5 ~ 3.3V V _{CI} = 2.5 ~ 3.3V	0	-	0.3 V _{CCD} /I _{OVCC}	V
V _{PP}	V _{IH} V _{IL}	V _{PP}	7.25V	7.5V	7.75V	V
Output high voltage (SDO, LEDPWM)	V _{OH1}	I _{OH} = -1.0 mA	0.8	-	V _{CCD} /I _{OVCC}	V
Output low voltage (SDO, LEDPWM)	V _{OL1}	V _{CCD} /I _{OVCC} = 1.65 ~ 2.4V I _{OL} = 1.0 mA	0	-	0.2 V _{CCD} /I _{OVCC}	V
Logic High level input current	I _{IH}	V _{SYNC} , H _{SYNC}	-	-	1	μA
	I _{IHD}	RESX, DCX_SCL, CSX, RDX, WRX_SCL DB[23...0], SDI, DCX DB[23...0]	-	-	1	μA
Logic Low level input current	I _{IL}	V _{SYNC} , H _{SYNC}	-1	-		μA
		RESX, DCX, CSX, RDX, WRX_SCL	-1	-		μA
	I _{ILD}	DB[23...0], SDI, DCX DB[23...0]	-1	-		μA
Current consumption standby mode (V _{CIP} /V _{CI} -V _{SSD})	I _{ST(VDD)}	V _{CIP} /V _{CI} =2.8V, V _{CCD} /I _{OVCC} =1.8V T _A =25°C	-	TBD	-	μA
Current consumption standby mode (V _{CCD} /I _{OVCC} -V _{SSD})	I _{ST(VCCD/I_{OVCC})}		-	TBD	-	μA
Current consumption during Deep-standby mode (V _{CIP} /V _{CI} -V _{SSD})	I _{DP-ST(VDD)}	V _{CIP} /V _{CI} =2.8V, V _{CCD} /I _{OVCC} =1.8V T _A =25°C	-	TBD	-	μA
Current consumption during Deep-standby mode (V _{CCD} /I _{OVCC} -V _{SSD})	I _{DP-ST(VCCD/I_{OVCC})}		-	TBD	-	μA

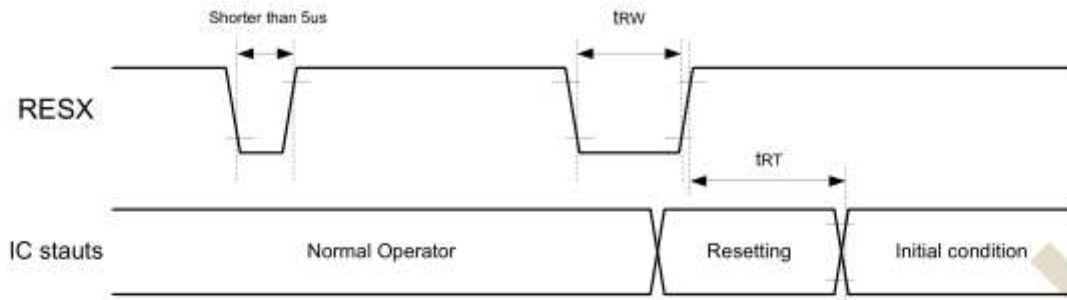
Note: 1. The VOTP pin is open on normal mode and in used while OTP programming condition.

2. The GRAM data is eliminated under the Deep standby mode.

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6.2 AC characteristics**6.2.1. Reset input timings****Figure 11.1: Reset input timings**

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width ⁽²⁾	RESX	10	-	μ s
t_{RT}	Reset complete time ⁽³⁾	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

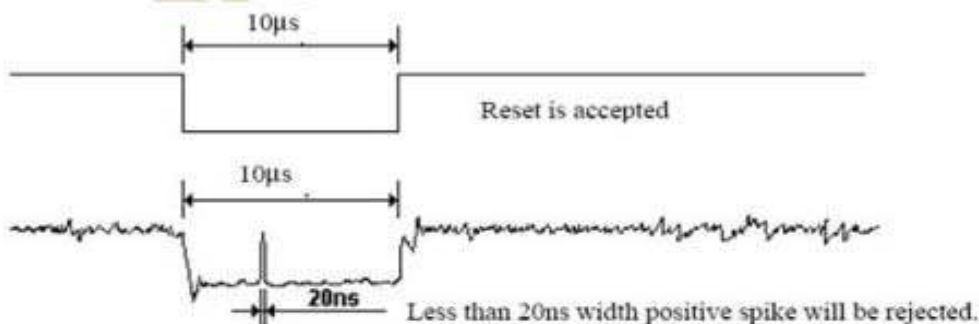
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μ s	Reset Rejected
Longer than 10 μ s	Reset
Between 5 μ s and 10 μ s	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

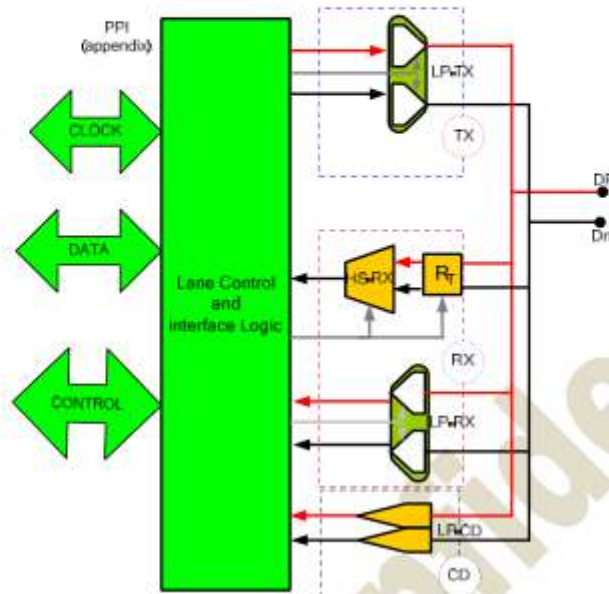
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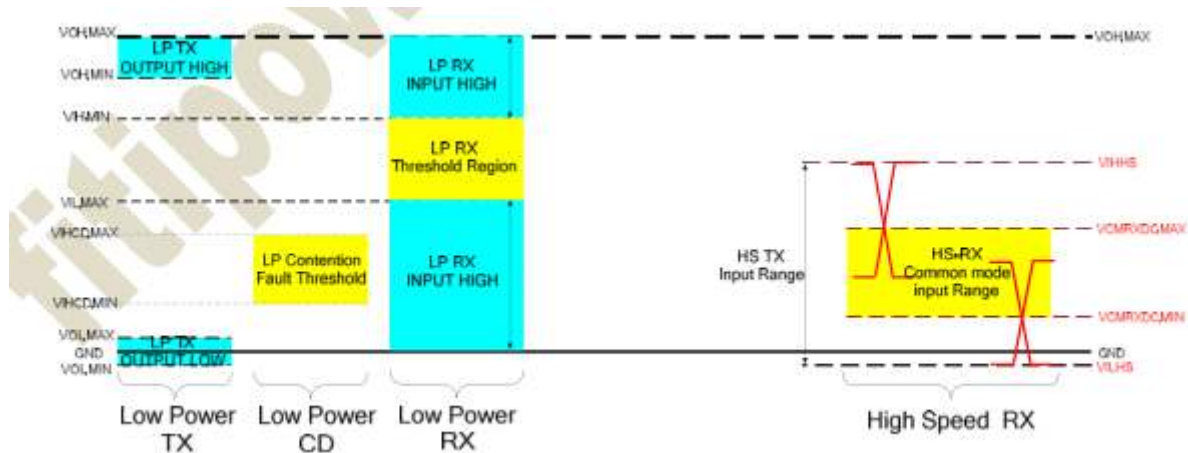
6.2.2. DSI D-PHY electronic characteristics**The Description of D-PHY Layer**

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 13.2 shows the complete set of electronic functions required for a fully featured PHY transceiver.



shows both the HS and LP signal levels of electronic characteristics, respectively.

Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.



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The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V _{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V _{OL}	Thevenin output low level	-50	-	50	mV	
Z _{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1) Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t _{RLP} /t _{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
T _{LP-PER-TX}	Period of the LP exclusive-OR clock	90			ns	
δV/δt _{SR}	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 - 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C _{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

(2) When the output voltage is between 400 mV and 930 mV.

(3) Measured as average across any 50 mV segment of the output signal transition.

(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.

(5) This value represents a corner point in a piecewise linear curve.

(6) When the output voltage is in the range specified by VPIN(absmax).

(7) When the output voltage is between 400 mV and 700 mV.

(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.

(9) When the output voltage is between 700 mV and 930 mV.

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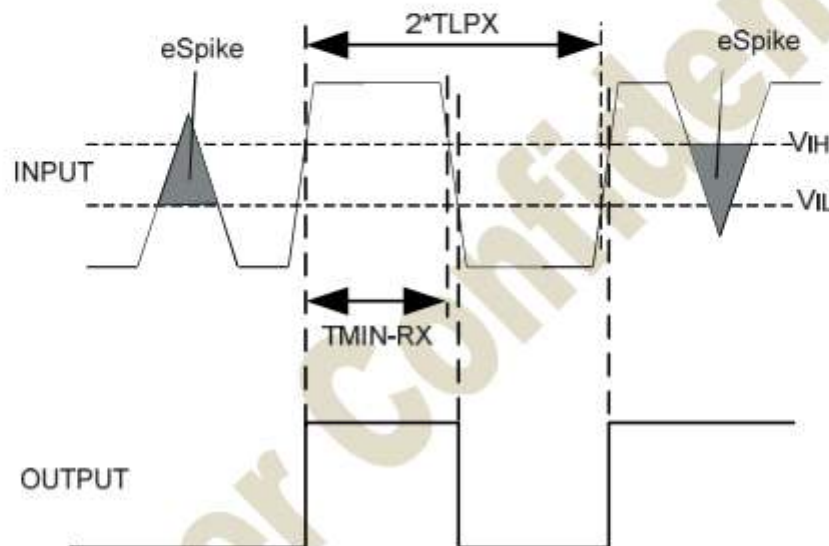
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The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 13.4 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX.



Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input threshold	880	-	-	mV	-
V_{IL}	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

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Line Contention Detection

Contention can be inferred by following conditions:

1. Detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL.
2. Detect an LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VIHCD.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V _{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V _{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, Z_{ID}, between the positive input pin D_p and the negative input pin D_n. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V _{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
V _{IDTH}	Differential input high threshold	-	-	70	mV	-
V _{IDTL}	Differential input low threshold	-70	-	-	mV	-
V _{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V _{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
Z _{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 1: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
ΔV _{CMRX(HF)}	Common mode interference beyond 450 MHz	-	-	100	mV _{pp}	(1)
C _{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) ΔV_{CMRX(HF)} is the peak amplitude of a sine wave superimposed on the receiver inputs.

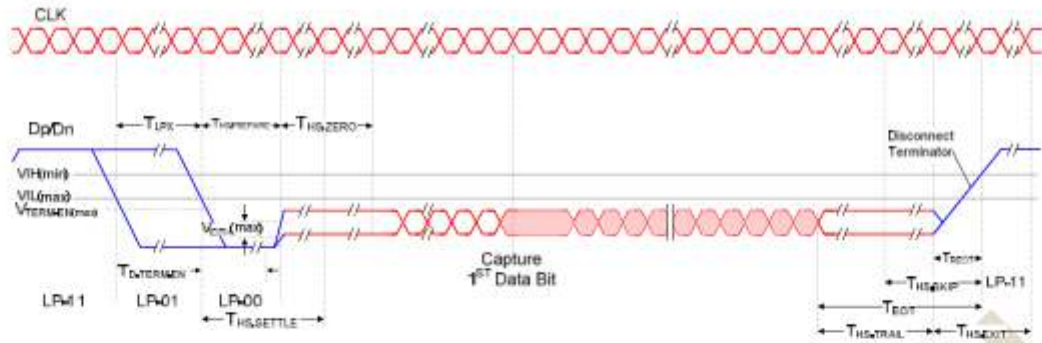
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 2: HS Receiver AC Specifications

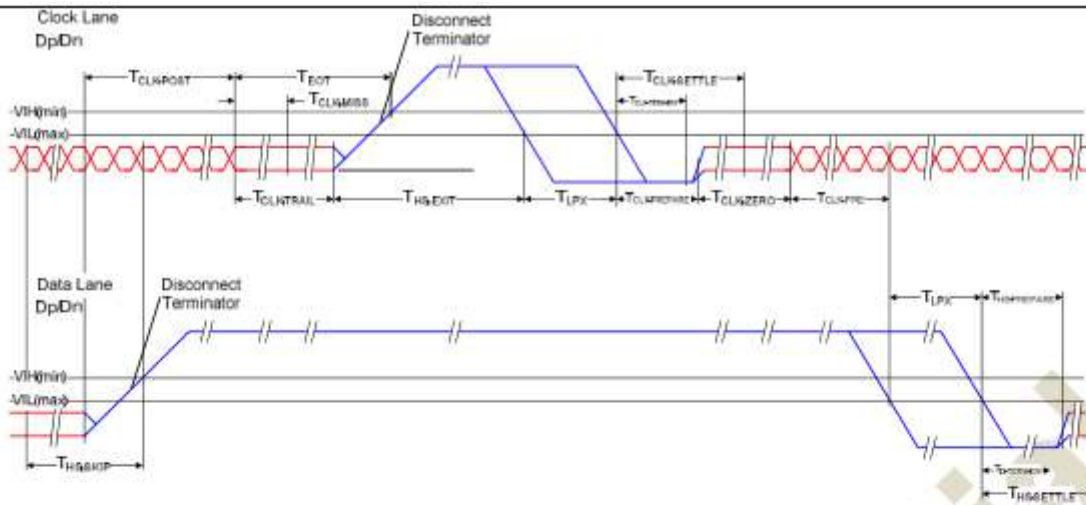
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Burst Mode Data Transmission**Figure 1 : High-Speed Data Transmission in Bursts**

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40 + 4*UI$	-	$85 + 6*UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145 + 10*UI$	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	$35 + 4*UI$	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	$85 + 6*UI$	-	$145 + 10*UI$	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$\max(n*8*UI, 60 + n*4*UI)$	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns


Figure : Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	$60 + 52 \cdot UI$	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	$8 \cdot UI$	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

6.2.3 Timings for DSI Video mode

Vertical Timings

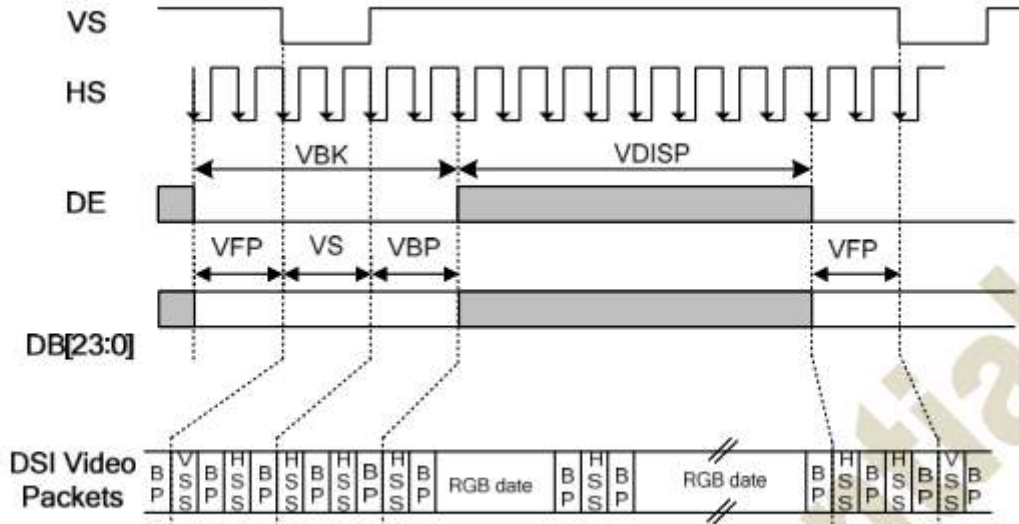


Figure 11.9: Vertical Timings for DPI I/F

Resolution=720x1280 (T_A=25°C, V_{CCD}/I_{OVCC}=1.8V, V_{CIP}=2.8V, V_{CI}=2.8V)

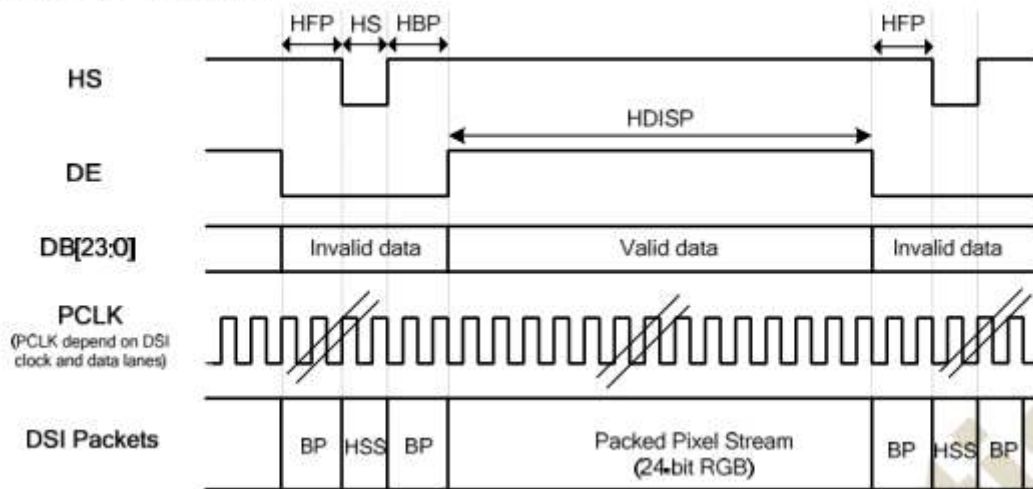
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

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Horizontal Timings

Resolution=720x1280 (TA=25°C, VCCD/IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	-	88	DCK
Horizontal active area	HDISP	-	-	720	-	DCK

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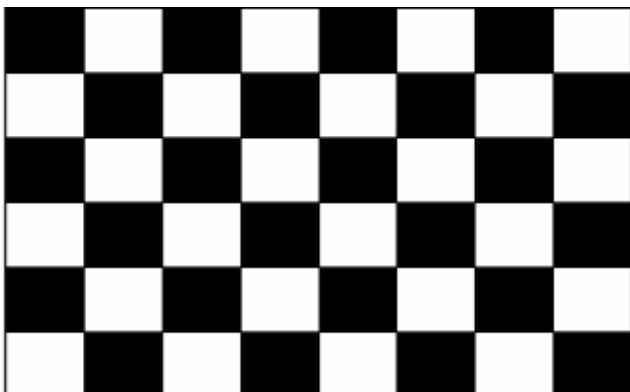
7.0 RELIABILITY TEST ITEMS

No.	Item	Conditions	Notes
1	High Temperature Storage	Ta=+60°C, 240hrs	
2	Low Temperature Storage	Ta=-20°C, 240hrs	
3	High Temperature Operation	Ta=+50°C, 240hrs	
4	Low Temperature Operation	Ta=-10°C, 240hrs	
5	High Temperature and High Humidity(operation)	Ta=+50°C, 90%RH ,240hrs	
6	Thermal cycling Test	-10°C/30 min ~ +60°C/30 min for a total 200 cycles, Start with cold temperature and end with high temperature.	
7	Vibration	1.Frequency range:8~33Hz 2.Stoke:1.3 mm 3.Vibration:sinusoidal wave, perpendicular axis(both x,z axis:2hrs, y axis 4Hrs)\ 4. Sweep : 2.9G, 33.3Hz-400Hz 5. Cycle : 15 Min	
8	Shock	1.Shock level : 980m/s ² (equal to 100G) 2.Waveform:1/2 Sine wave, 6msec 3.±X, ±Y, ±Z,each axis 1 times	
9	ESD	150pF, 330Ω, ±8kV&±15kV Air & Contact test	1
		200pF,0Ω ±200V Contact test	2
10	Load upon operation	50~200g	LCM
		30~120g	With TP

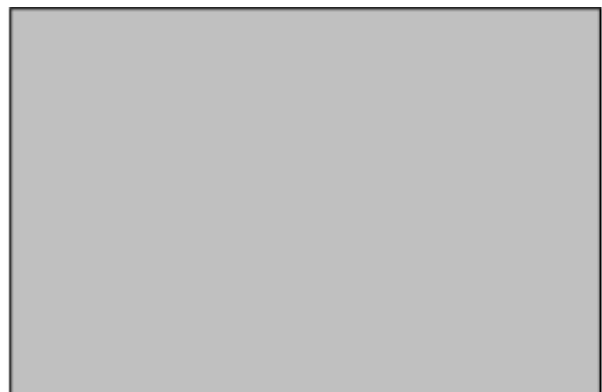
Note 1: LCD glass and metal bezel

Note 2: IF connector pins

Note 3: Operation with test pattern sustained for 4hrs, then change to gray pattern immediately.



(a) Test Pattern (chess board Pattern)



(b) Gray Pattern

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8.0 OUTLINE DIMENSION

1	2	3	4	5	6	7	8
Date: (日期) 2016/11/19 (页数) 1/1 图纸视角:			DESIGN: (设计) DSR CHECKED: (检查) APPROVED: (核准)		SPECIFICATION FOR LCM CUSTOMER'S CODE: (客户型号) LOVE MODEL NO.: (乐源型号) WTIMV70E-01		LCM 规格 EDITION: (版本号) A1

NOTES:

1. DISPLAY TYPE: 6.95" TFT LCD
2. DISPLAY MODE: Normally Black
3. VIEWING DIRECTION : IPS
4. DRIVER: JD9365+JD5001
5. LCM (White 9AVG 1/6)
 Brightness: 220cd/m²(MIN), 250cd/m²(TYP)
 Chromaticity: X=0.30±0.04, Y=0.33±0.04
 Uniformity: 75% (MIN)
6. Backlight: 18 chip white LEDs
 If=20mA*4, Vf=19.5V (TYP)
7. OPERATING TEMP: -20° C TO 70° C,
 STORAGE TEMP: -30° C TO 80° C
8. *Critical parameter, unspecified Tolerances: ±0.20mm
9. SUGGESTION: TP window size unilateral increase 0.3~0.5mm than LCM A.A

DETAIL A 4:1

6*3=18EA, 20mA*3=60mA
 B/L LED CIRCUIT DIAGRAM

NO.	DEFIND
1	TFT
2	GND
3	LOWCL.8
4	NC
5	GND
6	MPI N2
7	MPI P2
8	GND
9	MPI P0
10	MPI NO
11	GND
12	MPI PT
13	MPI NI
14	GND
15	MPI TCN
16	MPI TCP
17	GND
18	MPI F3
19	MPI N3
20	GND
21	RS:ST
22	NC
23	NC
24	GND
25	NC
26	VDD3.3V
27	NC
28	NC
29	LED K
30	LED K
31	LED A
32	LED A
33	GND

check by: 确认

Approved by: 承认

Please Confirm This Drawing On/Before 请签回此图

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9.0 CHECK LIST(品质标准)

检验项目	判定标准	检验方法	缺陷类别
点缺陷	a. 彩点: D>0.3MM, 不允许有; D≤0.2MM: A区: N≤1; B区: N≤5, 且DS≥10mm b. 白点不允许有; c. 黑点: D≤0.2mm, N≤2, d. 彩点, 黑点的总数N≤5, 且DS ≥10mm e. 荧光点(花点)满天星: 不允许有	用测试治具按图纸要求点亮产品, 以30CM距离, 45度角度对产品发光区进行目视检验。	MAJ
最大亮度	以规格书和图面实际要求为准	参考LCD屏规格书, 将机器屏幕亮度设到最大, 播放100%白图片, 用色彩分析仪测量屏幕中心点亮度值。	MAJ
亮度均匀性	≥75%	参考LCD规格书, 将机器屏幕亮度设置到最大, 播放100白图片, 用色彩分析仪测试下图1 P0-P8的亮度值, 分别计为L0-L8, 按照公式计算亮度的均匀性 $P_i = L_i / L_0 * 100\%$ (i未1-8中的亮度值的最小), 9.7寸及以下只测试P0, P5-P8五点, 测量的亮度均匀性应与规格书相符, 同时可接受的整机最大屏幕对比度应不低于75%	MAJ
屏幕边缘漏光	不允许	整机平放在平整的桌面上, 以后以45度的角度查看TFT屏的四周, 不可以出现有光从铁框边缘露出现象。	MAJ
划痕	无深度的细划痕: L≤2MM,W≤0.1MM,N≤1, 有深度的划痕感不允许。	目视	MIN
功能性缺陷	LCD出现功能性缺陷(白屏、闪屏、花屏, 线条等显示异常缺陷, 不允许。	试装测试。	MAJ
按压白点	不允许。	使用200G的力度在背光背后平整按压。	MIN

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可视角度	水平方向 \geq 规格书标明角度。	参考LCD屏规格书，依旧检验角度检验方法，肉眼观察水平左右方向的可视角度不小于LCD规格书标明的角度。	MAJ
	垂直方向 \geq 规格书标明角度。	参考LCD屏规格书，依旧检验角度检验方法，肉眼观察垂直上下方向的可视角度不小于LCD规格书标明的角度。	MAJ
高低温存储	检查屏不能出现屏闪、线条、花屏、背光折皱、白印等结构及功能问题。	1. 将样品竖直平行放置在试验箱的样品架上，环境温度 $+60^{\circ}\text{C} \pm 2^{\circ}\text{C}$ ，放置 12 小时后再常温下恢复 2 小时。 2. 将样品竖直平行于出口风口放置在试验箱的样品架上，环境温度 $-10 \pm 2^{\circ}\text{C}$ 放置 12 小时后再常温下恢复 2 小时。	MAJ
高温工作		1. 将样品竖直平行放置在试验箱的样品架上，使样品处于循环的工作状态。 2. 试验设备温度 $45^{\circ}\text{C} \pm 2^{\circ}\text{C}$ ，在此温度环境下运行 24 小时。	MAJ
低温工作		1. 样品竖直平行放置在试验箱的样品架上，使样品处于循环工作状态。 3. 试验设备温度 $-10^{\circ}\text{C} \pm 2^{\circ}\text{C}$ ，在此温度环境下运行 24 小时	MAJ

1.点亮外观:

检验项目	条件	规格	备注
亮点、黑点、污点	动作试验	$0.3 < D$: 不可有 $0.25 < D \leq 0.3$: 1EA OK $0.2 \leq D \leq 0.25$: 2EA OK; $D < 0.2$: 不计	1. 点距 20mm 2. 盖上 LCD 仍能明显看见判 NG
亮线、刮伤、异物	动作试验	$0.03 < W$: 不可有 ; $3.0 < L$: 不可有 $L \leq 2.0$ $0.02 < W \leq 0.03$: 2EA OK $L \leq 3.0$ $0.01 < W \leq 0.02$: 3EA OK $W \leq 0.01$: 不计 点灯时发光面上不可有亮线等明暗	
MURA	动作试验	现象, 如果出现时, 盖上 LCD 不可看见	

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牛顿环	动作试验	盖上 LCD 不可看见	
2.非点亮外观: 项目重缺点轻缺点判定基准			
2.1 包装箱	2.1.1	不可有破裂	
	2.1.2	若有特殊记号必须检附相关证明档	
2.2 产品标签	2.2.1	内容必须正确	
	2.2.2	字体清晰	
	2.2.3	贴附位置必须正确	
	2.2.4	不可短缺或误配	
	2.2.5	不可重叠贴附	
2.3 线材	2.3.1.	不可有裸线或断线	
	2.3.2.	长度、线径、颜色必须正确, 不可刺伤、压伤或破损	
	2.3.3.	热缩套管不可破损	
	2.3.4.	不可有组装不良现象	
	2.3.5.	A.K 不可反接,(A 为正极,K 为负极)	

10.0 LOT MARK

10.1 Location of Lot Mark

- (1) Location: The label is attached to the backside of the LCD module.
- (2) Detail of the Mark: as attached below.
- (3) This is subject to change without prior notice.

WTI W70E- 01

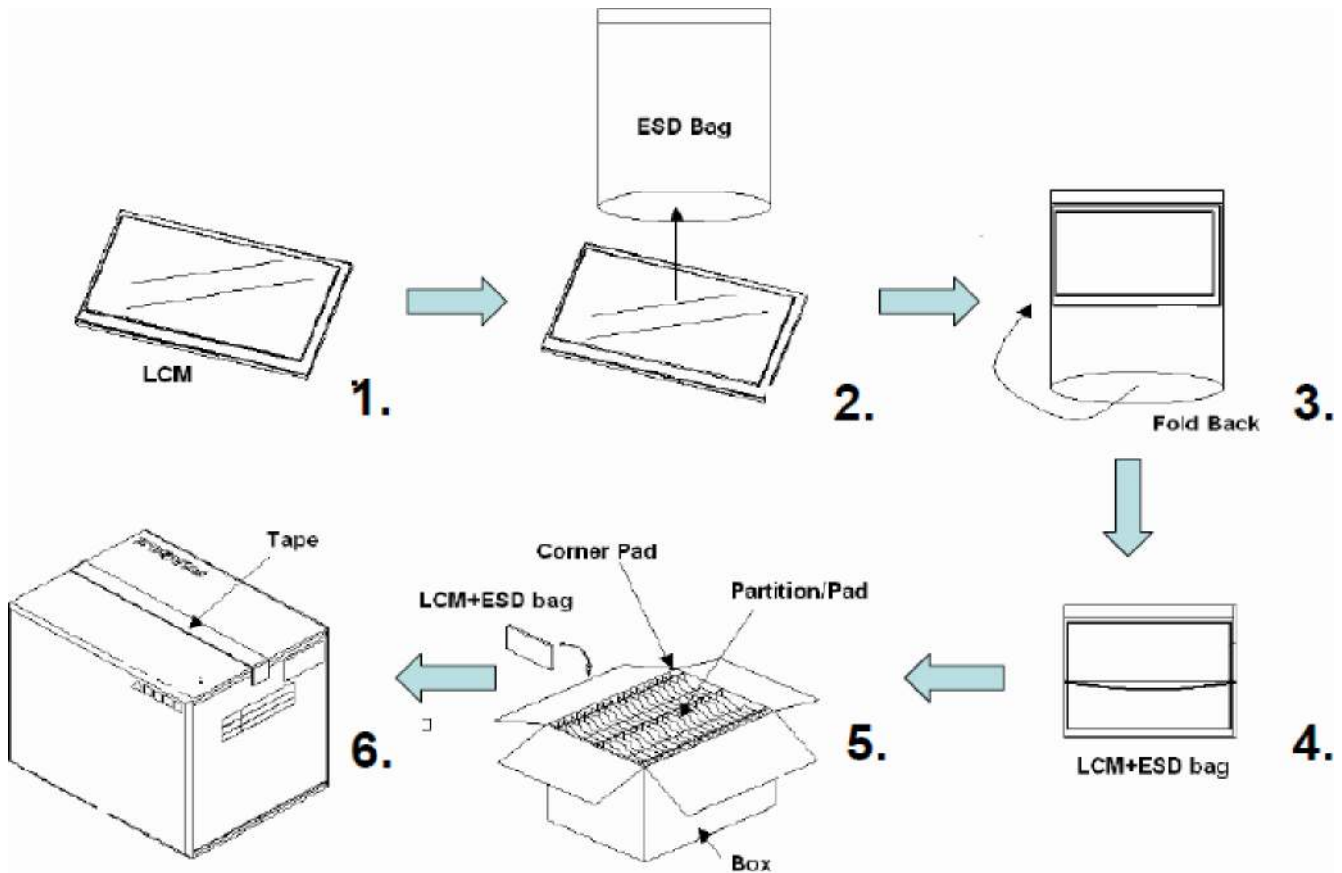
11.0 PACKAGE SPECIFICATION

11.1 Packing form

LCM Model	LCM Qty. in the box	Inner Box Size (mm)	Note
WTI W70E- 01	80 pcs/box	460±5 x 360±5 x 175±5	

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11.2 Packing assembly drawings



Items	Material	Notice
Box	Corrugated Paper Board	AB Flute
Partition/Pad	Corrugated Paper Board	B Flute
Corner Pad	Corrugated Paper Board	AB Flute
ESD bag	PE	

12.0 GENERAL PRECAUTION

12.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

12.2 Assembly Precaution

12.2.1 Please use the mounting hole on the module side in installing and do not bending or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.

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- 12.2.2. Please design display housing in accordance with the following guide lines.
- 12.2.2.1 Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.
 - 12.2.2.2 Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. The clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.
 - 12.2.3 Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands.(Polarizer film, surface of LCD panel is easy to be flawed.)
 - 12.2.4 Please do not press any parts on the rear side such as source IC, gate IC, and FPC during handling LCD module, If pressing rear part is unavoidable, handle the LCD module with care not to damage them.
 - 12.2.5 Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.
 - 12.2.6 Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.
 - 12.2.7 Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.

12.3 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. Century does not warrant the module, if customers disassemble or modify the module.

12.4 Breakage of LCD Panel

- 12.4.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.
- 12.4.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.
- 12.4.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.
- 12.4.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

12.5 Absolute Maximum Ratings and Power Protection Circuit

- 12.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.
- 12.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
- 12.5.3. It's recommended to employ protection circuit for power supply.

12.6 Operation

- 12.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

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- 12.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.
- 12.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.
- 12.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.
- 12.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

12.7 Static Electricity

- 12.7.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.
- 12.7.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge.
- 12.7.3 Persons who handle the module should be grounded through adequate methods.

12.8 Disposal

When disposing LCD module, obey the local environmental regulations.

12.9 Others

- 12.9.1 A strong incident light into LCD panel might cause display characteristics' changing inferior because of Polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land Strong UV rays.
- 12.9.2 Please pay attention to a panel side of LCD module not to contact with other materials in pressing it alone.
- 12.9.3 For the packaging box, please pay attention to the followings:
 - 12.9.3.1 Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.
 - 12.9.3.2 Please do not pile them up more than 6 boxes(They are not designed so) And please do not turn over.
 - 12.9.3.3 Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
 - 12.9.3.4 Packing box and inner case for LCDs are made of cardboard, So please pay attention not to get them wet(Such like keeping them in high humidity or wet place can occur getting them wet.)