

N-channel 30 V 13.6 m Ω logic level MOSFET in LFPAK using NextPower technology

Rev. 3 — 24 October 2011

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

1.3 Applications

Quick reference data

Table 1.

- DC-to-DC converters
- Load switching

Synchronous buck regulator

1.4 Quick reference data

Min -	Тур	Max	Unit
-			5
	-	30	V
-	-	32	А
-	-	26	W
-55	-	175	°C
-	14.4	16.9	mΩ
-	11.6	13.6	mΩ
-	1.2	-	nC
-	4	-	nC
	- -55 - - - -	- 14.4 - 11.6 - 1.2	26 -55 - 175 - 14.4 16.9 - 11.6 13.6 - 1.2 -

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Pinning information 2.

Table 2.	Pinning	j information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		5
2	S	source	mb	
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	$\begin{array}{c} \begin{array}{c} \\ \end{array} \\ 1 \end{array} \begin{array}{c} 2 \end{array} \begin{array}{c} 3 \end{array} \begin{array}{c} 4 \end{array}$	mbb076 S

SOT669 (LFPAK; Power-SO8)

Ordering information 3.

Table 3. Ordering information						
Type number	Package					
	Name	Description	Version			
PSMN013-30YLC	LFPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669			

Limiting values 4.

Table 4. **Limiting values**

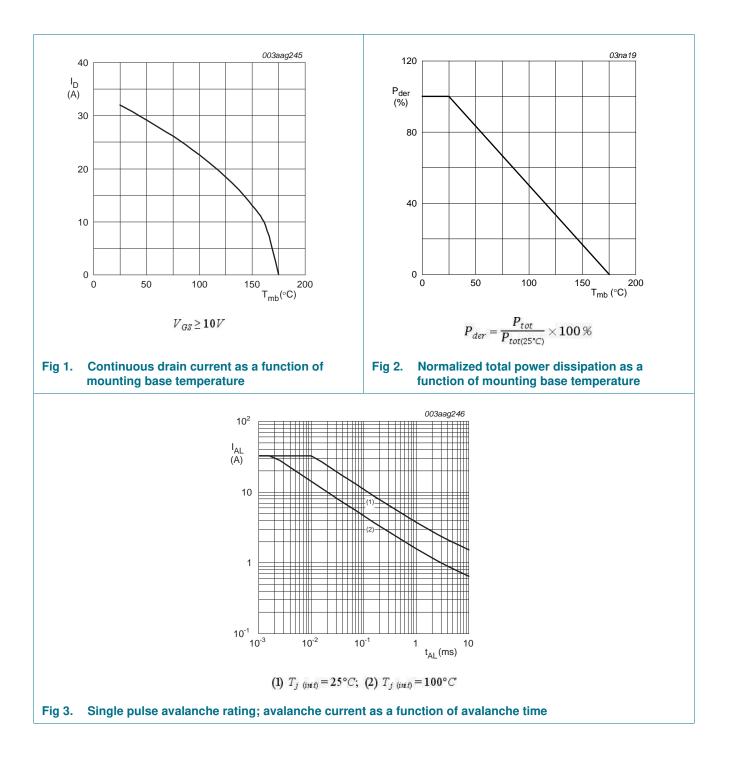
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	30	V
V _{DGR}	drain-gate voltage	25 °C \leq T _j \leq 175 °C; R _{GS} = 20 kΩ	-	30	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; see <u>Figure 1</u>	-	32	А
		V_{GS} = 10 V; T_{mb} = 100 °C; see <u>Figure 1</u>	-	23	А
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see <u>Figure 4</u>	-	130	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	26	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	130	-	V
Source-drai	n diode				
I _S	source current	T _{mb} = 25 °C	-	23	А
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	130	А
Avalanche r	ruggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$ \begin{array}{l} V_{GS} = 10 \text{ V}; \text{T}_{j(init)} = 25 \text{ °C}; \text{I}_\text{D} = 32 \text{ A}; \\ V_{sup} \leq 30 \text{ V}; \text{R}_{GS} = 50 \Omega; \text{ unclamped}; \\ \text{see } \underline{\text{Figure } 3} \end{array} $	-	7	mJ

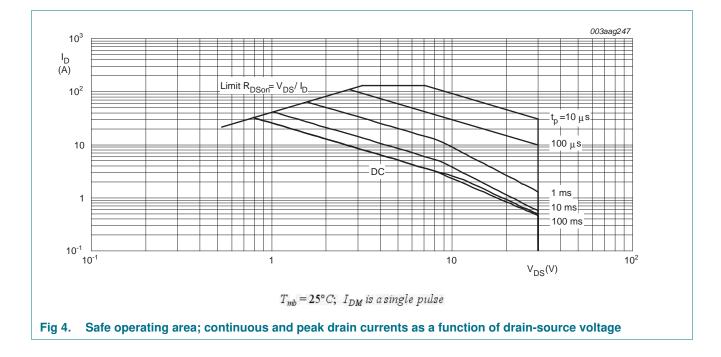
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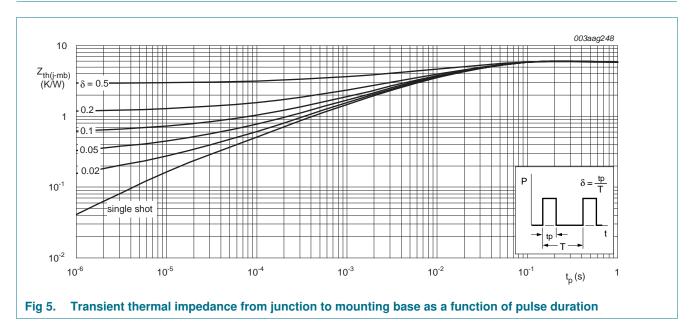
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5. Thermal characteristics

Table 5.	Thermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	see Figure 5	-	5.66	5.83	K/W



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6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V _{(BR)DSS} drain-source breakdown		$I_D = 250 \ \mu A; V_{GS} = 0 \ V; T_j = 25 \ ^{\circ}C$	30	-	-	V
	voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ see <u>Figure 10</u> ; see <u>Figure 11</u>	1.05	1.68	1.95	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ °C}$	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = -55 °C	-	-	2.25	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μA
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	100	μA
I _{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I _D = 10 A; T _j = 25 °C; see <u>Figure 12</u>	-	14.4	16.9	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 150 °C; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	-	27.2	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; see <u>Figure 12</u>	-	11.6	13.6	mΩ
	V_{GS} = 10 V; I_D = 10 A; T_j = 150 °C; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	-	22.1	mΩ	
R _G	gate resistance	f = 1 MHz	-	2.12	4.24	Ω
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see <u>Figure 14</u> ; see <u>Figure 15</u>	-	8.3	-	nC
		$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 14; see Figure 15	-	4	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	7.7	-	nC
Q _{GS}	gate-source charge	$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	1.3	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	see <u>Figure 14</u> ; see <u>Figure 15</u>	-	0.9	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	0.4	-	nC
Q _{GD}	gate-drain charge		-	1.2	-	nC
V _{GS(pl)}	gate-source plateau voltage	$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V}; \text{ see } \frac{\text{Figure } 14}{\text{Figure } 15}$	-	2.7	-	V
C _{iss}	input capacitance	$V_{DS} = 15 \text{ V}; \text{ V}_{GS} = 0 \text{ V}; \text{ f} = 1 \text{ MHz};$	-	521	-	pF
C _{oss}	output capacitance	$T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 16}{16}$	-	128	-	pF
C _{rss}	reverse transfer capacitance		-	39	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = 15 V; R_L = 0.6 Ω; V_{GS} = 4.5 V;	-	11.6	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \ \Omega$	-	9.9	-	ns
t _{d(off)}	turn-off delay time		-	16.3	-	ns
t _f	fall time		-	6.2	-	ns

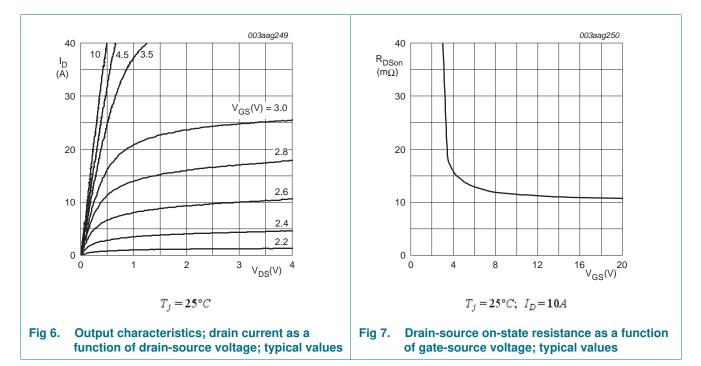
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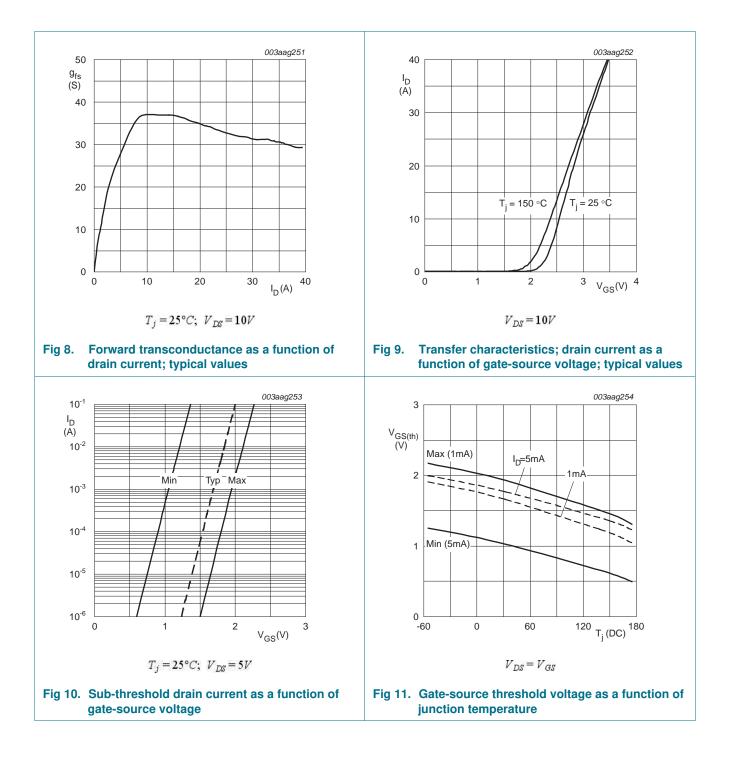
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Table 6. Characteristics ...continued

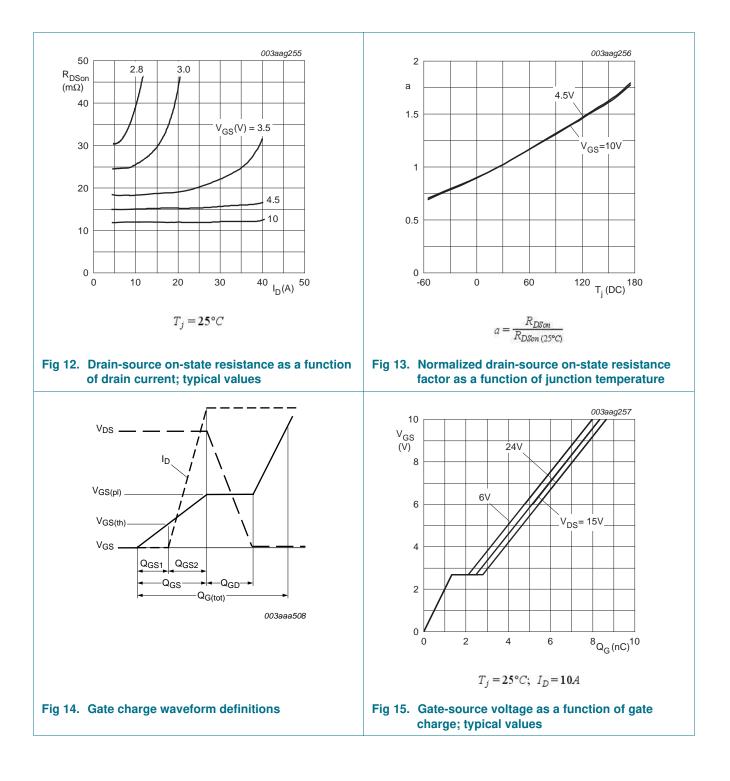
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Q _{oss}	output charge	$\label{eq:VGS} \begin{array}{l} V_{GS} = 0 \ V; \ V_{DS} = 15 \ V; \ f = 1 \ MHz; \\ T_j = 25 \ ^\circ C \end{array}$	-	3.3	-	nC
Source-dra	in diode					
V_{SD}	source-drain voltage	I _S = 10 A; V _{GS} = 0 V; T _j = 25 °C; see <u>Figure 17</u>	-	0.86	1.1	V
t _{rr}	reverse recovery time	$I_{S} = 10 \text{ A}; \text{ d}I_{S}/\text{d}t = -100 \text{ A}/\mu\text{s};$	-	16	-	ns
Q _r	recovered charge	$V_{GS} = 0 V; V_{DS} = 15 V$	-	6	-	nC
t _a	reverse recovery rise time	$V_{GS} = 0 V; I_S = 10 A;$	-	9.5	-	ns
t _b	reverse recovery fall time	$dI_S/dt = -100 A/\mu s; V_{DS} = 15 V;$ see Figure 18	-	6.5	-	ns



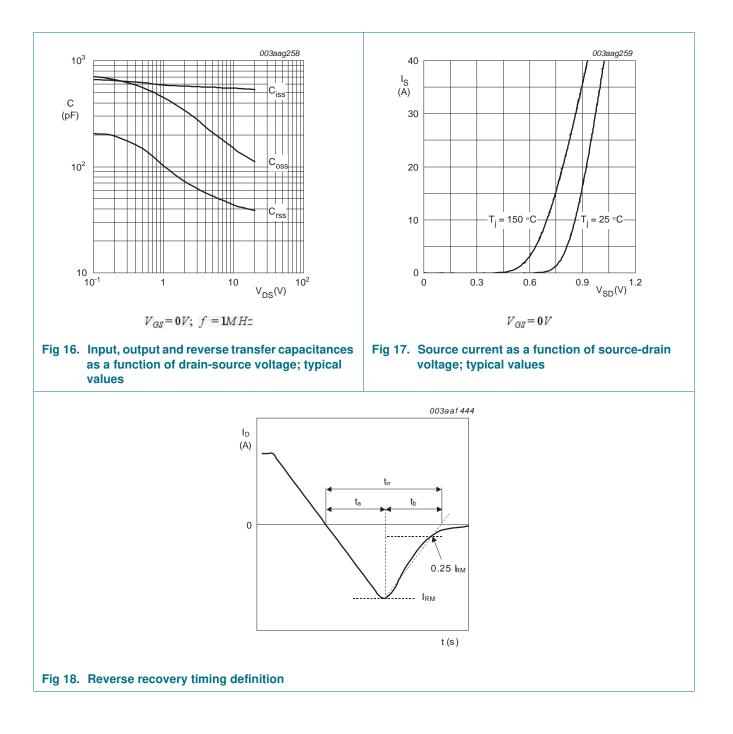
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7. Package outline

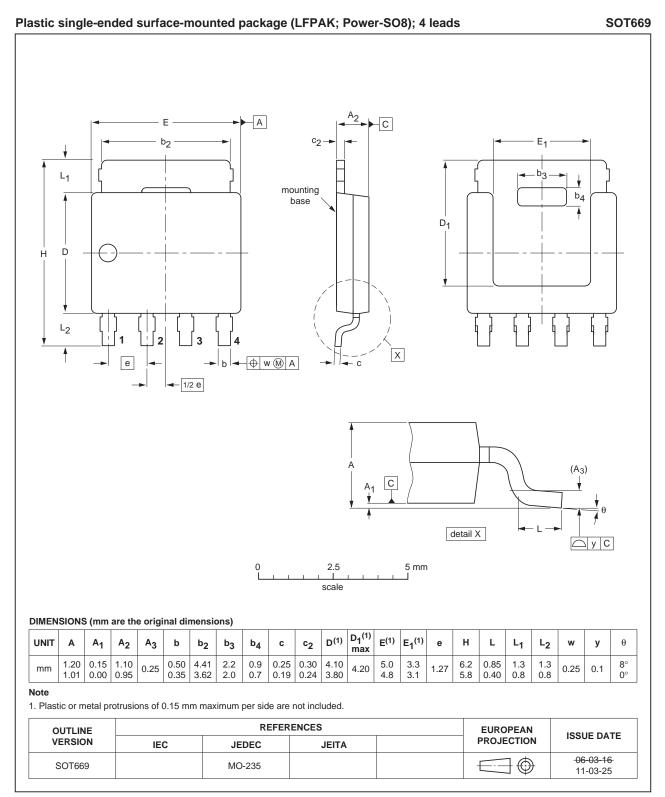


Fig 19. Package outline SOT669 (LFPAK; Power-SO8)

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PSMN013-30YLC

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8. Revision history

Table 7. Revision h	istory			
Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN013-30YLC v.3	20111024	Product data sheet	-	PSMN013-30YLC v.2
Modifications:	 Status change 	ed from preliminary to produc	xt.	
	 Various chang 	jes to content.		
PSMN013-30YLC v.2	20110929	Preliminary data shee	t -	PSMN013-30YLC v.1

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9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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