TPS7A15 400-mA, Low V_{IN}, Low V_{OUT}, Ultra-Low Dropout Regulator

1 Features

- Ultra-low input voltage range: 0.7 V to 2.2 V
- High efficiency:
  - Dropout at 400 mA: 80 mV (max)
  - Specified for $V_{IN} = V_{OUT} + 100$ mV
- Excellent load transient response:
  - 20 mV for I_{LOAD} 1 mA to 250 mA in 10 µs
- Accuracy (load, line, temperature): +1%, –1.1%
- High PSRR: 84 dB at 1 kHz
- Available in fixed-output voltages:
  - 0.5 V to 2.0 V (in 25-mV steps)
- V_{BIAS} range:
  - 2.2 V to 5.5 V
- Packages:
  - 6-pin, 1-mm × 0.71-mm DSBGA
  - 6-pin, 2-mm × 2-mm WSON (preview)
- Active output discharge

2 Applications

- Camera modules
- Wireless headphones and earbuds
- Smart watches, fitness trackers
- Smart phones and tablets
- Portable medical devices
- Solid state drives (SSDs)

3 Description

The TPS7A15 is a small, low-dropout regulator (LDO) with excellent transient response. This device can source 400 mA with outstanding ac performance (load and line transient responses). The input voltage range is from 0.7 V to 2.2 V, and the output range is from 0.5 V to 2.0 V with a very high accuracy of 1% over load, line, and temperature.

The primary power path is through the IN pin and can be connected to a power supply as low as 50 mV above the output voltage. All electrical characteristics (including excellent output voltage tolerance, transient response, and PSRR) are specified for input voltages 100 mV greater than the output voltage, thereby yielding high practical efficiency. This regulator supports very low input voltages by using a higher, externally supplied V_{BIAS} rail that powers the internal circuitry of the LDO. For example, the supply voltage to the IN pin can be the output of a high-efficiency, DC/DC step-down regulator and the BIAS pin supply voltage can be a rechargeable battery.

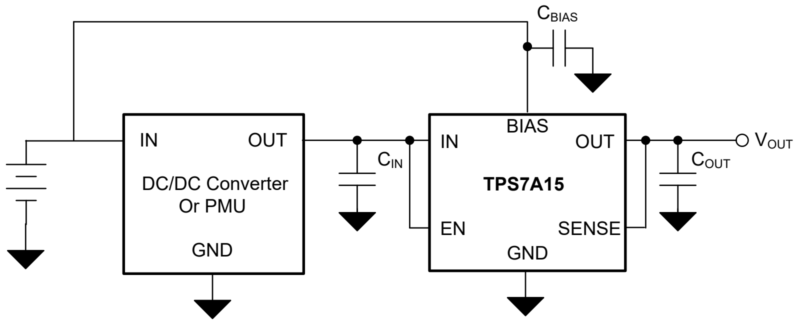
The TPS7A15 is equipped with an active pulldown circuit to quickly discharge the output when disabled, and provides a known start-up state.

The TPS7A15 is available in a 2-mm × 2-mm, 6-pin WSON package and in an ultra-small 0.71-mm × 1.0-mm, 6-bump WCSP package.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[3]
TPS7A15	YCK (WCSP, 6)	0.71 mm × 1 mm
	DRV (WSON, 6)[2]	2 mm × 2 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview package.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2022) to Revision A (July 2023)	Page
• Added DRV (WSON) package to document as *Advance Information*	1
• Changed fixed output voltage range from *0.5 V to 2.05 V* to *0.5 V to 2.0 V* throughout document	1
• Changed description of packages in last paragraph of *Description* section	1

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5 Pin Configuration and Functions

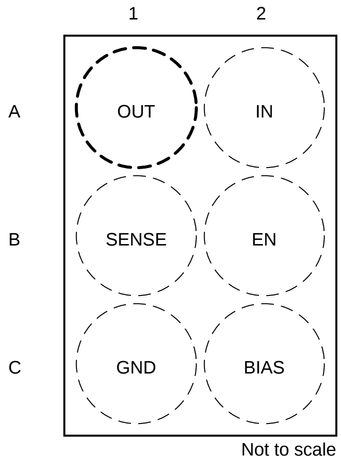

Figure 5-1. YCK Package, 6-Pin WCSP, 0.35-mm Pitch (Top View)

Table 5-1. Pin Functions: YCK Package

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	OUT	Output	Regulated output pin. A 1-μF or greater capacitance is required from OUT to ground for stability. For best transient response, use a 2.2-μF or larger ceramic capacitor from OUT to GND. Place the output capacitor as close to OUT as possible.
A2	IN	Input	Input pin. A 0.75-μF or greater capacitance is required from IN to ground for stability. For good transient response, use a 2.2-μF or larger ceramic capacitor from IN to GND. Place the input capacitor as close to input of the device as possible.
B1	SENSE	Input	SENSE input. This pin is a feedback input to the regulator for SENSE connections. Connecting SENSE to the load helps eliminate voltage errors resulting from trace resistance between OUT and the load.
B2	EN	Input	Enable pin. Driving this pin to logic high enables the low-dropout regulator (LDO). Driving this pin to logic low disables the LDO. If enable functionality is not required, this pin must be connected to IN or BIAS.
C1	GND	—	Ground pin. This pin must be connected to ground.
C2	BIAS	Input	BIAS pin. This pin enables the use of low-input voltage, low-output voltage (LILO) conditions. For best performance, use a 0.1-μF or larger ceramic capacitor from BIAS to GND. Place the bias capacitor as close to BIAS as possible.

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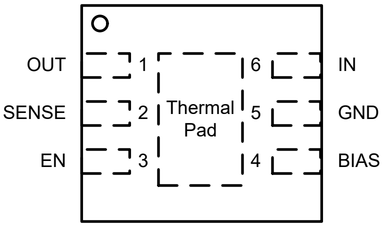

Figure 5-2. DRV Package (Preview), 6-Pin WSON With Exposed Thermal Pad (Top View)

Table 5-2. Pin Functions: DRV Package

PIN		TYPE	DESCRIPTION
NO.	NAME		
4	BIAS	Input	BIAS pin. This pin enables the use of LILO conditions. For best performance, use a 0.1-μF or larger ceramic capacitor from BIAS to GND. Place the bias capacitor as close to BIAS as possible.
3	EN	Input	Enable pin. Driving this pin to logic high enables the LDO. Driving this pin to logic low disables the LDO. If enable functionality is not required, this pin must be connected to IN or BIAS.
5	GND	—	Ground pin. This pin must be connected to ground.
6	IN	Input	Input pin. A 0.75-μF or greater capacitance is required from IN to ground for stability. For good transient response, use a 2.2-μF or larger ceramic capacitor from IN to GND. Place the input capacitor as close to input of the device as possible.
1	OUT	Output	Regulated output pin. A 1-μF or greater capacitance is required from OUT to ground for stability. For best transient response, use a 2.2-μF or larger ceramic capacitor from OUT to GND. Place the output capacitor as close to OUT as possible.
2	SENSE	Input	SENSE input. This pin is a feedback input to the regulator for SENSE connections. Connecting SENSE to the load helps eliminate voltage errors resulting from trace resistance between OUT and the load.
Thermal Pad		—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	2.4	V
	Enable, V_{EN}	–0.3	6.0	
	Bias, V_{BIAS}	–0.3	6.0	
	Sense, V_{SENSE}	–0.3	V_{IN} + 0.3 (2)	
	Output, V_{OUT}	–0.3	V_{IN} + 0.3 (2)	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The absolute maximum rating is 2.4 V or (V_{IN} + 0.3 V), whichever is less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted). (1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0.7		2.2	V
V_{BIAS}	Bias voltage	Greater of 2.2 or V_{OUT} + 1.4		5.5	V
V_{OUT}	Output voltage	0.5		2.0	V
I_{OUT}	Peak output current	0		400	mA
C_{IN}	Input capacitance(2)	0.75			µF
C_{BIAS}	Bias capacitance(3)		0.1		µF
C_{OUT}	Output capacitance, DRV package	1		22	µF
C_{OUT}	Output capacitance, YCK package	1		47	µF
ESR	Output capacitor series resistance			100	mΩ
T_J	Operating junction temperature	–40		125	℃

(1) All voltages are with respect to GND.

(2) An input capacitor is required to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients. A larger input capacitor may be necessary depending on the source impedance and system requirements.

(3) A BIAS input capacitor is not required for LDO stability. However, a capacitor with a derated value of at least 0.1 µF is recommended to maintain transient, PSRR, and noise performance.

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6.4 Thermal Information

THERMAL METRIC(1)		TPS7A15		UNIT
		DRV (WSON)	YCK (DSBGA)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	75.7	148.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.1	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.0	42.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.0	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.0	42.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	19.7	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) For information about how to improve junction-to-ambient thermal resistance, see the *An empirical analysis of the impact of board layout on LDO thermal performance* application note.

6.5 Electrical Characteristics

specified at T_J = –40°C to +125°C, $V_{IN} = V_{OUT(NOM)} + 0.1$ V, V_{BIAS} = greater of 2.2 V or $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, and C_{BIAS} = 0.1 µF, unless otherwise noted; all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Accuracy over temperature	$V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ 2.2 V, greater of 2.2 V or $V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 1 mA ≤ I_{OUT} ≤ 400 mA	T_J = –40°C to +85°C	–1.1		1	%
			T_J = –40°C to +125°C	–2.5		1	
$\Delta V_{OUT} / \Delta V_{IN}$	V_{IN} line regulation	$V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ 2.2 V		–2.5	0.013	2.5	mV
$\Delta V_{OUT} / \Delta V_{BIAS}$	V_{BIAS} line regulation	$V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V		–2.5	0.02	2.5	mV
$\Delta V_{OUT} / \Delta I_{OUT}$	Load regulation	1 mA ≤ I_{OUT} ≤ 400 mA			0.49		%/A
$I_{Q(BIAS)}$	Bias pin current	I_{OUT} = 0 mA	T_J = –40°C to +85°C			30	µA
			T_J = –40°C to +125°C			41	
		I_{OUT} = 400 mA	T_J = –40°C to +125°C			6.5	mA
$I_{Q(IN)}$	Input pin current(1)	I_{OUT} = 0 mA	T_J = –40°C to +85°C			5.7	µA
			T_J = –40°C to +125°C			17	
I_{GND}	Ground pin current(1)	I_{OUT} = 400 mA			320	500	µA
$I_{SHDN(BIAS)}$	V_{BIAS} shutdown current	V_{IN} = 2.2 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.2 V			0.264	12	µA
$I_{SHDN(IN)}$	V_{IN} shutdown current	V_{IN} = 1.8 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.2 V, T_J = –40°C to +85°C			0.5	5.7	µA
		V_{IN} = 1.8 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.2 V			0.5	22	
I_{CL}	Output current limit	V_{OUT} = 0.95 × $V_{OUT(NOM)}$		450	800	1100	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V			270		mA
$V_{DO(IN)}$	V_{IN} dropout voltage(2)	V_{IN} = 0.95 × $V_{OUT(nom)}$, I_{OUT} = 400 mA, V_{OUT} ≥ 0.6 V, DRV package	V_{IN} = 0.95 × $V_{OUT(nom)}$, I_{OUT} = 400 mA, V_{OUT} ≥ 0.6 V		31	80	mV
$V_{DO(IN)}$	V_{IN} dropout voltage(2)	V_{IN} = 0.95 × $V_{OUT(nom)}$, I_{OUT} = 400 mA, V_{OUT} ≥ 0.6 V			31	80	mV
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage(2)	V_{BIAS} = greater of 1.7 V or $V_{OUT(nom)}$ + 0.6 V, V_{SENSE} = 0.95 × $V_{OUT(nom)}$, I_{OUT} = 400 mA, DRV package	V_{BIAS} = greater of 1.7 V or $V_{OUT(nom)}$ + 0.6 V, V_{SENSE} = 0.95 × $V_{OUT(nom)}$, I_{OUT} = 400 mA, DRV package			1.075	V
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage(2)	V_{BIAS} = greater of 1.7 V or $V_{OUT(nom)}$ + 0.6 V, V_{SENSE} = 0.95 × $V_{OUT(nom)}$, I_{OUT} = 400 mA				1	V

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6.5 Electrical Characteristics (continued)

specified at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.1 V, V_{BIAS} = greater of 2.2 V or $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, and C_{BIAS} = 0.1 µF, unless otherwise noted; all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} PSRR	V_{IN} power-supply rejection ratio	f = 100 Hz	I_{OUT} = 3 mA		90		dB
			I_{OUT} = 400 mA		71		
		f = 1 kHz	I_{OUT} = 3 mA		84		
			I_{OUT} = 400 mA		73		
		f = 10 kHz	I_{OUT} = 3 mA		70		
			I_{OUT} = 400 mA		58		
		f = 100 kHz	I_{OUT} = 3 mA		53		
			I_{OUT} = 400 mA		40		
		f = 1 MHz	I_{OUT} = 3 mA		65		
			I_{OUT} = 400 mA		23		
		f = 1 MHz, V_{IN} = V_{OUT} + 150 mV	I_{OUT} = 3 mA		65		
			I_{OUT} = 400 mA		40		
V_{BIAS} PSRR	V_{BIAS} power-supply rejection ratio	f = 1 kHz,	I_{OUT} = 400 mA		65		dB
		f = 100 kHz			47		
		f = 1 MHz			26		
V_n	Output voltage noise	Bandwidth = 10 Hz to 100 kHz, V_{OUT} = 0.8 V, I_{OUT} = 400 mA			7.2		μV_{RMS}
$V_{UVLO(BIAS)}$	Bias supply UVLO	V_{BIAS} rising		1.15	1.42	1.7	V
		V_{BIAS} falling		1.0	1.3	1.64	
$V_{UVLO\_HYST(BIAS)}$	Bias supply hysteresis	V_{BIAS} hysteresis			103		mV
$V_{UVLO(IN)}$	Input supply UVLO	V_{IN} rising		584	603	623	mV
		V_{IN} falling		530	552	566	
$V_{UVLO\_HYST(IN)}$	Input supply hysteresis	V_{IN} hysteresis			55		mV
t_{STR}	Start-up time(3)				200		µs
$V_{HI(EN)}$	EN pin logic high voltage			0.6			V
$V_{LO(EN)}$	EN pin logic low voltage					0.25	V
I_{EN}	EN pin current	EN = 5.5 V		–20	10	30	nA
$R_{PULLDOWN}$	Pulldown resistor	V_{IN} = 0.9 V, $V_{OUT(nom)}$ = 0.8 V, V_{BIAS} = 1 V, V_{EN} = 0 V, P version only			36		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature rising			165		°C
		Reset, temperature falling			140		

(1) This current flowing from V_{IN} to GND.
(2) Dropout is not measured for V_{OUT} < 0.6 V. V_{BIAS} must be 2.2 V or greater for specified dropout value.
(3) Startup time = time from EN assertion to 0.95 × $V_{OUT(NOM)}$.

6.6 Switching Characteristics

specified at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.1 V, V_{BIAS} = greater of 2.2 V or $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); all typical values are at T_J = 25°C; all transient numbers are over multiple load and line pulses. 100µs on (high load) / 100µs off (low load)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Line transient(1)	V_{IN} = ($V_{OUT(NOM)}$ + 0.1 V) to 2.1 V	Transition time, t_R = 1 V / µs			1	$\%V_{OUT}$
		V_{IN} = 2.1 V to ($V_{OUT(NOM)}$ + 0.1 V)	Transition time, t_F = 1 V / µs	–1			
ΔV_{OUT}	Load transient(1)	I_{OUT} = 1 mA to 250 mA	Transition time, t_R = 10 µs, t_F = 10 µs, t_{OFF} = 200 µs, t_{ON} = 1 ms, C_{IN} = 2 µF, C_{OUT} = 2 µF	–5			$\%V_{OUT}$
		I_{OUT} = 250 mA to 1 mA				5	

(1) This specification is verified by design.

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6.7 Typical Characteristics

at operating temperature T_J = 25°C, $V_{OUT(NOM)}$ = 0.9 V, V_{IN} = $V_{OUT(NOM)}$ + 0.1 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{OUT} = 1 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)

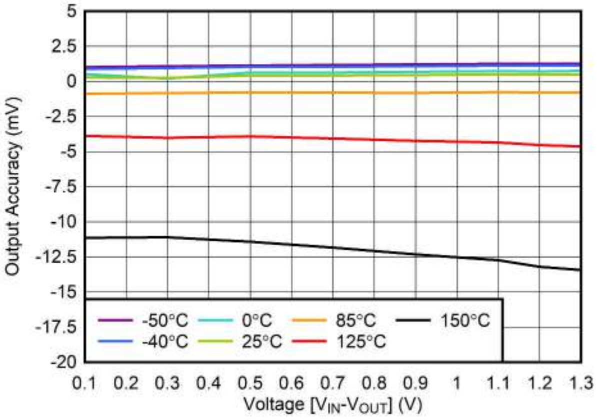

Figure 6-1. Output Voltage Accuracy vs V_{IN}

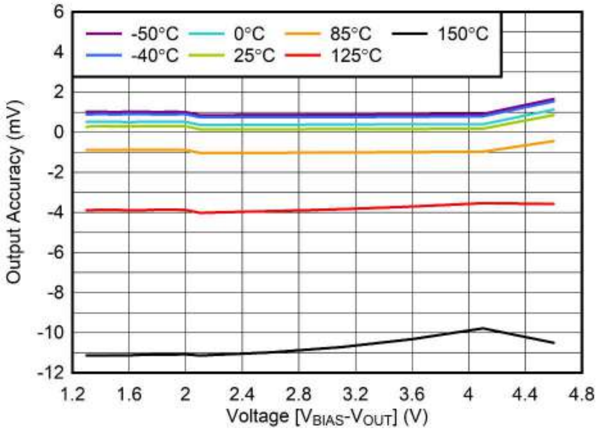

Figure 6-2. Output Voltage Accuracy vs V_{BIAS}

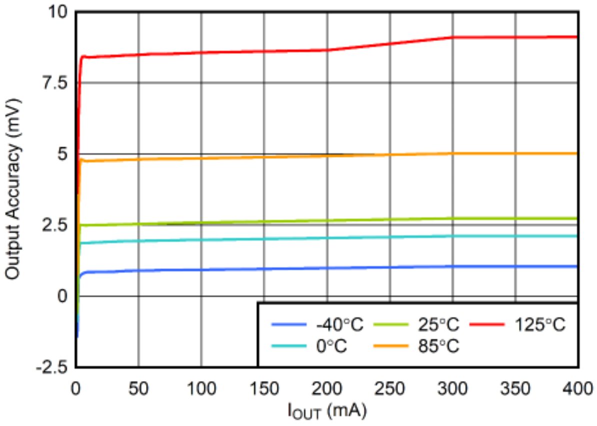

Figure 6-3. Output Voltage Accuracy vs I_{OUT}

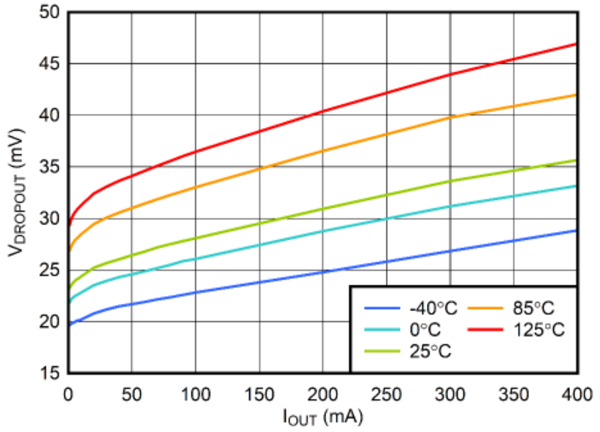

Figure 6-4. V_{IN} Dropout Voltage vs I_{OUT}

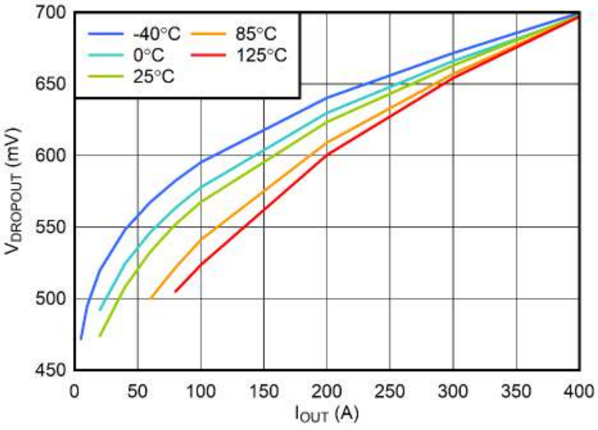

Figure 6-5. V_{BIAS} Dropout Voltage vs I_{OUT}

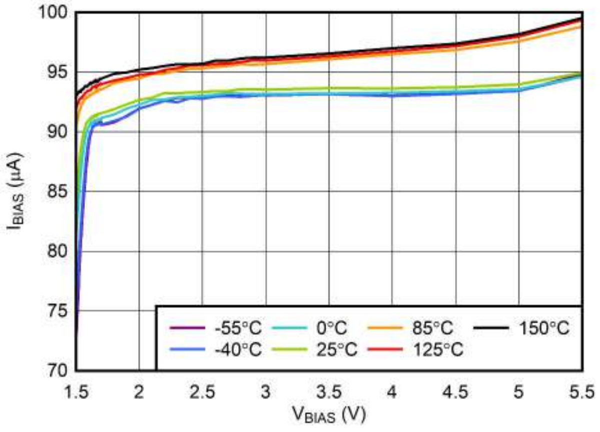

Figure 6-6. V_{BIAS} Input Current vs V_{BIAS}

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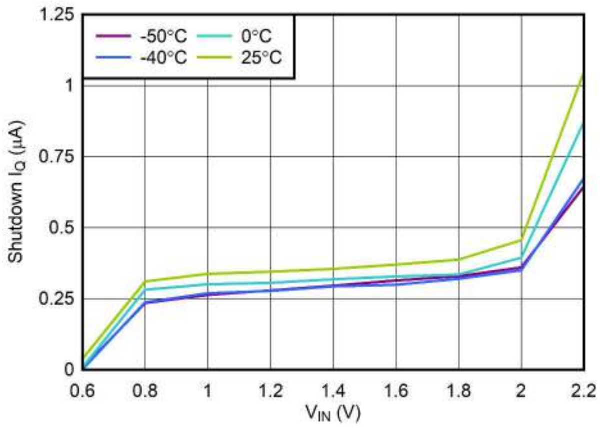
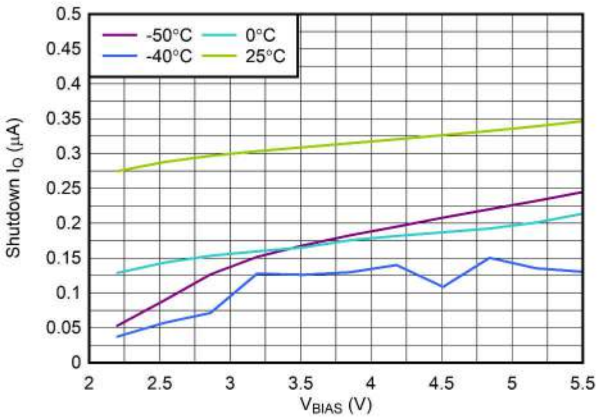
6.7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{OUT(NOM)}$ = 0.9 V, V_{IN} = $V_{OUT(NOM)}$ + 0.1 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{OUT} = 1 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)



I_{OUT} = 0 mA

Figure 6-7. V_{IN} Shutdown I_Q vs V_{IN}



I_{OUT} = 0 mA

Figure 6-8. V_{BIAS} Shutdown I_Q vs V_{BIAS}

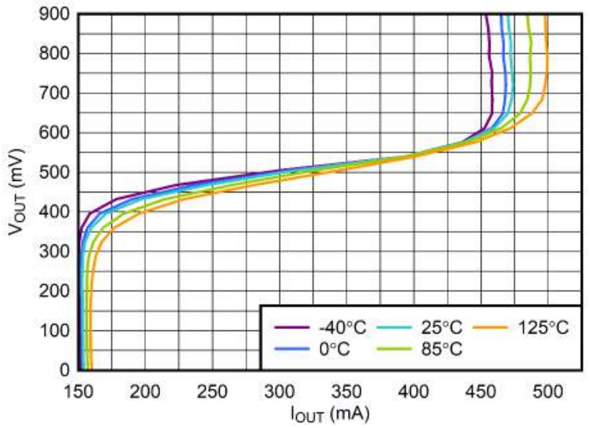


Figure 6-9. Foldback Current Limit vs I_{OUT}

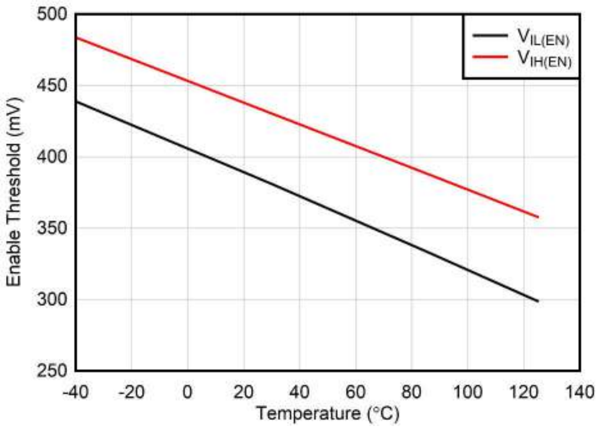


Figure 6-10. Enable Threshold vs Temperature

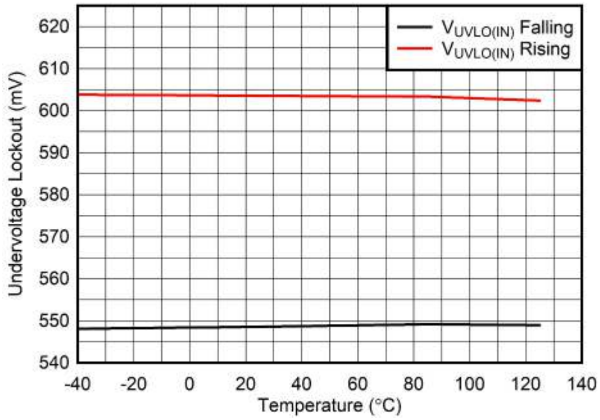


Figure 6-11. V_{IN} UVLO vs Temperature

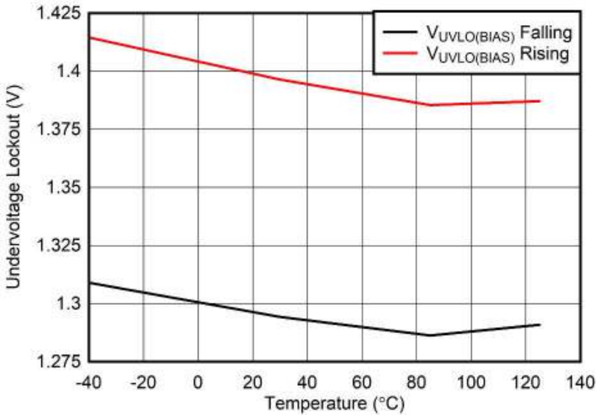


Figure 6-12. V_{BIAS} UVLO vs Temperature

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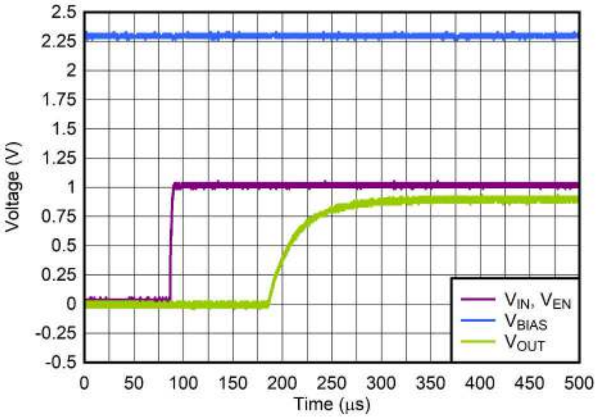
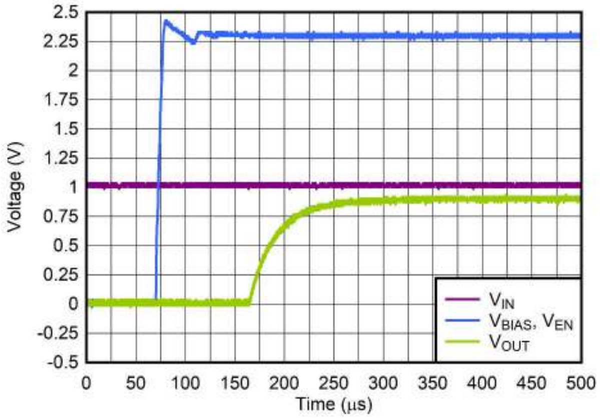
6.7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{OUT(NOM)}$ = 0.9 V, V_{IN} = $V_{OUT(NOM)}$ + 0.1 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{OUT} = 1 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)



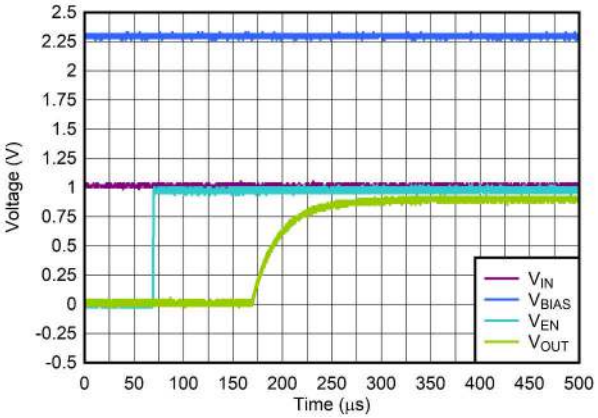
t_r = 1 µs

Figure 6-13. Start-Up With V_{BIAS} Before V_{IN}



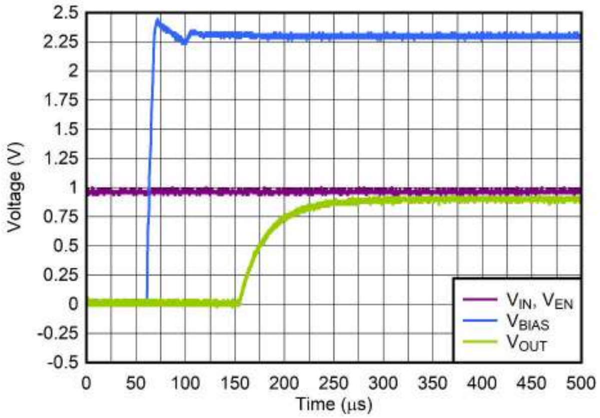
t_r = 1 µs

Figure 6-14. Start-Up With V_{IN} Before V_{BIAS} and V_{EN}



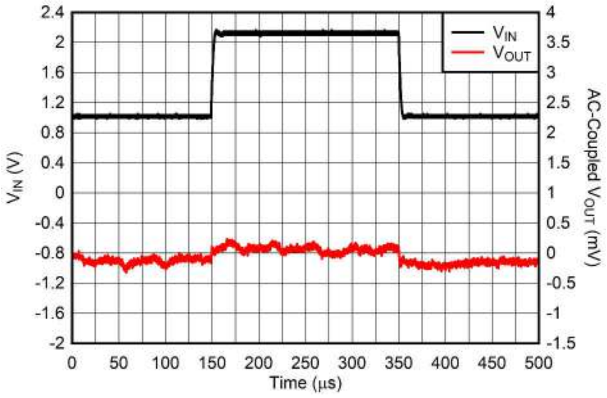
t_r = 1 µs

Figure 6-15. Start-Up With V_{IN} and V_{BIAS} Before V_{EN}



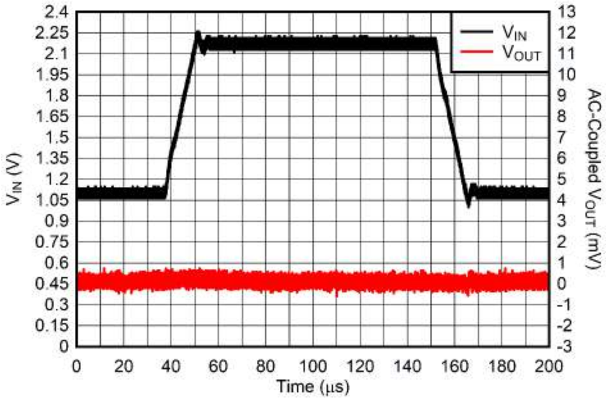
t_r = 1 µs

Figure 6-16. Start-Up With V_{IN} and V_{EN} Before V_{BIAS}



t_r = t_f = 1 µs

Figure 6-17. Line Transient From 1 V to 2.2 V



t_r = t_f = 10 µs, I_{OUT} = 400 mA

Figure 6-18. Line Transient From 1 V to 2.2 V

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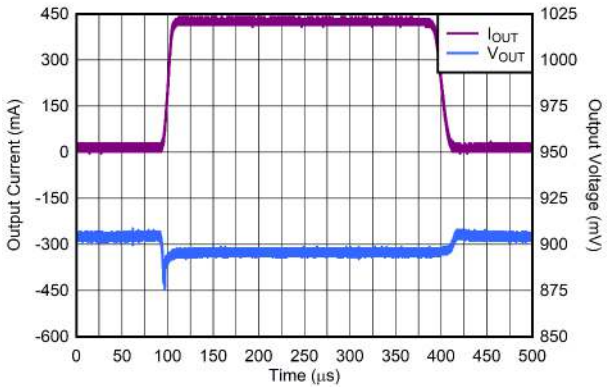
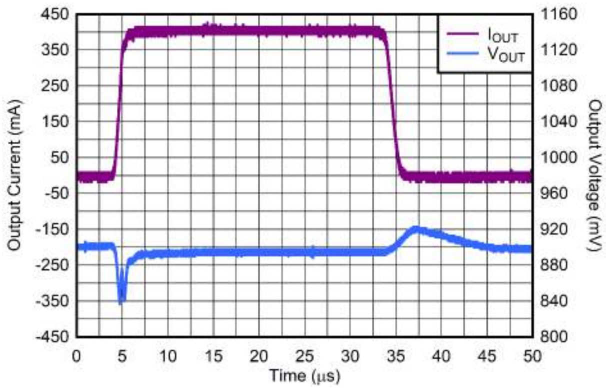
6.7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{OUT(NOM)}$ = 0.9 V, V_{IN} = $V_{OUT(NOM)}$ + 0.1 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{OUT} = 1 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)



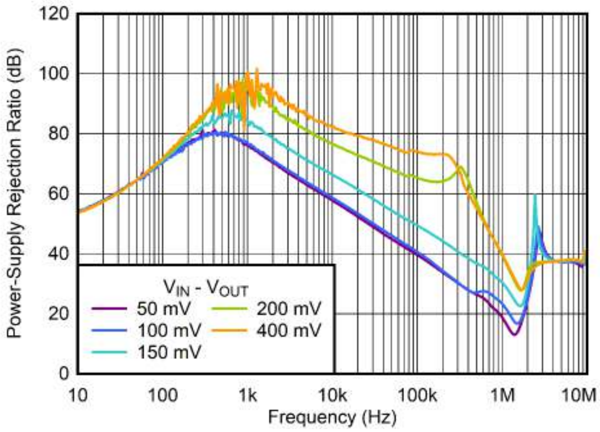
t_r = t_f = 10 µs

Figure 6-19. Load Transient From 100 µA to 400 mA



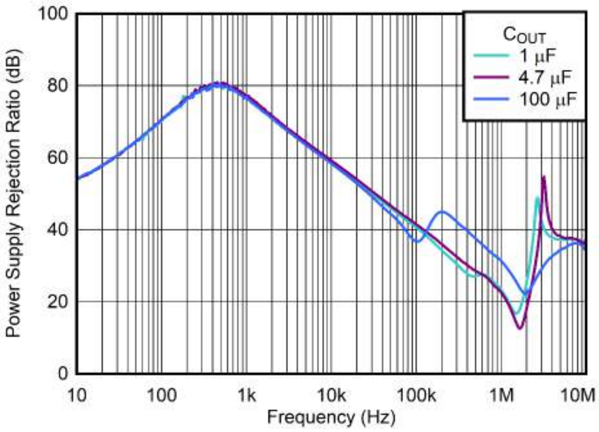
t_r = t_f = 1 µs

Figure 6-20. Load Transient From 100 µA to 400 mA



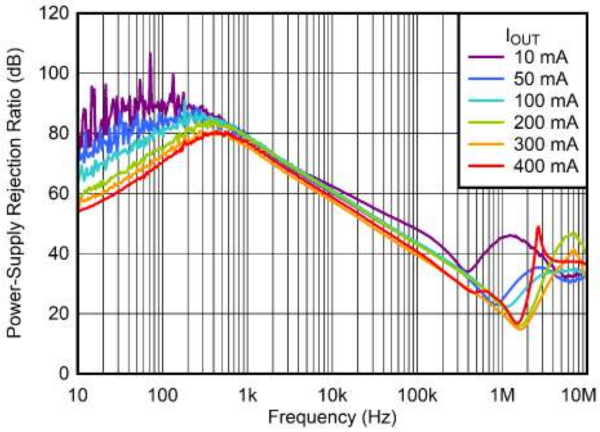
C_{IN} = 0 µF, I_{OUT} = 400 mA

Figure 6-21. V_{IN} PSRR vs Frequency and V_{IN} – V_{OUT}



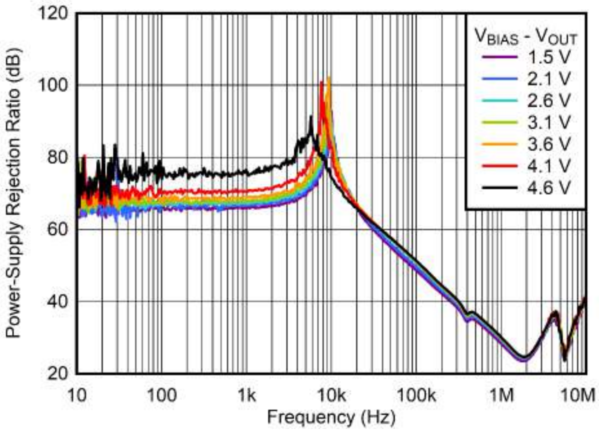
C_{IN} = 0 µF, I_{OUT} = 400 mA

Figure 6-22. V_{IN} PSRR vs Frequency and C_{OUT}



C_{IN} = 0 µF

Figure 6-23. V_{IN} PSRR vs Frequency and I_{OUT}



C_{BIAS} = 0 µF

Figure 6-24. V_{BIAS} PSRR vs Frequency and V_{BIAS} – V_{OUT}

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6.7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{OUT(NOM)}$ = 0.9 V, V_{IN} = $V_{OUT(NOM)}$ + 0.1 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{OUT} = 1 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted)

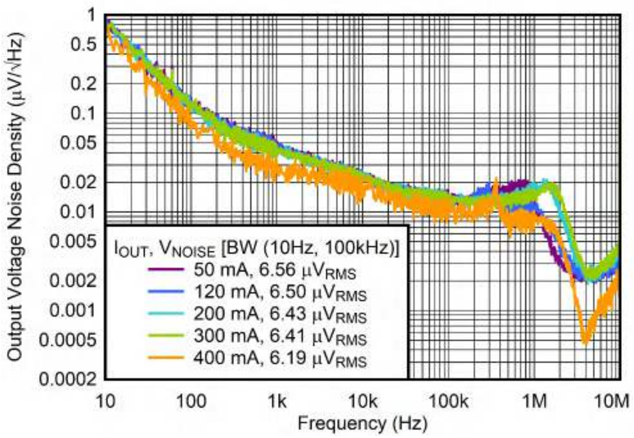


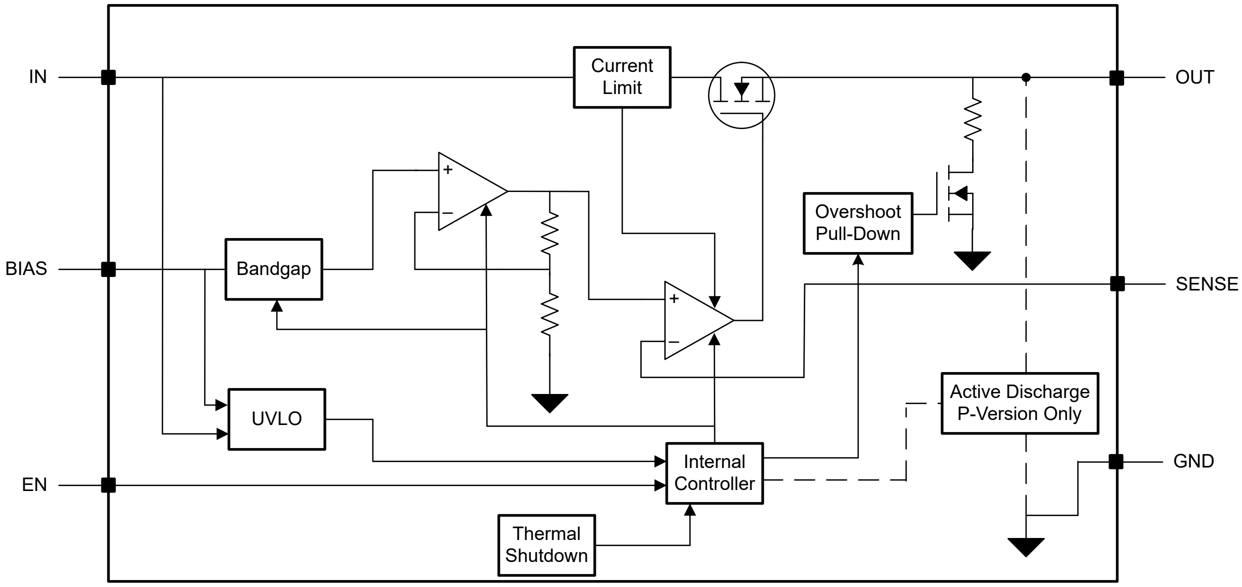
Figure 6-25. Output Noise vs Frequency and I_{OUT}

7 Detailed Description

7.1 Overview

The TPS7A15 is a low-input, ultra-low dropout, low-quiescent-current linear regulator that is optimized for excellent transient performance. These characteristics make the device ideal for most battery-powered applications. The low operating V_{IN} – V_{OUT} voltage combined with the BIAS pin dramatically improve the efficiency of low-voltage output applications by powering the voltage reference and control circuitry and allowing the use of a pre-regulated, low-voltage input supply (IN) for the main power path. This low-dropout regulator (LDO) offers foldback current limit, shutdown, thermal protection, and active discharge.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Excellent Transient Response

The TPS7A15 responds quickly to a change on the input supply (line transient) or the output current (load transient) given the device high input impedance and low output impedance across frequency. This same capability also means that this LDO has a high power-supply rejection ratio (PSRR) and, when coupled with a low internal noise-floor (e_n), the LDO approximates an ideal power supply with outstanding line and load transient performance.

The choice of external component values optimizes the transient response; see the *Input, Output, and Bias Capacitor Requirements* section for proper capacitor selection.

7.3.2 Active Overshoot Pulldown Circuitry

When the LDO is active (when $V_{EN} \geq V_{HIGH(EN)}$), and the output voltage rises above the nominal voltage, a current sink in series with a resistor connected to V_{OUT} is enabled and the output is pulled down until near to the nominal voltage. This feature helps reduce overshoot when recovering from transients.

7.3.3 Global Undervoltage Lockout (UVLO)

The TPS7A15 uses two undervoltage lockout circuits: one on the BIAS pin and one on the IN pin to prevent the device from turning on before both V_{BIAS} and V_{IN} rise above their lockout voltages. The two UVLO signals are connected internally through an AND gate, as shown in Figure 7-1, that turns off the device when the voltage on either input is below their respective UVLO thresholds.

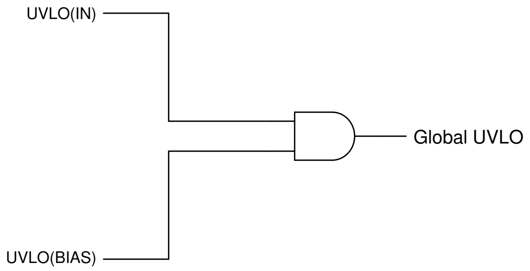


Figure 7-1. Global UVLO Circuit

7.3.4 Enable Input

The enable input (EN) is active high. Applying a voltage greater than $V_{EN(HI)}$ to EN enables the regulator output voltage, and applying a voltage less than $V_{EN(LOW)}$ to EN disables the regulator output. If independent control of the output voltage is not needed, connect EN to either IN or BIAS.

7.3.5 Internal Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$).

In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted to GND, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 60\% \times V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on.

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If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 7-2 shows a diagram of the foldback current limit.

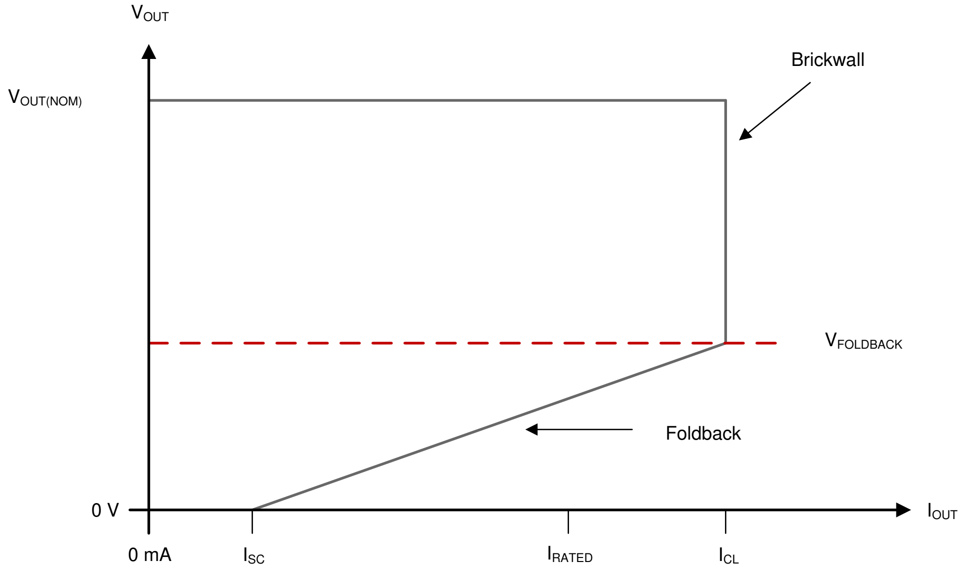

Figure 7-2. Foldback Current Limit

7.3.6 Active Discharge

The active discharge function uses an internal MOSFET that connects a resistor ($R_{PULLDOWN}$) to ground when the LDO is disabled in order to actively discharge the output voltage. The active discharge circuit is activated by driving EN to logic low to disable the device, when the voltage at IN or BIAS is below the UVLO threshold, or when the regulator is in thermal shutdown. Active discharge does not operate when both IN and BIAS are off, because this function requires sufficient input voltage to turn on the internal MOSFET.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device-rated current.

7.3.7 Thermal Shutdown

The internal thermal shutdown protection circuit disables the output when the thermal junction temperature (T_J) of the pass transistor rises to the thermal shutdown temperature threshold, $T_{SD(shutdown)}$ (typical). The thermal shutdown circuit hysteresis ensures that the LDO resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time constant of the semiconductor die is fairly short; thus, the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

Table 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} \geq V_{OUT\ (nom)} + V_{DO}$ and $V_{IN} \geq V_{IN(min)}$	$V_{BIAS} \geq V_{OUT} + V_{DO(BIAS)}$	$V_{EN} \geq V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT\ (nom)} + V_{DO(IN)}$	$V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J \geq T_{SD}$ for shutdown

7.4.1 Normal Mode

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The bias voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.2 Dropout Mode

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. Similarly, if the bias voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode as well. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$ or $V_{BIAS} < V_{OUT(NOM)} + V_{DO}$ directly after being in normal regulation state, but not during start up), the pass transistor is driven into ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short time when the device pulls the pass transistor back into the linear region.

7.4.3 Disabled Mode

The output of the device can be shut down by forcing the voltage of the enable pin to less than the maximum EN pin low-level voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

8.1.1 Recommended Capacitor Types

The regulator is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and bias pins. Multilayer ceramic capacitors are the industry standard for use with LDOs, but must be used with good judgment. Ceramic capacitors that use X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance. Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. Generally, assume that effective capacitance decreases by as much as 50%. The input, output, and bias capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input, Output, and Bias Capacitor Requirements

A minimum input ceramic capacitor is required for stability. A minimum output ceramic capacitor is also required for stability; see the *Recommended Operating Conditions* table for the minimum capacitor values.

The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. A higher-value input capacitor may be necessary if large, fast rise-time load or line transients are anticipated, or if the device is located several inches from the input power source. Dynamic performance of the device is improved with the use of an output capacitance larger than the minimum value specified in the *Recommended Operating Conditions* table, thus use a larger capacitance than the minimum value when practical.

Although a bias capacitor is not required, good design practice is to connect a 0.1-µF ceramic capacitor from BIAS to GND. This capacitor counteracts reactive bias source effects if the source impedance is not sufficiently low. If the BIAS source is susceptible to fast voltage drops (for example, a 2-V drop in less than 1 µs) when the LDO load current is near the maximum value, the BIAS voltage drop can cause the output voltage to fall briefly. In such cases, use a BIAS capacitor large enough to slow the voltage ramp rate to less than 0.5 V/µs. For smaller or slower BIAS transients, any output voltage dips must be less than 5% of the nominal voltage.

Place the input, output, and bias capacitors as close as possible to the device to minimize the effects of trace parasitic impedance.

8.1.3 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

Using a bias rail enables the TPS7A15 to achieve a lower dropout voltage between IN and OUT. However, a minimum bias voltage above the nominal programmed output voltage must be maintained. Figure 6-12 specifies the minimum V_{BIAS} headroom required to maintain output regulation.

8.1.4 Behavior During Transition From Dropout Into Regulation

Some applications may have transients that place this device into dropout, especially when this device can be powered from a battery with relatively high ESR. The load transient saturates the output stage of the error amplifier when the pass element is driven fully on, making the pass element function like a resistor from V_{IN} to V_{OUT}. The error amplifier response time to this load transient is limited because the error amplifier must first recover from saturation and then places the pass element back into active mode. During this time, V_{OUT} overshoots because the pass element is functioning as a resistor from V_{IN} to V_{OUT}.

When V_{IN} ramps up slowly for start up, the slow ramp-up voltage may place the device in dropout. As with many other LDOs, the output can overshoot on recovery from this condition. However, this condition is easily avoided through the use of the enable signal.

If operating under these conditions, apply a higher dc load or increase the output capacitance to reduce the overshoot. These solutions provide a path to dissipate the excess charge.

8.1.5 Device Enable Sequencing Requirement

The IN, BIAS, and EN pin voltages can be sequenced in any order without causing damage to the device. Start up is always monotonic regardless of the sequencing order or the ramp rates of the IN, BIAS, and EN pins. See the *Recommended Operating Conditions* table for proper voltage ranges of the IN, BIAS, and EN pins.

8.1.6 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current while output voltage regulation is maintained. See the *Typical Characteristics* section for the typical load transient response. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions in Load Transient Waveform are broken down as described in this section. Regions A, E, and H are where the output voltage is in steady-state operation.

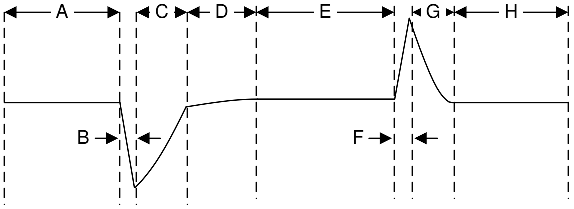

Figure 8-1. Load Transient Waveform

During transitions from a light load to a heavy load, the following behavior can be observed:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to an increase in the output capacitor charge (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

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A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

8.1.7 Undervoltage Lockout Circuit Operation

The V_{IN} UVLO circuit makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range. The V_{IN} UVLO circuit also makes sure that the device shuts down when the input supply collapses. Similarly, the V_{BIAS} UVLO circuit makes sure that the device stays disabled before the bias supply reaches the minimum operational voltage range. The V_{BIAS} UVLO circuit also makes sure that the device shuts down when the bias supply collapses.

Typical VIN or VBIAS UVLO Circuit Operation depicts the UVLO circuit response to various input or bias voltage events. The diagram can be separated into the following parts:

- Region A: The output remains off while either the input or bias voltage is below the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device is still enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls as a result of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached and a normal start up follows.
- Region F: Normal operation followed by the input or bias falling to the UVLO falling threshold.
- Region G: The device is disabled when either the input or bias voltage falls below the UVLO falling threshold to 0 V. The output falls as a result of the load and active discharge circuit.

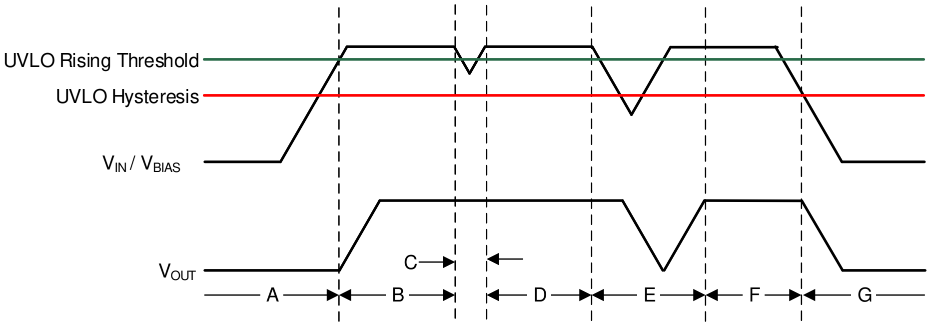

Figure 8-2. Typical V_{IN} or V_{BIAS} UVLO Circuit Operation

8.1.8 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

Equation 2 calculates the maximum allowable power dissipation for the device in a given package:

$$P_{D\text{-}MAX} = [(T_J - T_A) / R_{\theta JA}] \quad (2)$$

Equation 3 represents the actual power being dissipated in the device:

$$P_D = [(I_{GND(IN)} + I_{IN}) \times V_{IN} + I_{GND(BIAS)} \times V_{BIAS}] - (I_{OUT} \times V_{OUT}) \quad (3)$$

If the load current is much greater than $I_{GND(IN)}$ and $I_{GND(BIAS)}$, Equation 3 can be simplified as:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A15 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device depends on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 5, maximum power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). The equation is rearranged in Equation 6 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (6)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the YCK package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

8.1.9 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 7 and are given in the *Electrical Characteristics* table.

$$\Psi_{JT}\text{: } T_J = T_T + \Psi_{JT} \times P_D \text{ and} \\ \Psi_{JB}\text{: } T_J = T_B + \Psi_{JB} \times P_D \quad (7)$$

where:

- P_D is the power dissipated as explained in Equation 3 and the *Power Dissipation (P_D)* section
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.10 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is illustrated in Figure 8-3 and can be separated into the following regions:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} – V_{OUT}$) at a given output current level; see the *Dropout Mode* section for more details.
- The rated output current limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - Figure 8-3 provides the shape of the slope. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus, when $V_{IN} – V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} – V_{OUT}$.

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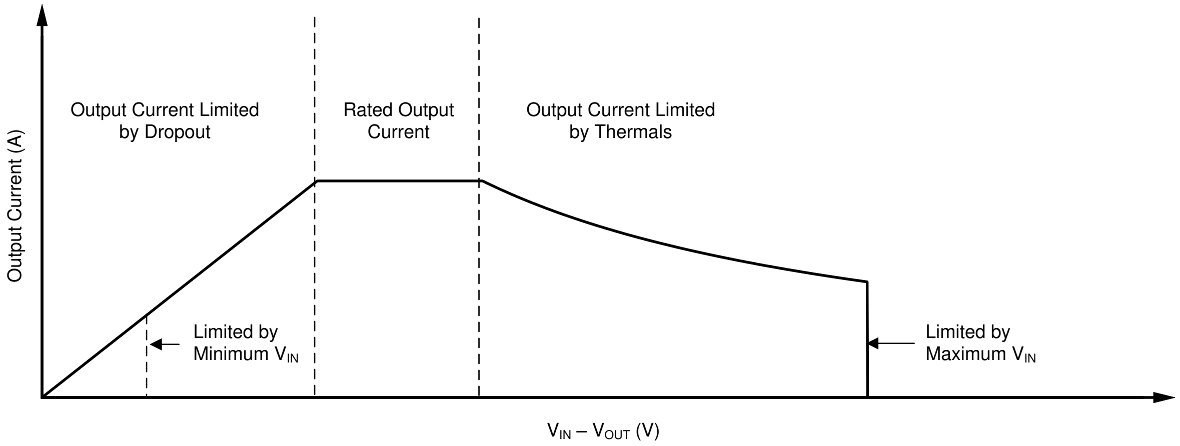

Figure 8-3. Continuous Operation Diagram With Description of Regions

8.2 Typical Application

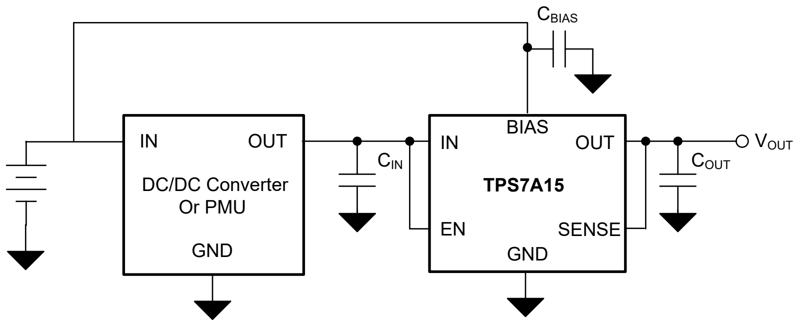

Figure 8-4. High-Efficiency Supply From a Rechargeable Battery

8.2.1 Design Requirements

Table 8-1 lists the parameters for this design example.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.05 V
V_{BIAS}	2.4 V to 5.5 V
V_{OUT}	0.9 V
I_{OUT}	350 mA

8.2.2 Detailed Design Procedure

This design example is powered by a rechargeable battery that can be a building block in many portable applications. Noise-sensitive portable electronics require an efficient, small-size solution for their power supply. Traditional LDOs are known for their low efficiency in contrast to low-input, low-output voltage (LILO) LDOs, such as the TPS7A15. Using a bias rail in the TPS7A15 allows the device to operate at a lower input voltage, thus reducing the voltage drop across the pass transistor and maximizing device efficiency. The low voltage drop allows the efficiency of the LDO to approximate that of a DC/DC converter. Equation 8 calculates the efficiency for this design.

$$\text{Efficiency} = \eta = P_{OUT} / P_{IN} \times 100\ \% = (V_{OUT} \times I_{OUT}) / (V_{IN} \times I_{IN} + V_{BIAS} \times I_{BIAS}) \times 100\ \% \quad (8)$$

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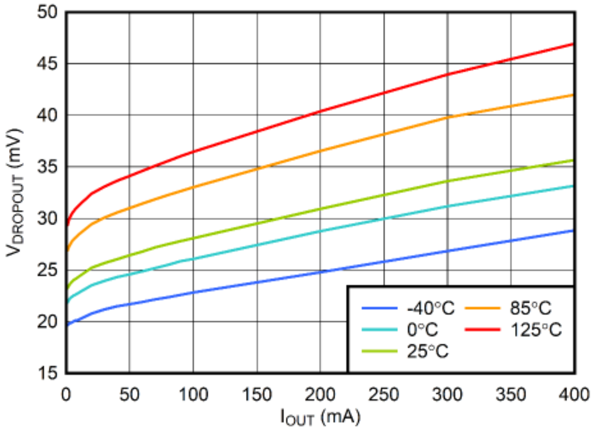
Equation 8 reduces to Equation 9 because the design example load current is much greater than the quiescent current of the bias rail.

$$\text{Efficiency} = \eta = (V_{OUT} \times I_{OUT}) / (V_{IN} \times I_{IN}) \times 100\% \tag{9}$$

For this design example, the 0.9-V output version (TPS7A1509) is selected. A nominal 1.05-V input supply comes from a DC/DC converter connected to the battery. Use a minimum 1.0-µF input capacitor to minimize the effect of resistance and inductance between the 1.05-V source and the LDO input. A minimum 2.2-µF output capacitor is also recommended for stability and good load transient response.

The dropout voltage (VDO) is less than 80 mV maximum at a 0.9-V output voltage and 400-mA output current, so there are no dropout issues with a minimum input voltage of 1.0 V and a maximum output current of 200 mA. In addition, the TPS7A15 is designed to meet its key specifications so long as the input voltage is at least 100 mV greater than the output voltage.

8.2.3 Application Curve



$V_{BIAS} = V_{OUT(NOM)} + 1.4$ V, $V_{EN} = V_{IN}$, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, $C_{BIAS} = 0.1$ µF

Figure 8-5. V_{IN} Dropout Voltage vs I_{OUT}

8.3 Power Supply Recommendations

This LDO is designed to operate from an input supply voltage range of 0.7 V to 2.2 V and a bias supply voltage range of 2.2 V to 5.5 V. The input and bias supplies must be well regulated and free of spurious noise. To make sure that the output voltage is well regulated and dynamic performance is at optimum, the input supply must be at least $V_{OUT(nom)} + V_{DO}$ and $V_{BIAS} = V_{OUT(nom)} + V_{DO(BIAS)}$.

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8.4 Layout

8.4.1 Layout Guidelines

For correct printed circuit board (PCB) layout, follow these guidelines:

- Place input, output, and bias capacitors as close to the device as possible
- Use copper planes for device connections to optimize thermal performance
- Place thermal vias around the device to distribute heat

8.4.2 Layout Example

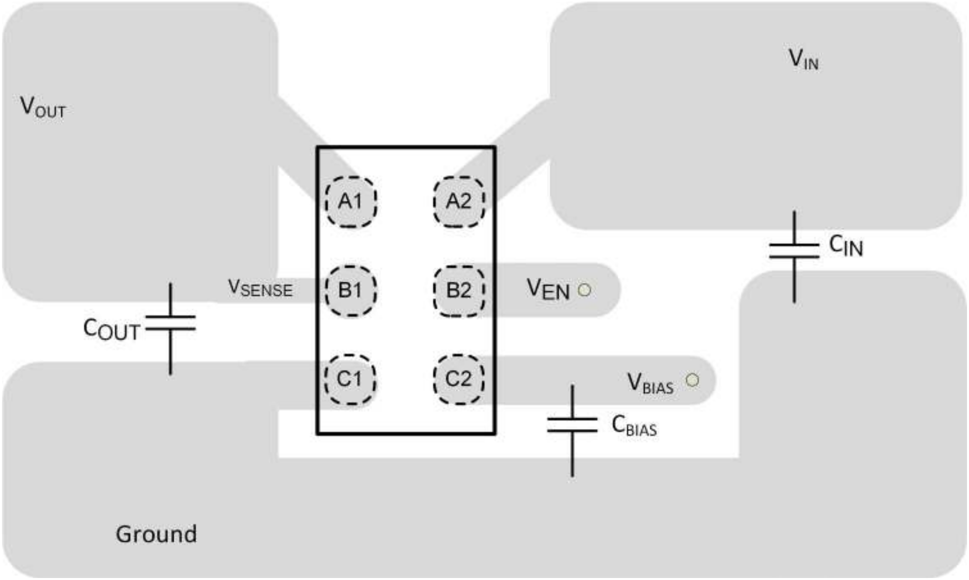

Figure 8-6. Recommended Layout (YCK Package)

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

Table 9-1. Device Nomenclature(1) (2)

PRODUCT	DESCRIPTION
TPS7A15**xx(x)(P)yyyz**	**xx(x)** is the nominal output voltage. Two or more digits are used in the ordering number (for example, 09 = 0.9 V; 95 = 0.95 V; 125 = 1.25 V). **P** indicates an active pull down; if there is no P, then the device does not have the active pull-down feature. **yyy** is the package designator. **z** is the package quantity. R is for reel (12000 pieces for YBK package; 3000 pieces for DRV package).

(1) For the most current package and ordering information see the *Package Option Addendum* at the end of this document, or visit the device product folder on www.ti.com.

(2) Output voltages from 0.5 V to 2.0 V in 25-mV increments are available. Contact TI for details and availability.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *AN-1112 DSBGA Wafer Level Chip Scale Package* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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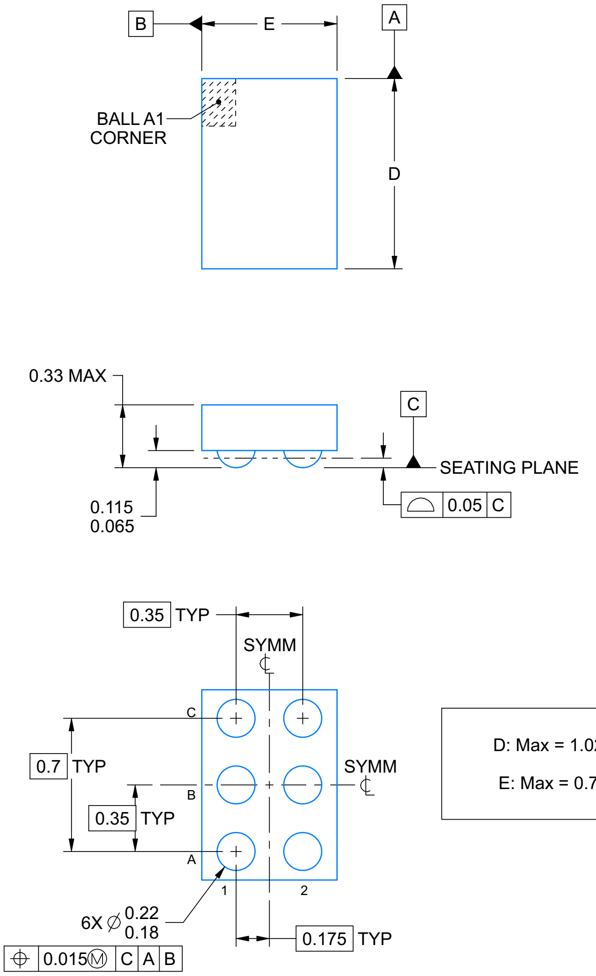
10.1 Mechanical Data

PACKAGE OUTLINE

YCK0006-C02

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.02 mm, Min = 0.98 mm

E: Max = 0.73 mm, Min = 0.69 mm

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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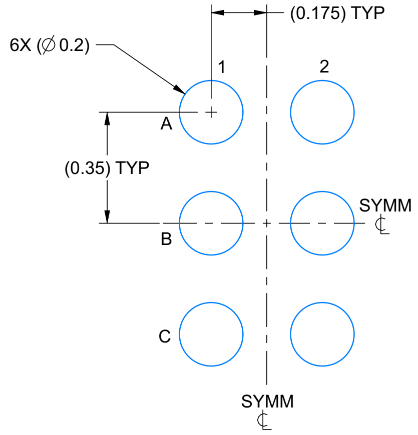
EXAMPLE BOARD LAYOUT

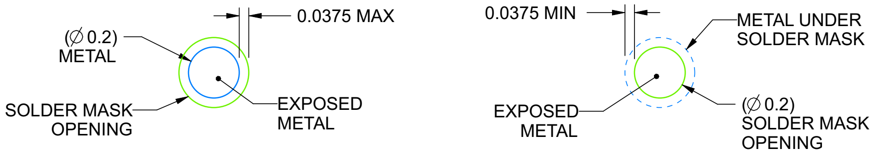
YCK0006-C02

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



NON-SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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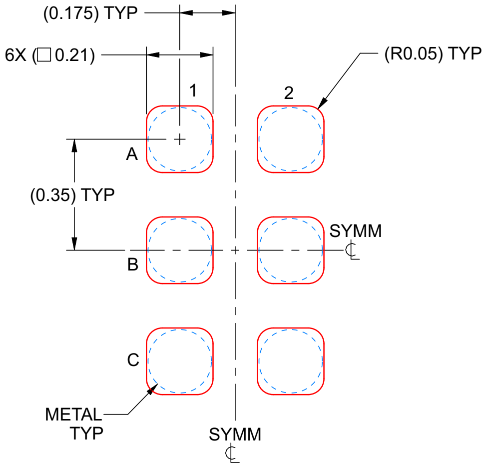
EXAMPLE STENCIL DESIGN

YCK0006-C02

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A1508PYCKR	ACTIVE	DSBGA	YCK	6	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	MW	Samples
TPS7A1509PYCKR	ACTIVE	DSBGA	YCK	6	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	MV	Samples
XS7A1508PDRVR	ACTIVE	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XS7A1518PDRVR	ACTIVE	WSON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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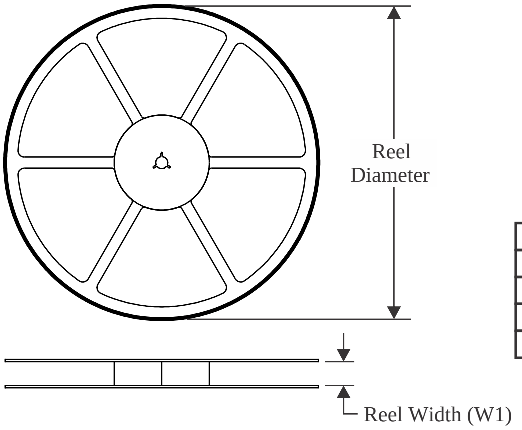
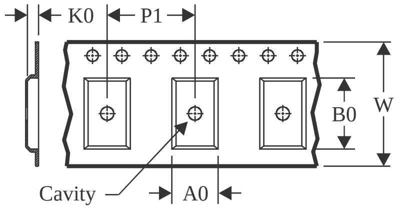
TAPE AND REEL INFORMATION

REEL DIMENSIONS

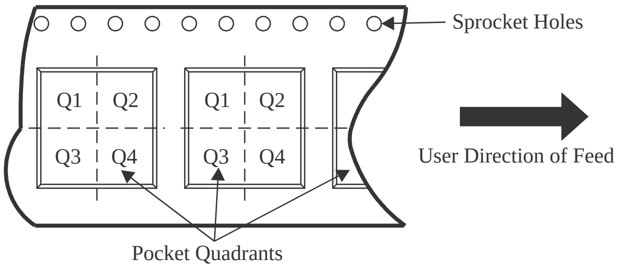


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

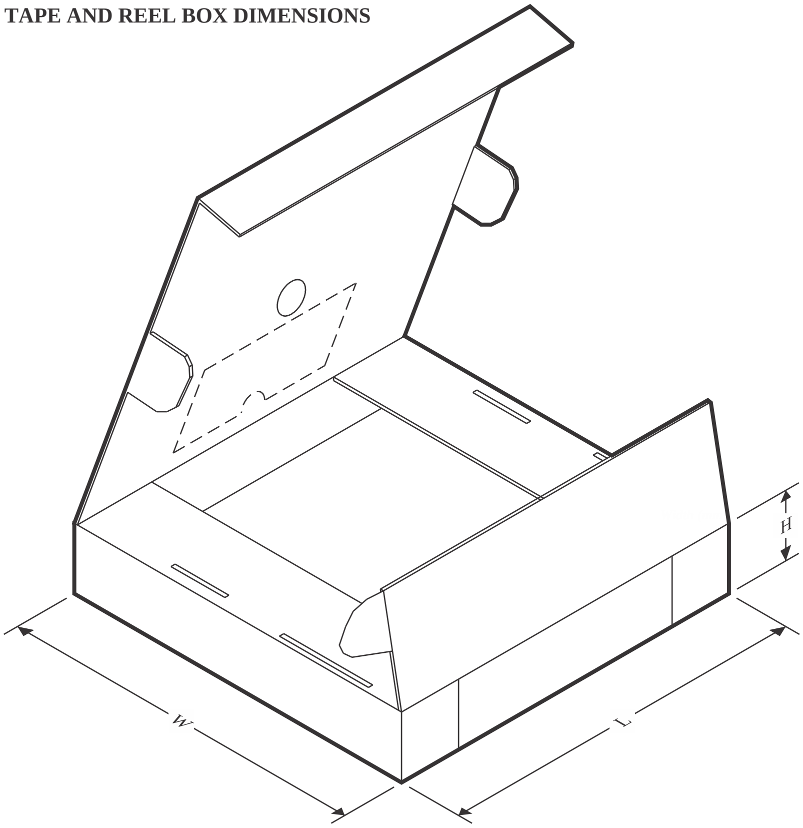
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1508PYCKR	DSBGA	YCK	6	12000	180.0	8.4	0.8	1.1	0.34	2.0	8.0	Q1
TPS7A1508PYCKR	DSBGA	YCK	6	12000	180.0	8.4	0.8	1.1	0.34	2.0	8.0	Q1
TPS7A1509PYCKR	DSBGA	YCK	6	12000	180.0	8.4	0.8	1.1	0.34	2.0	8.0	Q1
TPS7A1509PYCKR	DSBGA	YCK	6	12000	180.0	8.4	0.8	1.1	0.34	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



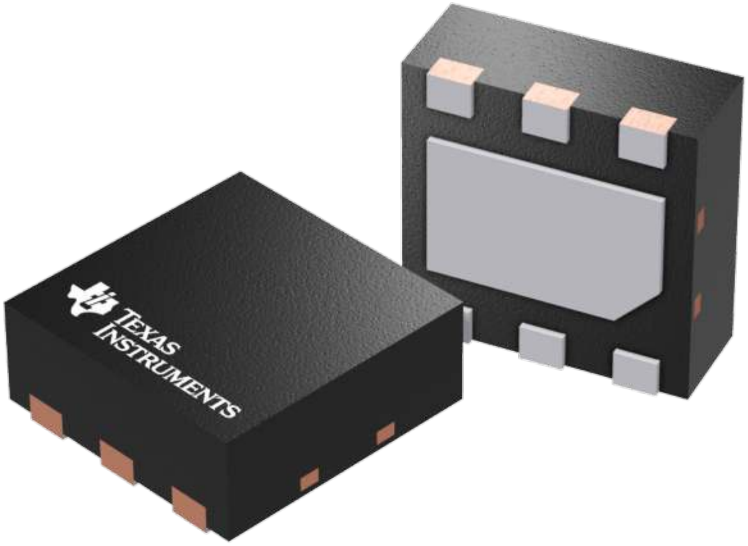
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1508PYCKR	DSBGA	YCK	6	12000	182.0	182.0	20.0
TPS7A1508PYCKR	DSBGA	YCK	6	12000	182.0	182.0	20.0
TPS7A1509PYCKR	DSBGA	YCK	6	12000	182.0	182.0	20.0
TPS7A1509PYCKR	DSBGA	YCK	6	12000	182.0	182.0	20.0

DRV 6

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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