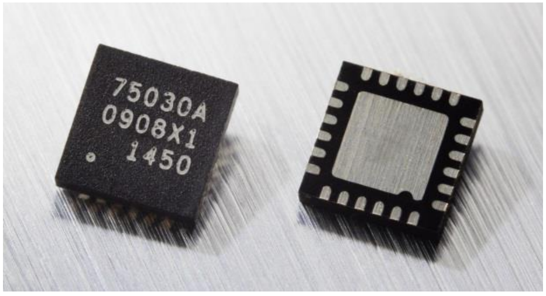
Features & Benefits

- Two independent simultaneously operating active light measurement channels
- Integrated DC light cancellation circuitry for active light channel DC light suppression
- Two logarithmic ambient light channels
- High input capacitance tolerant input current terminals
- Extremely high degree of adaptability for different optical systems
- Stand-by and sleep modes
- Integrated 16bit ADC
- Integrated temperature sensor
- Digital communication interface via SPI
- Integrated watchdog timer
- High safety design by comprehensive diagnostic and monitoring functions
- Minimum amount of external components
- Small-size SMD package QFN24 4x4 mm



Ordering Information

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX75030	R	LW	BAA-000	RE or TU
MLX75030	C	LW	BAA-000	RE or TU

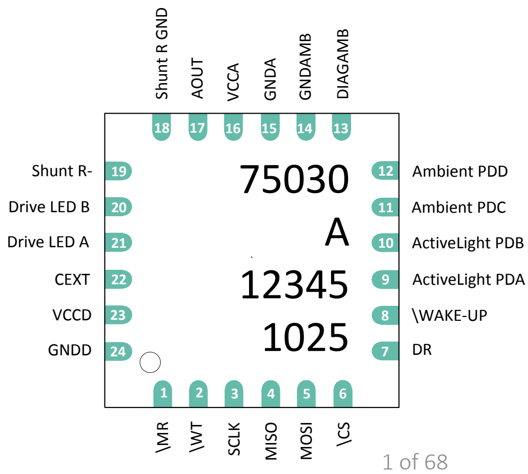
Legend:

Temperature Code:	R = -40 to 105°C, C = 0°C to 70°C
Package Code:	LW = = Quad Flat Package (QFN) with wettable flanks
Option Code:	BAA-000 = Design Revision
Packing Form:	RE = Reel, TU = Tube
Ordering example:	MLX75030RLW-BAA-000-RE

Application Examples

- Optical proximity sensing & display dimming
- Touch-less gesture recognition
- Driver/passenger discrimination
- Touch Screen Wake-up on Proximity

Pin Description



1. General Description

The MLX75030 Universal ActiveLight Sensor Interface has been designed to allow easy and robust dual-channel optical reflection and dual channel ambient light measurement. Therefore it is ideally suited for the design of responsive human-machine interfaces (HMI) that require proximity or gesture detection in environments subject to wide background light level variations, possibly in combination with display dimming.

The MLX75030 IC consists of two optical sensor interface parts. Part one is optimized for active light measurements and is designed to control up to 2 external LEDs and to sense modulated light current from up to 2 external photodiodes on independent channels A and B. The ActiveLight detection is virtually independent from background light by means of integrated hardware-level ambient light suppression. Part two consists of two logarithmic current sensors C and D, which measure the photocurrent of externally connected photodiodes. Simple and programmable operation is ensured by internal control logic, configurable user registers and SPI communication.

2. Functional Block Diagram

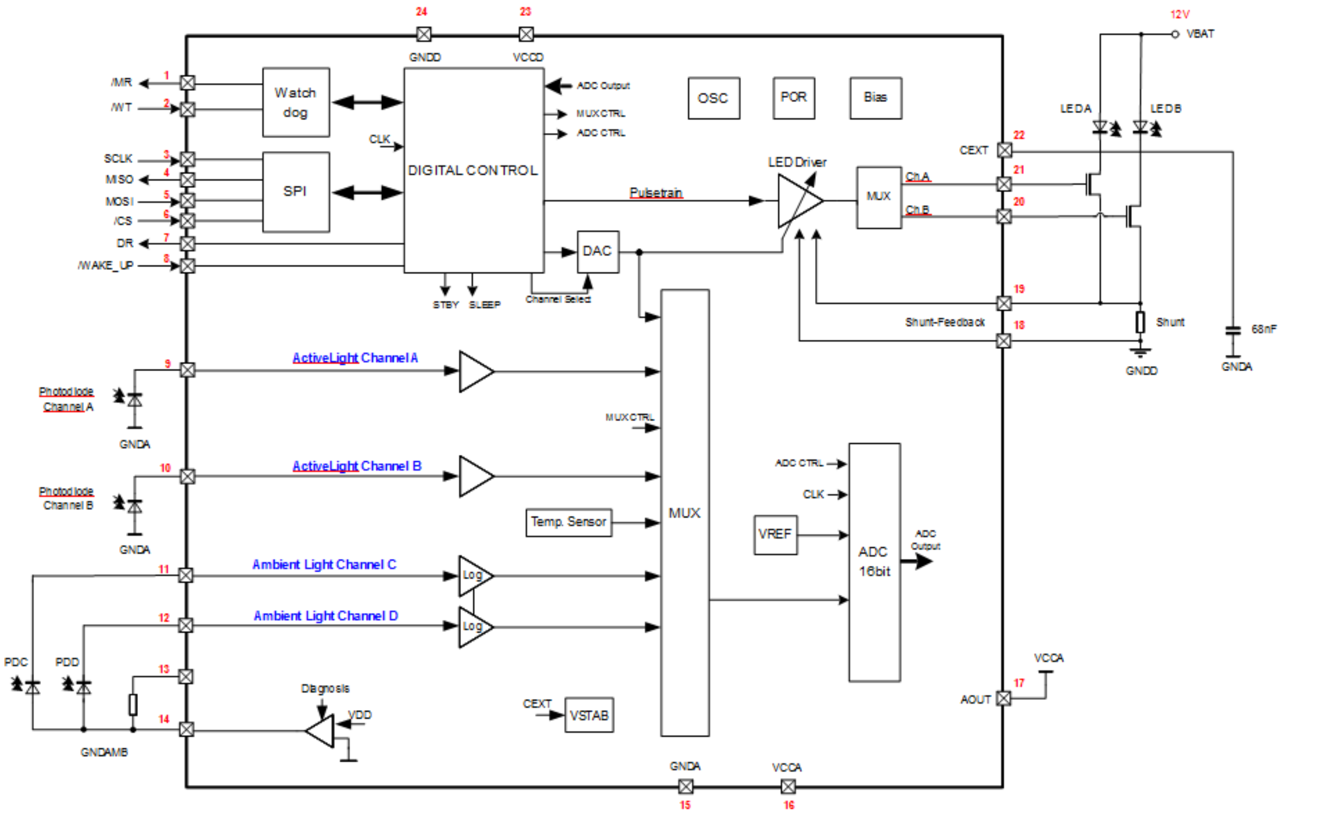


Figure 1 : MLX75030 Functional Block Diagram

3. Application Diagram

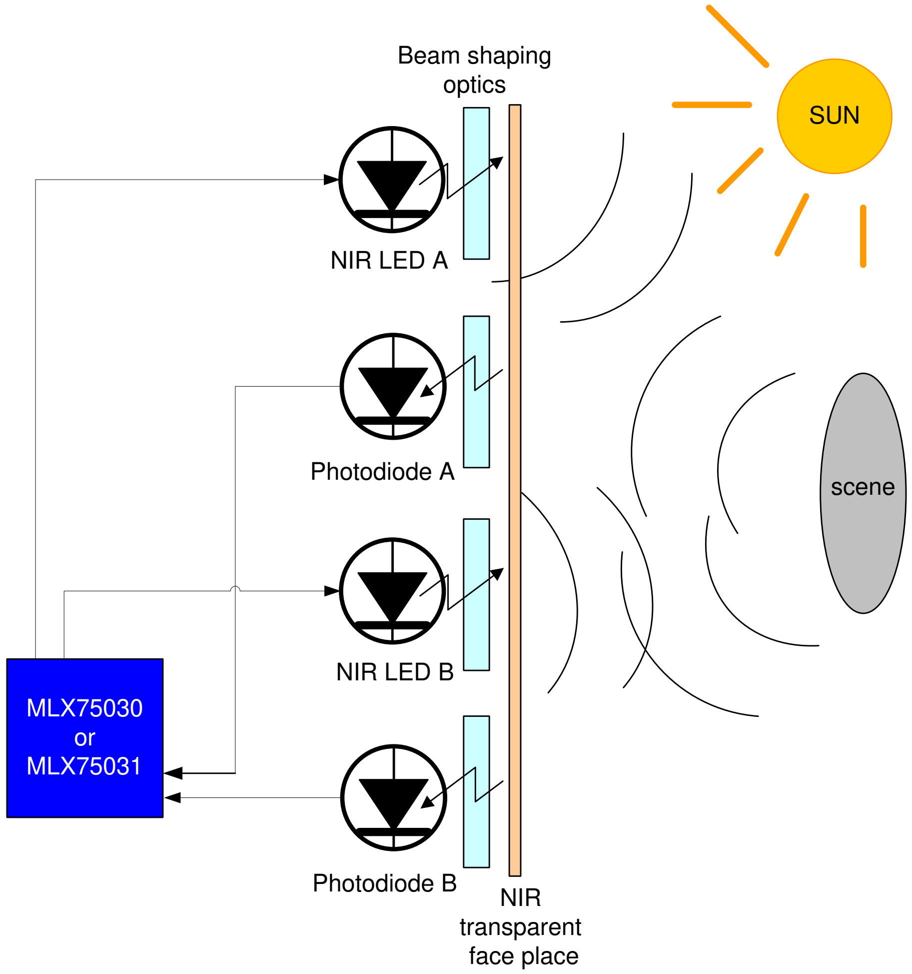


Figure 2 : Application diagram of a dual channel active reflection detector with 2 photodiodes and 2 LEDs.
The measured signal is virtually independent of background light from the sun or other sources.

Table of Contents

4. Glossary of Terms

ADC	Analog-Digital converter
CR	Chip Reset
CRC	Cyclic Redundancy Check
CS	Chip Select
CSLP	Confirm Sleep
CSTBY	Confirm Standby
CTRL	Control Signal
DAC	Digital to Analog Converter
DC	Direct Current
DR	Device Ready
EMC	Electromagnetic Compatibility
GNDA	Ground for analog Blocks of MLX7530
GNDD	Ground for digital Blocks of MLX75030
IR	Infrared
LED	Light emitting diode
LPF	Low-pass filter
LSB	Least Significant Bit
MISO	Master In Slave Out
MOSI	Master Out Slave In
MR	Master Reset
MSB	Most Significant Bit
MUX	Multiplexer
NOP	No Operation
NP	Number of Pulses
NRM	Normal Running Mode
OSC	Oscillator
OTP	One time programmable
OTR	Optical transfer ratio
PD	Photodiode
POR	Power on reset
RCO	RC-Oscillator
RO	Read-Out
RR	Read Register
RSLP	Request Sleep
RSTBY	Request Standby
S&H	Sample and Hold
SCLK	SPI Shift Clock
SC-LPF	Switched Capacitor biquad Low-pass filter
SM	Start Measurement
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TIA	Transimpedance Amplifier
VBATT_30	VBATT which is supplied from connection 30 of the car
VCCA	Supply Voltage for the analog blocks
VCCD	Supply Voltage for the digital blocks
VDD_30	VDD which is supplied from connection 30 of the car
VSENSE	Voltage across the shunt resistor
WDT	Watchdog Timer
WR	Write Register
WT	Watchdog Trigger
uC	Microcontroller

5. Absolute Maximum Ratings

Exceeding the absolute maximum ratings may cause permanent damage.
Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

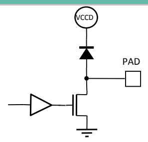
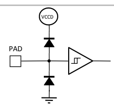
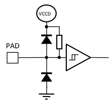
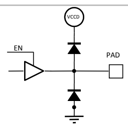
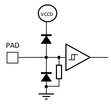
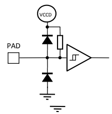
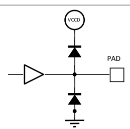
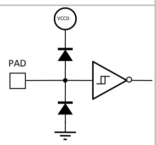
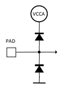
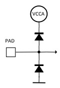
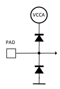
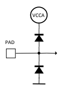
Parameter	Symbol	Condition	Min	Max	Units
Supply voltage range	V_{DD}		-0.3	5.0	V
Terminal current	$I_{terminal}$	*per bondpad*	-20	+20	mA
Terminal voltage	$V_{terminal}$	*Pins 1-8, 14-24*	-0.3	V_{DD}+0.3	V
		Pins 9-13[1]	-0.3	V_{DD}+0.3	V
Storage temperature	T_{stg}		-40	+150	°C
Junction temperature	T_j			+150	°C
Power dissipation[2]	P_{tot}	*For max ambient temperature of 100°C and Teta_ja = 154K/W*		320	mW
ESD capability of any pin (Human Body Model)	ESD_{HBM}	*Human body model, acc. to AEC-Q100-002*	-2	2	kV
		Pins 9-13	-1	1	kV
ESD capability of any pin (Charge device model)	ESD_{CDM}	*Charge device model acc. to AEC- Q100-011*	-750	+750	V
Maximum latch–up free current at any pin	I_{LATCH}	*JEDEC- Standard EIA / JESD78*	-100	+100	mA

Table 1 : Absolute Maximum Ratings

[1] Pins 9-13 require special care with regard to the used ESD protection devices, since these nodes of the design are very sensitive to substrate noise and/or leakage currents.

[2] The Power dissipation is valid for ϑ_{JA} values for the 24 Pin QFN 4x4 package according to Table 27.

6. Pin Definitions & Descriptions

Pin №	Name	Functional Schematic	Type	Function
1	\MR		Digital Output	Master Reset
2	\WT		Digital Input	Watchdog Trigger
3	SCLK		Digital Input	SPI Shift Clock
4	MISO		Digital Output	SPI Data Output
5	MOSI		Digital Input	SPI Data Input
6	\CS		Digital Input	Chip Select
7	DR		Digital Output	Device Ready
8	\WAKE-UP		Digital Input	Normal Mode
9	ActiveLight Detect PDA		Analog Input	IR Photo Diode A
10	ActiveLight Detect PDB		Analog Input	IR Photo Diode B
11	Ambient PDC		Analog Input	Ambient Light Photo Diode C
12	Ambient PDD		Analog Input	Ambient Light Photo Diode D

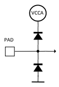
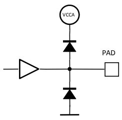
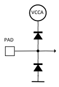
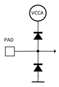
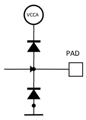
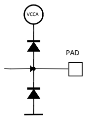
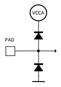
13	DIAGAMB		Analog Input	Ambient channel diagnostic
14	GNDAMB		Analog I/O	Ground Ambient Light Channels
15	GNDA		Ground	Ground
16	VCCA		Supply	Regulated Power Supply
17	AOUT		Analog I/O	Analog Test Output, connect to VCCA
18	Shunt R GND		Analog Input	Shunt resistor feedback to Ground
19	Shunt R-		Analog Input	Shunt resistor feedback
20	Drive LED B		Analog Output	Drives FET gate for IR LED Emitter B
21	Drive LED A		Analog Output	Drives FET gate for IR LED Emitter A
22	CEXT		Analog Input	External blocking Cap, connected to GNDA
23	VCCD		Supply	Regulated external power supply
24	GNDD		Ground	Ground

Table 2 : Pin definitions and descriptions

7. General Electrical Specifications

DC Operating Parameters T_A = -40°C to 105°C (R version), T_A = 0°C to 70°C (C version), V_{DD} = 3.0V to 3.6V (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Voltage range	V_{DD}		3.0	3.3	3.6	V
Supply Current (active Mode)	I_{DD}	without photodiode dc current			6	mA
Standby Current	I_{SBY}	@ Vcc=3.6V, T=30°C			500	uA
Sleep Current	I_{Sleep}	@ Vcc=3.6V, T=30°C			50	uA
Operation Temperature Range	T_A		-40		105	°C
Pull-up resistor	Rpu	for SCLK and \CS		50k		Ohm
Pull-down resistor	Rpd	for MOSI		50k		Ohm
High-level Input Voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Low-level Input Voltage	V_{IL}		0		0.3 V_{DD}	V
Hysteresis on Digital Inputs	V_{HYST}			0.28		V
High Output Voltage (not on pin MR)	V_{OH}	C_L=30pF	0.8 V_{DD}		V_{DD}	V
Low Output Voltage (not on pin MR)	V_{OL}	C_L=30pF	0		0.2 V_{DD}	V
Input leakage	I_{LK}		-10		10	µA
Tri-state Output Leakage Current	I_{OZ}		-10		10	µA
Input Capacitance, per Pin	C_{IN}			10		pF
Output voltage Low, Pin MR	V_{OutL}	I_{ODC}=2mA			0.1	V

Table 3 : Electrical specifications

8. Sensor Specific Specifications

DC Operating Parameters T_A = -40°C to 105°C, T_A = 0°C to 70°C (C version),
V_{DD} = 3.0V to 3.6V (unless otherwise specified)

ActiveLight Channels (Detectors A & B)						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Active light signal optical transfer ratio	$OTR = \frac{I_{LED}}{I_{PDAB}}$		30		80000	
dc sunlight signal	I_{Sun}		140		900	uA
fast full scale transition at I_{sunmax}	$t_{sunrise}$		3.5			ms
min. relative active light modulation (referred to received IR signal)	$\frac{\Delta I_{PDAB\_min}}{I_{PDAB}}$	- 400Hz BW, - max LED current of 1000mA - 25°C - dc sun constant - ActiveLight response time per channel 2.5ms			0.3	%
Carrier frequency range for ActiveLight measurement	f_0	selectable via "SetPF" register, see also 9.4.6	45.7		109.4	kHz
Input capacitance PDA, PDB	$C_{PDA,B}$	At 1.0 V reverse bias			10	pF
DC light measurement range	$I_{DC\ range}$		0		275	uA
DC light measurement offset	$I_{DC\ offset}$	At I_{DC} = 0uA	4096	7168	10240	LSB
DC light measurement slope	$I_{DC\ sens}$		115	150	184	LSB/uA
DC light measurement		Idc range: 0uA -> 275uA		5	12	%
DC light measurement word				16		Bit
DC light measurement		for averaging of 8		13		Bit
TIA Test pulse	$ADC_{TIA\_test\_00}$	T=27°C, DACA6=0, DACA7=0 Gain Anti-alias Filter=2 ADC Buffer bypassed	35035	36182	37570	LSB
Temperature coefficient of TIA Test pulse	$TC\ ADC_{TIA\_test\_00}$	DACA6=0, DACA7=0 Gain Anti-alias Filter=2 ADC Buffer bypassed		-2.78		LSB/K
TIA Test pulse step width	$ADC_{TIA\_test\_step}$	T=27°C, Gain Anti-alias Filter=2 ADC Buffer bypassed	4458	5932	7770	LSB
Temperature coefficient of TIA Test pulse step width	$TC\ ADC_{TIA\_test\_step}$	Gain Anti-alias Filter=2 ADC Buffer bypassed		-4.8		LSB/K
TIA Test pulse step width variation	$\Delta_{ADC\_TIA\_TEST\_STEP}$	Gain Anitalias Filter=2 ADC Buffer bypassed		5	10	%
Error condition Err6						
Critical error detected on TIA output, is TIA output outside 1.1V+/- (0.65 … 0.75V) Note: • Critical error may occur if the referring active light Channel is disabled and the according diagnostic function is enabled (see EnChan register). • Critical error may occur after enabling of the referring active light Channel due to analog settling time.						

Table 4 : ActiveLight sensor channels specifications

ActiveLight Channel DC-Light Compensation						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Maximum ActiveLight Signal DC-Light compensation range	RS_{COMP_max}	in percent of LED current DC_COMP_IC1,2,3,4,5=15 DAC=255	15	20		%
ActiveLight Signal Compensation Offset	RS_{COMP_Offset}	in percent of LED current @ Idc = 0uA			0.8	%
Range of segment 1	Iamb_1	1rst corner dc current	7.2	10.0	12.0	uA
Range of segment 2	Iamb_2	2nd corner dc current	40.0	45.0	50.0	uA
Range of segment 3	Iamb_3	3rd corner dc current	135.0	150.0	165.0	uA
Range of segment 4	Iamb_4	4th corner dc current	440.0	500.0	560.0	uA
Full compensation level @ segment 1	Icomp_1	DC_COMP_IC1,2,3,4,5 = 15 DAC=255 in percent of LED current	1.5	3.5	4.7	%
Full compensation level @ segment 2	Icomp_2		5.1	7.7	10.3	%
Full compensation level @ segment 3	Icomp_3		9.5	13.7	17.9	%
Full compensation level @ segment 4	Icomp_4		13.6	18.8	24.0	%
Full compensation level @ 900uA (max DC sunlight)	Icomp_5		15.0	20.7	25.8	%
Full compensation level @ segment 1	Icomp_1	DC_COMP_IC1,2,3,4,5 = 7 DAC=255 in percent of LED current	0.65	1.6	2.2	%
Full compensation level @ segment 2	Icomp_2		2.4	3.6	4.8	%
Full compensation level @ segment 3	Icomp_3		4.4	6.4	8.4	%
Full compensation level @ segment 4	Icomp_4		6.3	8.85	11.4	%
Full compensation level @ 900uA (max DC sunlight)	Icomp_5		7.1	9.6	12.1	%
DC_COMP_IC1 = 15, other =0	I_{C_1}	in percent of LED current	1.4	2.3	2.8	%
DC_COMP_IC2 = 15, other =0	I_{C_2}	in percent of LED current	2.1	2.9	3.6	%
DC_COMP_IC3 = 15, other =0	I_{C_3}	in percent of LED current	5.0	6.6	8.2	%
DC_COMP_IC4 = 15, other =0	I_{C_4}	in percent of LED current	4.4	5.9	7.3	%
DC_COMP_IC5 = 15, other =0	I_{C_5}	in percent of LED current	2.0	3.0	4.1	%

Table 5: DC light compensation specifications

Ambient Light Channels (detectors C, D)						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Input current range for detectors C	I_{ambc}		0.01		1040	uA
Input current range for detectors D	I_{ambd}		0.0005		20	uA
input current threshold level	I_{ambc_detect}		333			nA
input current threshold level	I_{ambd_detect}		5.5			nA
Input capacity on ambient	C_{ambc}	at 0.6V			1	nF
Input capacity on ambient	C_{ambd}	at 0.6V			100	pF
Transfer function logarithmic	V_{amb}	See section 10.3 and 10.4				
Output Ambient Channel C		At VCC=3,3V, Iin=100uA	29464	32768	36072	LSB
Output Ambient Channel D		At VCC=3,3V, Iin=10uA	29464	32768	36072	LSB
Slope Ambient Channel C		At VCC=3,3V and 105°C	5300	5900	6500	LSB/dec
Slope Ambient Channel D		At VCC=3,3V and 105°C	5300	5900	6500	LSB/dec
Ambient Channels Linearity Error		for Iin ≥ I_{ambx_detect} including temperature compensation		3	5	%
Ambient light word length				16		bits
Ambient light channel resolution		for averaging of 16 measurements		13		bits
Ambient light response time		See section 9.1.3 for a detailed explanation of this parameter. for Iin ≥ I_{ambx_detect}			3	ms
Ambient PDC voltage	V_{ambc}	At VCC=3,3V, Iin=100uA	0.4	0.6	0.9	V
Ambient PDD voltage	V_{ambd}	At VCC=3,3V, Iin=10uA	0.4	0.6	0.9	V
Error condition Err3						
Note: • Err3 is set if output voltage OUTN or OUTP of the ambient channel SC filter is out of range (meaning: <40% of VCCA or >60% of VCCA). Critical error may occur after enabling of the referring Ambient Light Channel due to analog settling time.						

Table 6 : Ambient light channel specifications

Temperature Sensor						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Temp. sensor range	ϑ		-40		105	°C
Temp. sensor transfer function[3]	V_{ϑ}	@ VDD=3,3V	-82	-67	-51	LSB/K
Temp. sensor error	$\vartheta_{error@0...105°C}$	@ VDD=3,3V, T_{amb} = 0…105°C			±5	°C
Temp. response time	t_{resp_ϑ}				1	s
Temp. sensor word length				16		bits
Temp. sensor resolution		for averaging of 16 measurements		13		bits

Table 7 : Temperature sensor specifications

LED Driver						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
LED current		Shunt = 1 Ω	1.05		993	mA
Shunt resistor values			1		10	Ohm
Shunt voltage			1.05		993	mV
Rising and falling time				3		us
DC offset level				1		mV
Time before pulse	T_{dc_pulse}	See section 9.4.1	47.5		420	us
External important transistor parameter						
Max gate source voltage	V_{GS}	VDD=3V			2	V
Max Gate/Basis current	$I_{G/B}$	VDD=3V			400	uA
Error condition Err5						
Err5 difference between Vdac and Vsense. Detection level larger 100mV						

Table 8 : LED driver specifications

POR						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
POR on threshold voltage	V_{POR-ON}		1.58		2.75	V
POR off threshold voltage	$V_{POR-OFF}$		1.68		2.85	V
POR hysteresis voltage	V_{HYS}		60		130	mV

Table 9: Power on Reset specifications

[3] *This value is stored in the Calib1 Register*

SPI and Timing						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
SPI word length					8	bit
SPI Clock Frequency	$f_{SCLK} = 1/t_{SCLK}$		0.5	1	5	MHz
Frequency of Internal RC Oscillator	$f_{RCO} = 1/T_{RCO}$			2.5	±7.5%	MHz
CS low prior to first *SCLK* edge	t_{cs_sclk}		50			ns
CS high after last *SCLK* edge	t_{sclk_cs}		50			ns
CS high time between transmissions	t_{cs_inter}		50			ns
Time between *CS* high and *DR* low	t_{cs_dr}		0		21.84 (232us)[4]	µs
Min low time on *WAKE_UP* pin	t_{wu_l}		100			µs
Min low time on *WT* pin	t_{wt_l}		10			µs
WDT initial active window time	t_{wdt_init}	After POR, Watchdog Reset and Wake-Up		140	±7.5%	ms
WDT open window time	t_{wdt_open}			70	±7.5%	ms
WDT closed window time	t_{wdt_closed}			70	±7.5%	ms
MR low time during reset	t_{MR}	After Watchdog Reset		2	±7.5%	ms
Start-up time after power-on	$t_{startup}$			50	±7.5%	ms
Start-up time after power-on for SPI	$t_{startup\_SPI}$				15	µs
Start-up time after wake-up from sleep	t_{wakeup_slp}			50	±7.5%	ms
Start-up time after wake-up from standby	t_{wakeup_stby}			50	±7.5%	ms
Error condition Err2						
RCO stuck at High or Low						
Error condition Err4						
Internal voltage regulator : err4 is set if the regulator does not start (detection threshold in the range [1V;2V]						

Table 10 : Serial peripheral interface specifications

[4] *with random measurement start, the max time can be up to 232us, if an autozeroing phase of the IC is executed.*

9. Detailed Description

9.1. Analog Sensor Functions

9.1.1. Active Light Sensor

The MLX75030 works with two separate transmit- and receive-channels A and B. In order to perform an active light measurement, carrier modulated light signal bursts are transmitted by the LED(s) and received by the ActiveLight channel detectors connected to the pins 9 and 10. Both receive-channels can work separate or in parallel.

The measured ActiveLight signal current is amplified and converted to digital numbers by the on-board ADC by following formula:

$$A_{ActiveLightADC} = I_{ActiveLightPD} \frac{4.10^4 * K_{DEMOD} * GAIN\_ADJ\_AA * GAIN\_BUF}{50,3 \frac{\mu V}{LSB}} + 2^{15}$$

Where

- $A_{ActiveLightADC}$ is the ActiveLight signal value in DN
- $I_{ActiveLightPD}$ is the ActiveLight signal current in uA
- K_{DEMOD} is a correlation gain value between 0.25 and 0.5, depending on the setting of Tdem bits in register SetAna
- $GAIN\_ADJ\_AA$ is the Anti-aliasing filter gain, set by SetAL and SetBL registers, defaulting to value 2
- $GAIN\_BUF$ is the ADC input buffer gain, set by SetAna and GainBuf registers, defaulting to value 1

It is recommended to use the default values of $GAIN\_ADJ\_AA$ and $GAIN\_BUF$. It is recommended to optimize the value of K_{DEMOD}.

9.1.1.1. Active Light Channel DC Light Measurement

The input DC current compensation circuitry of the transimpedance amplifier is able to supply and measure the dc current supplied to the photodetector. Both active light channels are identical in structure. In order to reach a feasible resolution in the current range of interest (low currents in the range up to 275uA), the measurement characteristic will saturate for currents above the I_{DC} current range, however the compensation circuit is nevertheless able to supply the specified current levels up to 900uA to the detector. The given ADC word length for the active light channel dc light data is 16Bit.

The DC light measurement can be used to estimate ambient light conditions and compensate DC light dependent parameters (see next section).

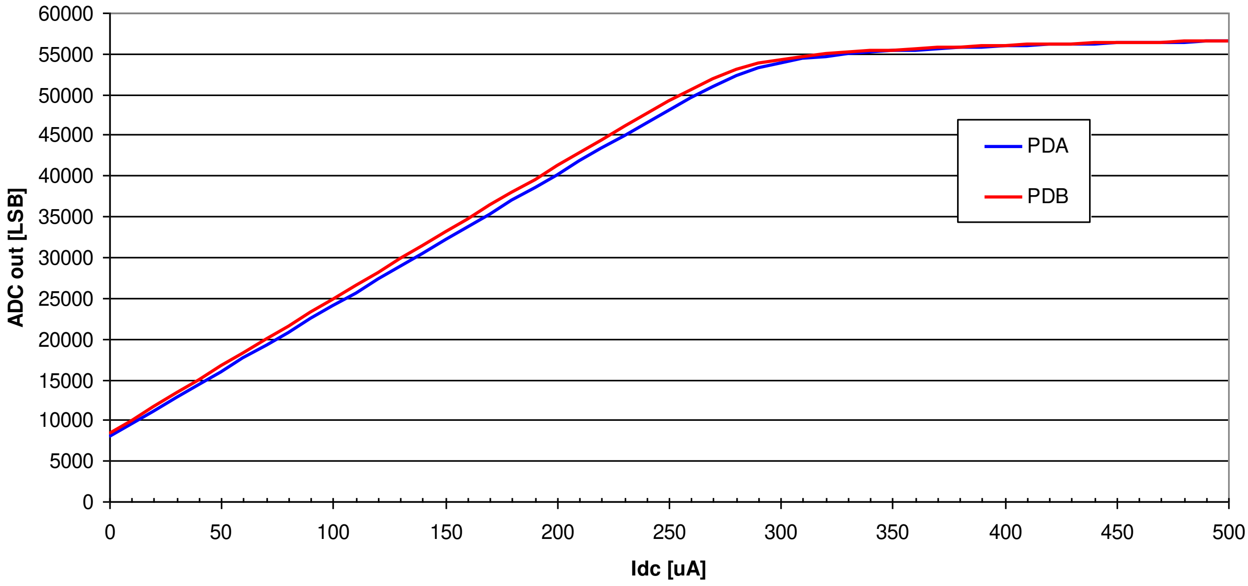


Figure 3: Typical ActiveLight channel DC measurement characteristics for both channels A and B

9.1.2. ActiveLight Channel DC Light compensation

Under certain operating conditions, the spectral sensitivity of some photodiodes is not constant and varies with the amount of (infrared) dc-light received. For the ActiveLight measurements this means that the ActiveLight signal can change rapidly if the sensor experiences highly changing sunlight conditions, even if all other conditions are constant. This results in reduced ActiveLight signal sensitivity of the system under changing dc-light conditions.

The variation of the ActiveLight signals as a function of DC-light can be partially compensated by automatically adapting the amplitude of the sensors' transmitted infrared light pulses for ActiveLight measurement.

In order to make the system as flexible as possible, the compensation can be adapted to different photodiode types by definition of the compensation characteristics as a piecewise linear curve like described in Figure 4. The values of the 5 corner points of the curve can be defined by the corresponding 4-Bit words PD_COMP_ICx<3:0> (x = 1..5) in the register maps, see section 9.4. The PD light compensation can be enabled by setting the EN_PDCOMP bit to "1".

In order to calculate the decimal values PD_COMP_ICx<3:0> (x = 1..5) for a certain photodiode, one has to measure the relative ActiveLight signal levels p_x at 5 different DC light levels I_{amb_x} while the EN_PDCOMP is set to "0" (a calculation example is given below, where $A@Iamb\_x$ is the measured ActiveLight signal at DC light signal I_{amb_x}):

p_0 = pulse level at (I_{amb_0} = 0) = 1 (this is the 100% reference)

p_1 = pulse level at (I_{amb_1} = 10uA) = e.g. 0.97440 = $\frac{A@Iamb\_0-2^{15}}{A@Iamb\_1-2^{15}}$

p_2 = pulse level at (I_{amb_2} = 45uA) = e.g. 0.94224 = $\frac{A@Iamb\_0-2^{15}}{A@Iamb\_2-2^{15}}$

p_3 = pulse level at (I_{amb_3} = 150uA) = e.g. 0.91556 = …
p_4 = pulse level at (I_{amb_4} = 500uA) = e.g. 0.89858 = …
p_5 = pulse level at (I_{amb_5} = 900uA) = e.g. 0.89477 = …

Based on these relative ActiveLight pulse levels, one can calculate the following parameters (x = 1..5):

$$r_{comp\_i} = 3 \cdot 10^{-5}(1-p_x)$$

	y_{comp_1}				1.285714	-0.28571	0	0	0				r_{comp_1}	
	y_{comp_2}				-1.28571	1.714286	-0.42857	-1.8E-17	1.78E-17				r_{comp_2}	
	y_{comp_3}		=		0	-1.42857	1.857143	-0.42857	-7.9E-17		•		r_{comp_3}	
	y_{comp_4}				0	0	-1.42857	2.678571	-1.25				r_{comp_4}	
	y_{comp_5}				0	0	0	-2.25	2.25				r_{comp_5}	

For the calculation example, we get the following values:

$$\begin{bmatrix} r_{comp\_1} \\ r_{comp\_2} \\ r_{comp\_3} \\ r_{comp\_4} \\ r_{comp\_5} \end{bmatrix} = \begin{bmatrix} 7.68E-07 \\ 1.73E-06 \\ 2.53E-06 \\ 3.04E-06 \\ 3.16E-06 \end{bmatrix}$$

The settings PD_COMP_ICx<3:0> (x = 1..5) can be derived from the y_{comp_x} (x = 1..5) as follows:

PD_COMP_IC1[3:0] = round ($\frac{y_{comp\_1}}{0.4 \times 0.132\ 10^{-6}}$, 0)

PD_COMP_IC2[3:0] = round ($\frac{y_{comp\_2}}{0.4 \times 0.165\ 10^{-6}}$, 0)

PD_COMP_IC3[3:0] = round ($\frac{y_{comp\_3}}{0.4 \times 0.334\ 10^{-6}}$, 0)

PD_COMP_IC4[3:0] = round ($\frac{y_{comp\_4}}{0.4 \times 0.334\ 10^{-6}}$, 0)

PD_COMP_IC5[3:0] = round ($\frac{y_{comp\_5}}{0.4 \times 0.180\ 10^{-6}}$, 0)

For the calculation example, this means:

PD_COMP_IC1[3:0] = 9dec
PD_COMP_IC2[3:0] = 14dec
PD_COMP_IC3[3:0] = 7dec
PD_COMP_IC4[3:0] = 5dec
PD_COMP_IC5[3:0] = 3dec

These values can be written inside the corresponding registers, see section 9.4. When the PD compensation is enabled (EN_PDCOMP = "1"), the compensation will modulate the LED current of the ActiveLight channels.

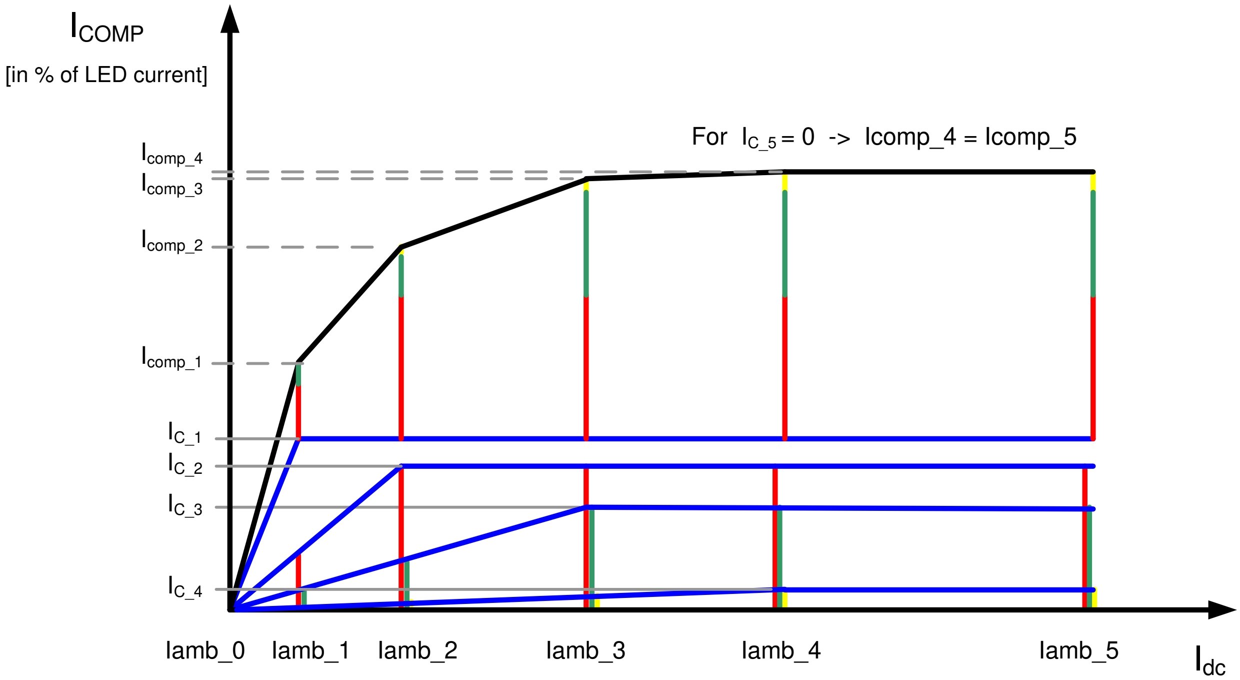


Figure 4: Example of a compensation curve I_{COMP} for I_{C_5}=0. The dc-currents of the corner points are fixed in the design and cannot be influenced. The compensation components I_{C_1}...I_{C_5} are defined by the registers DC_COMP_IC1...5 with 4 bits each. The resulting compensation characteristics are shown in the black graph.

9.1.3. Ambient Light Sensor

9.1.3.1. Normal Operation

The ambient light detection system of the MLX75030 consists of two independent channels C and D and an on-chip controllable dedicated ground pin GNDAMB. GNDAMB should not be directly connected to GND. An external photodiode is connected in between each channel and GNDAMB.
The ambient light signal is low pass filtered on chip.
The signal of a 1ms switched-capacitor filters is sampled by the ADC (on request by an SPI command, each 2.5ms), where it is converted into a 16bit digital word.

The total input stage, this means from the external diode up to the 1ms filter, has a cut-off frequency at ~160Hz. Sampling this output every 2.5ms, commanded by SPI, would make a sample rate of 400Hz, which well above the Nyquist frequency of the present frequency content of 160Hz.

Within the specified input current range the ambient input stages bias the external photodiodes with > 0V in normal operation.

9.1.3.2. Calibration and temperature compensation

The output of each ambient channel has a strong temperature dependence and a slight process dependence that can be compensated at run time. This is shown in following equation (channel x, where x = C or D):

$$I_x = \left(1 + TC_{Iref}\,\Delta T\right)\left(1 + \alpha \frac{O_x}{300^2}\Delta T\right) e^{\alpha\left(\frac{ambout_x - 2^{15}}{T}\right) + \beta} \qquad (1)$$

- I_x: calculated input light value
- $ambout_x$: 16-bit ADC converted value of the ambient channel
- TC_{Iref}: temperature coefficient of the reference current (typ. Value = +375ppm/K)
- O_x: offset of the measurement (digital value)
- α_x, β_x: calibration values for channel x (see below)

During calibration at least 2 light levels (I_{x1} and I_{x2}) have to be supplied to the target ambient channel (x) with its photodiode at the same known temperature T. The closer these values are chosen to the range used in application, the more accurate the final result will be. During the setting of these light levels, the output of ambient channel x: $ambout_{x1}$ and $ambout_{x2}$ are measured. This results in 2 equations and 2 unknowns: α_x and β_x. Both unknowns can be calculated from following formulas:

$$\alpha = \frac{T \ln\left(\frac{I_1}{I_2}\right)}{ambout_1 - ambout_2} \quad \text{and} \quad \beta = \ln\left(\frac{I_1}{1}\right) - \alpha\left(\frac{ambout_1 - 2^{15}}{T}\right) \qquad (2)$$

Note that these 2 values automatically correct any gain error of the connected photodiode and used lens system.

9.1.3.3. Diagnostics Mode Operation

In diagnostics mode, the status of the external photodiodes is checked. The following checks are performed for each ambient light channel X where X is C or D:

- X disconnected
- GNDAMB disconnected
- X shorted to GNDA/GNDD/GNDAMB
- X shorted to VCCA/VCCD
- GNDAMB shorted to GNDA/GNDD
- GNDAMB shorted to VCCA/VCCD
- X shorted to other ambient light channel

Note that in spite of the ability to detect any error by the ambient diagnostics, an error on an ambient pin might still have other unwanted effects.

- Shorting any channel to GNDA/GNDD/GNDAMB will make the readout of the whole ambient block useless. At this time a maximum current of 14mA might be constantly pulled from the supply, independent of the amount of channels that is shorted to GNDA/GNDD/GNDAMB.
- During normal operation, node GNDAMB should be considered a ground pin. Shorting this pin to any other voltage might result in a short current of max 800mA!
- Because of such unwanted effects, a detection of an error in diagnostics mode should be followed by a disabling of the ambient channels in order to avoid disturbing the operation of other blocks in the system.
- Note that unused channels should be connected with an external resistance (~60kOhm) to GNDAMB. Doing so will avoid disturbing the other channels, but will give a constant error on the channel connected to GNDAMB.

9.1.4. Temperature Sensor

The on-chip temperature sensor measures the IC temperature. The output voltage of the sensor is converted by the 16-bit ADC. The sensor will be trimmed for the best result during the production. This trimming value is not applied to the temperature sensor internally, but is available to the customer through two on-chip registers Calib1 and Calib2, see 9.4.11. The Calib1 register contains the slope of the temperature curve in LSB/K. The Calib2 register contains the offset of the curve at a defined temperature at which the chip is tested in production.

The temperature is calculated from the temperature readout (*tempout*) and the gain and offset calibration data (calibration data measured at 30°C) according to the formula:

$$T_K = 303.15K + \frac{\left(11775 + 67\,(calib2 - 32)\right) - tempout}{67 + (calib1 - 16)} \quad \text{K}$$

or in °C:

$$T = 30°\text{C} + \frac{\left(11775 + 67\,(calib2 - 32)\right) - tempout}{67 + (calib1 - 16)} \quad °\text{C}$$

Where:

- tempout: digital temperature readout (16 Bit)
- calib1: contents of calib1 register (5 Bit)
- calib2: contents of calib2 register (6 Bit)

9.1.5. DAC

For active light sensor applications, the MLX75030 DAC has been designed to have the following features:
To generate a pulse voltage signal from 1mV to 1V, so that LED current driven by LED driver can be 1mA to 1A if a 1Ω shunt resistor is used between pins 18 and 19. After controlling and slewing circuitry, the final output voltage over external shunt resistor is like in Figure 6.

DAC piece (2MSBs B[7:6])	Steps each piece (6LSBs B[5:0])	step size for 1 bit (V)	Range covered (V)	Range start (V)	Range end (V)
00	64	1.00E-04	6.40E-03	1.05E-03	7.35E-03
01	64	5.00E-04	3.20E-02	7.65E-03	3.92E-02
10	64	2.50E-03	1.60E-01	4.07E-02	1.98E-01
11	64	1.25E-02	8.00E-01	2.06E-01	9.93E-01

Table 11 : The DAC voltage values based DAC codes (B[7:6]) can refer to the following table

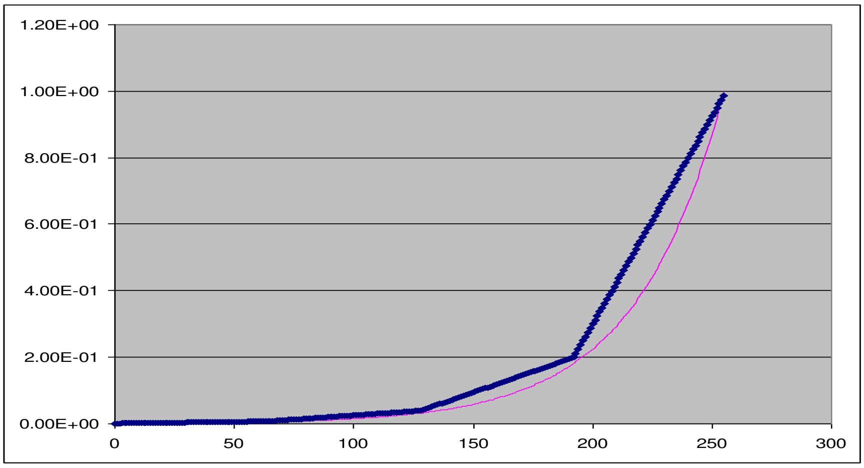


Figure 5 : Piece Wise Linear DAC voltage VS DAC codes

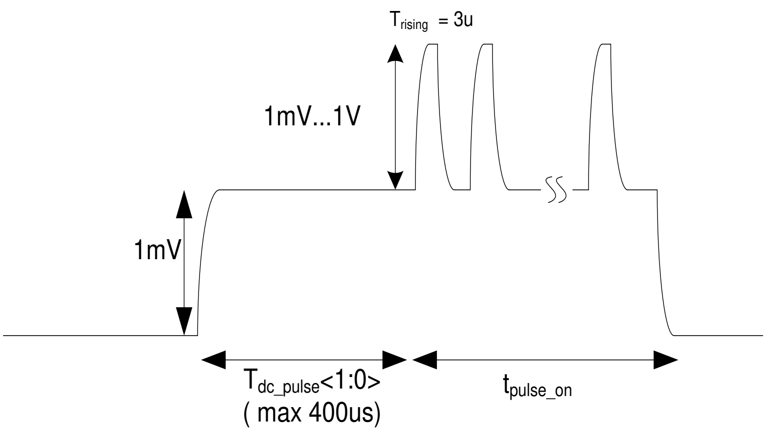


Figure 6: Vshunt waveform

9.1.6. LED Driver

LED driver will set the DAC voltage on external shunt resistor by a closed regulation loop.

9.1.7. POR

The Power On Reset (POR) is connected to voltage supply.
The POR cell generates a reset signal (high level) before the supply voltage exceeds a level from 2.7V.
The cell contains a hysteresis of 100mV.

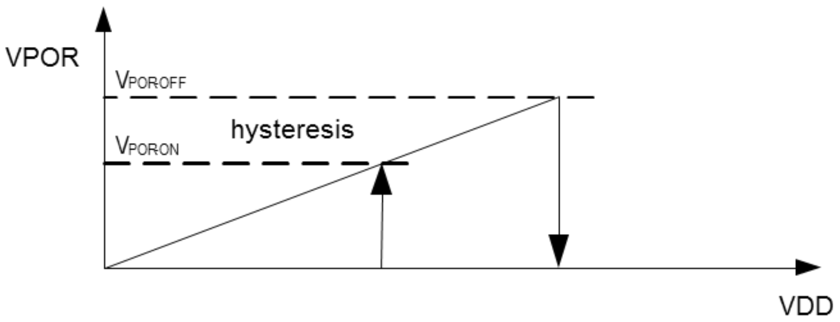


Figure 7: POR sequence

9.2. SPI

9.2.1. General Description of SPI Interface

After power-on, the sensor enters a reset state (invoked by the internal power-on-reset circuit). A start-up time $t_{startup}$ after power-on, the internal reference voltages have become stable and a first measurement cycle can start. To indicate that the start-up phase is complete, the *DR* pin will go high (*DR* is low during the start-up phase).

The control of this sensor is completely SPI driven. For each task to be executed, the proper command must be uploaded via the SPI. The SPI uses a four-wire communication protocol. The following pins are used:

- ***CS***: when *CS* pin is low, transmission and reception are enabled and the *MISO* pin is driven. When the *CS* pin goes high, the *MISO* pin is no longer driven and becomes a floating output. This makes it possible that one micro-processor takes control over multiple sensors by setting the *CS* pin of the appropriate sensor low while sending commands. The idle state of the chip select is high.
- ***SCLK***: clock input for the sensor. The clock input must be running only during the upload of a new command or during a read-out cycle. The idle state of the clock input is high.
- ***MOSI***: data input for uploading the different commands and the data that needs to be written into some registers. The idle state of the data input is low.
- ***MISO***: data output of the sensor.

A SPI timing diagram is given in Figure 8. This is the general format for sending a command. First the *CS* pin must be set low so that the sensor can accept data. The low level on the *CS* pin in combination with the first rising clock edge is used to start an internal synchronization counter that counts the incoming bits. Data on the *MOSI* pin is clocked in at the rising clock edge. Data on the *MISO* pin is shifted out during the falling clock edge. Note that the tri-state of the *MISO* pin is controlled by the state of *CS*.
After uploading a command, the *CS* pin must be set high for a minimum time of t_{cs_inter} in order to reset the internal synchronization counter and to allow new commands to be interpreted.

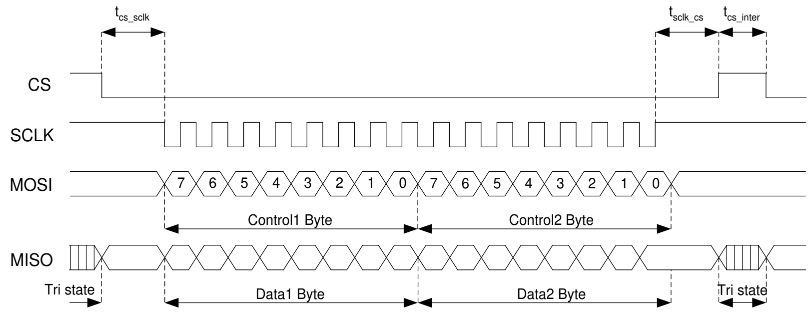


Figure 8 : SPI Timing Diagram for 2 byte instructions

The basic structure of a command consists of 2 bytes: the Control1 Byte and the Control2 Byte that are uploaded to the device and the Data1 Byte and the Data2 Byte that are downloaded to the micro-controller. Exceptions are the commands needed to read and write the user registers (WR/RR). These commands need 3 bytes.
The timing diagram is given in Figure 9.

All data transfer happens with MSB first, LSB last. Referring to Figure 8 and Figure 9 : within a byte, bit 7 is always defined as the MSB, bit 0 is the LSB. This applies to all data transfers from master to slave and vice versa.

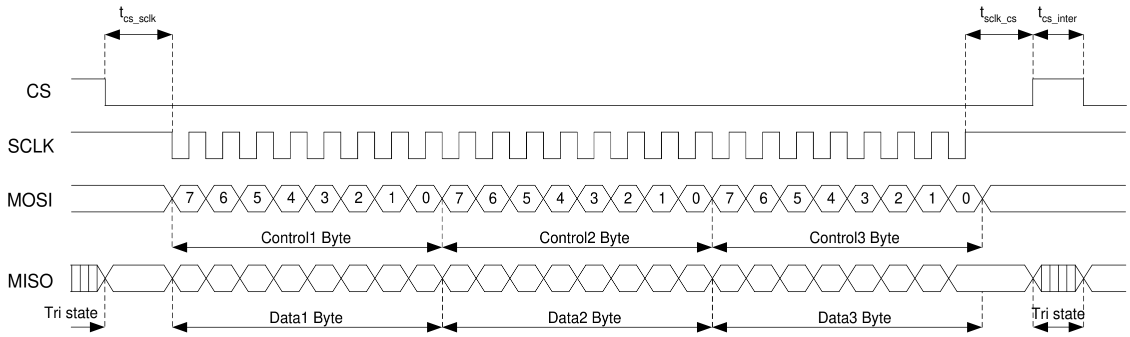


Figure 9 : SPI Timing Diagram for 3 byte instructions

The MSB of the Control1 Byte (bit 7) is a command token: setting this bit to 1 means that the Control1 Byte will be interpreted as a new command. If the MSB is 0, the next bits are ignored and no command will be accepted. The idle command has a Control1 Byte of 0x00. The command type (chip reset, power mode change, start measurements, start read-out, read/write register) is selected with the next bits 6..0 of the Control1 Byte.
The Control2 Byte consists of 0x00, to allow clocking out the Data2 Byte. The Data2 Byte contains always the Ctrl1 Byte that was uploaded. Thus the micro-controller can check that the Data2 Byte is an exact replica of the Ctrl1 Byte, to verify that the right command is uploaded to the device.

The Data1 Byte contains some internal status flags to allow checking the internal state of the device.
The internal status flags are defined in the table below.
See section 9.3 for more information concerning the operation of the status flags.

Status flag	Status when bit is set	Status when bit is clear
Bit 7 (MSB)	Previous Command was invalid	Previous Command was valid
Bit 6..5	Power State: 11 = (reserved) 10 = Normal Running Mode 01 = Stand-by State 00 = Sleep State	
Bit 4	Sleep Request was sent	No Sleep Request available
Bit 3	Standby Request was sent	No Standby Request available
Bit 2	Device is in TestMode	Device is not in TestMode
Bit 1	Internal Oscillator is enabled (Standby Mode or Normal Running Mode)	Internal Oscillator is shut down (Sleep Mode)
Bit 0 (LSB)	Critical Error occurred	No Error is detected

Table 12 : Internal Status Flags as given in the Data1 Byte

Table 13 : Instruction set of the Active light sensor summarizes the instruction set of the sensor.
A detailed explanation of these different commands is given in Section 9.2.2.

Symbol	Command Description	Control1 Byte	Control2 Byte	Control3 Byte
NOP	Idle Command	0000 0000	0000 0000	N/A
CR	Chip Reset	1111 0000	0000 0000	N/A
RSLP	Request Sleep	1110 0001	0000 0000	N/A
CSLP	Confirm Sleep	1010 0011	0000 0000	N/A
RSTBY	Request Standby	1110 0010	0000 0000	N/A
CSTBY	Confirm Standby	1010 0110	0000 0000	N/A
NRM	Normal Running Mode	1110 0100	0000 0000	N/A
SM	Start Measurement	1101 $R_2R_1R_0T$	$M_6..M_3$ $M_2M_1M_0P$	N/A
SD	Start Diagnostics	1011 0000	$M_6..M_3$ $M_2M_1M_0P$	N/A
RO	Start Read-Out	1100 0011	0000 0000	N/A
WR	Write Register	1000 0111	$D_7..D_0$	$A_3..A_0$ $P_1P_0$00
RR	Read Register	1000 1110	$A_3..A_0$ 0000	0000 0000

Table 13 : Instruction set of the Active light sensor

Besides the above instruction set, there are some test commands available for production test purposes.
To prevent unintentional access into these test modes, it requires multiple commands before the actual test mode is entered.

An overview of modes in which the device can operate is shown in Figure 10 : State Diagram of the MLX75030below. It also indicates which commands are available in the different operation modes.

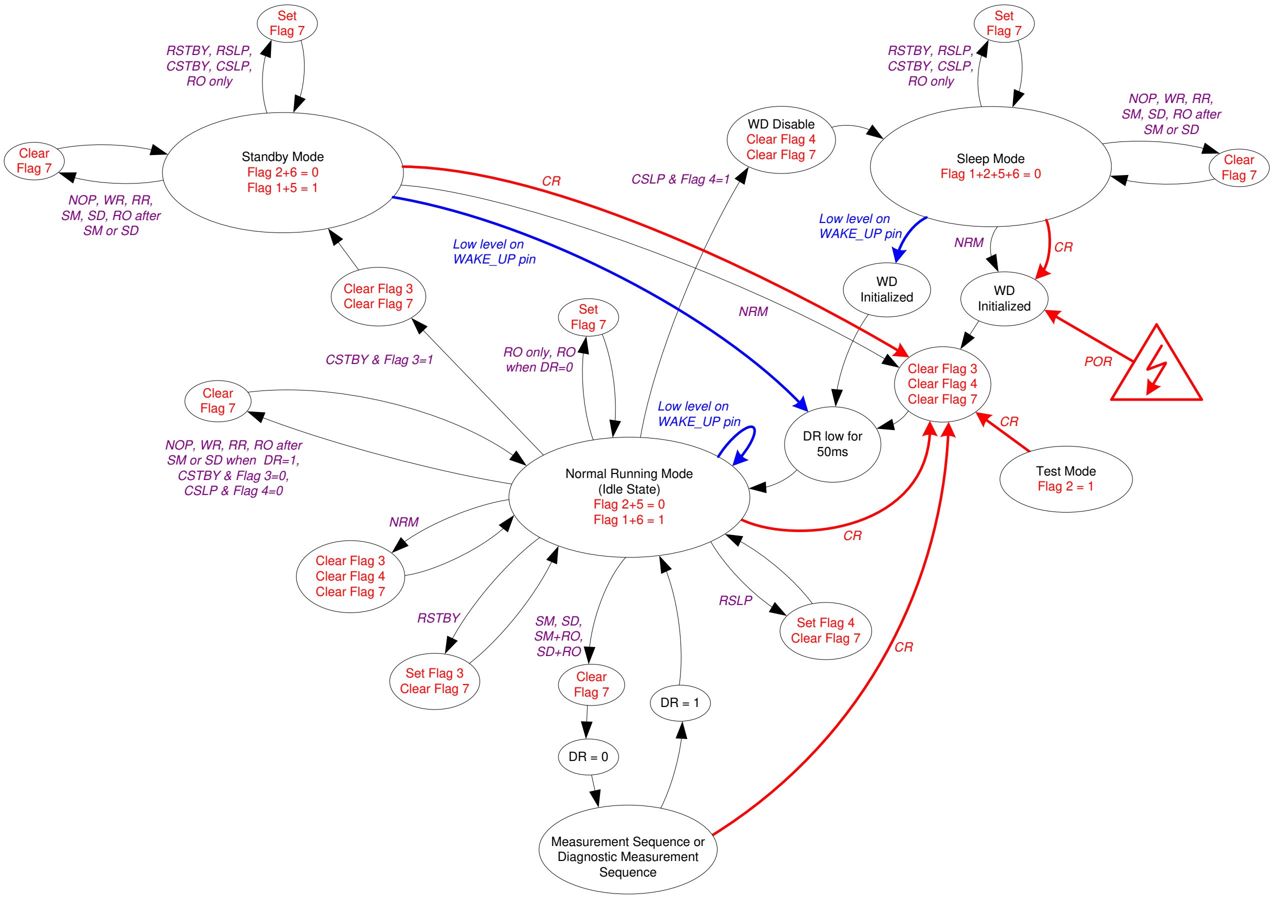


Figure 10 : State Diagram of the MLX75030

9.2.2. Detailed Explanation of SPI Instruction Words

9.2.2.1. NOP – Idle Command

The Idle Command can be used to read back the internal status flags that appear in the Data1 Byte.
The state of the device is not changed after the NOP command is uploaded.

9.2.2.2. CR – Chip Reset Command

After upload of a Chip Reset command, the sensor returns to a state as it is after power-up (Normal Running Mode) except for the watchdog counter, the state of the *MR* line and the contents of the 'Rst' register. The watchdog counter, the 'Rst' register and the state of the *MR* line will not be influenced by a CR command.

The CR command can be uploaded at any time, even during a measurement or a read-out cycle, provided that the internal synchronization counter is reset. This is done by setting the *CS* pin high for at least a time t_{cs_inter}.

When a CR command is uploaded during sleep mode resp. standby mode, the device goes automatically into normal running mode. Note that this requires a time t_{wakeup_slp} resp. t_{wakeup_stby} before the internal analog circuitry is fully set up again.

Right after upload of a CR command, the *DR* pin will go low during a time $t_{startup}$. Once the wake-up/reset phase is complete, the *DR* pin will go high.

9.2.2.3. RSLP/CSLP – Request Sleep/Confirm Sleep

To avoid that the slave device goes unintentionally into sleep mode, the master has to upload two commands. First a RSLP (Request Sleep) shall be uploaded, then the slave sets bit 4 of the internal status flag byte high. The master has to confirm the sleep request by uploading a CSLP (Confirm Sleep). Afterwards the slave will go into Sleep Mode, hereby reducing the current consumption.

The status flag can be cleared by uploading a CR command or a NRM command.
Note that uploading a Chip Reset makes the device switching into normal running mode.

When the device is operating in Sleep Mode, the *WAKE_UP* pin will be monitored. A falling edge on *WAKE_UP* will wake up the device and will switch it into Normal Running Mode.

When the device is operating in Sleep Mode, the *WT* pin will be monitored. If a falling edge is detected, the Critical Error flag in the Internal Status Flag Byte will be set high and the corresponding bit in the 'Err' register will be set high (refer also to Sections 9.3 and 9.4.7).

Note that no pull-up or pull-down resistor is foreseen on the *WAKE_UP* pin. To avoid that parasitic spikes can wake up the device, the *WAKE_UP* input is debounced (typical debounce time is in the range of 2µs). The low time on the *WAKE_UP* pin should be at least a time t_{wu_l}.

The state of the DR pin will not be changed when going into Sleep Mode. However, after a wake-up event the DR pin is set low during a time t_{wakeup_slp}.

9.2.2.4. RSTBY/CSTBY - Request Standby/Confirm Standby

To put the device in Standby Mode, a similar system is used: the master shall send the RSTBY command, requesting the slave to go into Standby Mode. The slave device sets bit 3 of the internal status flag byte high, indicating that it wants to go into standby. The master has to confirm this by sending the CSTBY byte.

The status flag can be cleared by uploading a CR command or a NRM command.
Uploading a Chip Reset makes the device switching into normal running mode.

When the device is operating in Standby Mode, the *WAKE_UP* pin will be monitored. A falling edge on *WAKE_UP* will wake up the device and will switch it into Normal Running Mode.

Note that no pull-up or pull-down resistor is foreseen on the *WAKE_UP* pin. To avoid that parasitic spikes can wake up the device, the *WAKE_UP* input is debounced (typical debounce time is in the range of 2µs). The low time on the *WAKE_UP* pin should be at least a time t_{wu_l}.

The state of the DR pin will not be changed when going into Standby Mode. However, after a wake-up event the DR pin is set low during a time t_{wakeup_stby}.

9.2.2.5. NRM – Normal Running Mode

The NRM command shall be used to wake up the device from Sleep Mode, or to go from Standby into Normal Running Mode. This requires a time t_{wakeup_slp} resp. t_{wakeup_stby} before the internal analog circuitry is fully set up again. The NRM will also clear the Sleep Request or Standby Request flag.

When the NRM command is uploaded during normal running mode, the state of the device will not be influenced, except when the Sleep Request or Standby Request flag was set high due to a RSLP or RSTBY command. In this case, the Sleep Request or Standby Request flag will be cleared; the state of the DR pin will not change.

9.2.2.6. SM – Start Measurement

The SM command is used to start up measurement cycles. Several types of measurements can be selected with the measurement selection bits M_6..M_0 in the Control2 Byte:

- M_6: setting this bit high enables the temperature measurement
- M_5: setting this bit high enables the read-out of the two ambient light channels
- M_4: setting this bit high enables the DC light measurement in the active light channel(s)
- M_3: setting this bit high fires LED A
- M_2: setting this bit high fires LED B
- M_1: setting this bit high enables the active light measurement in channel A
- M_0: setting this bit high enables the active light measurement in channel B

A typical timing diagram is given in Figure 11. After uploading the SM command, the measurement cycle is started as soon as the *CS* pin is set high. The ADC starts converting all the needed analog voltages and stores the digital values in registers. A time t_{cs_dr} after *CS* is set high, the state of the *DR* pin goes low. A time t_{dr} after *DR* was set low, the state of the *DR* pin becomes high, indicating that all measurements are completed and that the resulted data is available for read-out (read-back of the stored data in the registers). This time can be up to 231.84us, if an internal autozeroing process is under execution and needs to be finished.

Table 14 : Example measurement execution times tdr gives an overview of some execution times t_{dr} for the basic types of measurements.

Measurement Type	Min. t_{dr} (µs)	Max. t_{dr} (µs)
Temperature measurement	269	298
Ambient light measurements on all channels C and D	388	430
Active light measurements on channels A & B, with 32 pulses, pulse frequency of 48.1kHz, Tdem=6us, Tdc_pulse=400us	1513	1673
DC + Active light measurements on channels A & B, with 32 pulses, pulse frequency of 48.1kHz, Tdem=6us, Tdc_pulse=400us	1811	2002
Temperature measurement + Ambient light measurements on all channels C & D + DC + Active light measurements on channels A & B, with 32 pulses, pulse frequency of 48.1kHz, Tdem=6us, Tdc_pulse=400us	2079	2299

Table 14 : Example measurement execution times t_{dr}

__Note__ that the DR pin can be used as an interrupt for the master device as it indicates when a read-out cycle can be started.

__Note__ that measurement execution of ActiveLight measurement only is not allowed. ActiveLight measurements must always be done with Ambient Light measurements.

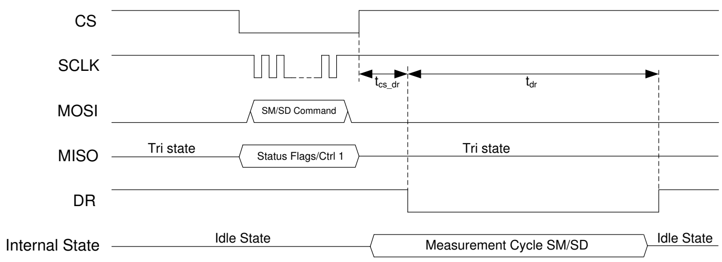


Figure 11 : Timing Diagram of a Measurement Cycle

The SM command contains 3 option bits $R_2R_1R_0$. These bits set the polarity of the anti-aliasing filters, the switched capacitors low pass filters and the ADC input buffer in active light channels A & B:

- R2: this bit inverts the op-amp in the anti-aliasing filter. The output will change from (Signal + Offset_opamp_aa) to (Signal - offset_opamp_aa). In this way, by processing 2 measurements with inverted R2 bits, the offset of the AA filter can be cancelled.
- R1: Inversion of the offset of active light_sclp_filter. The output will change from (Signal + Offset_opamp_sclp) to (Signal - offset_opamp_sclp). In this way, by processing 2 measurements with inverted R1 bits, the offset of the SCLP filter can be cancelled.
- R0: Inversion of the offset of the ADC_buffer. The output will change from (Signal + Offset_opamp_buf) to (Signal - offset_opamp_buf). In this way, by processing 2 measurements with inverted R0 bits, the offset of the SCLP filter can be cancelled.
- T: this bit replaces the light pulses by internal current pulses during the active light measurements.

The SM command contains an option bit T. If this bit is set to 0, normal active light measurements are performed (i.e. the external LEDs are fired and the active light channels A and/or B are measured). If this bit is set to 1, no LEDs are fired, but internal test pulses are applied to channels A and/or B. The internal test pulses can be influenced in amplitude by the bits DACA7 and DACA6. Limits for ADC outputs of the TIA test pulses are shown in Table 15 : Current levels for active light test mode.

DACA7	DACA6	I_Testpulse [uA]
0	0	5
0	1	13
1	0	21
1	1	29

Table 15 : Current levels for active light test mode

In the Control2 byte an even parity bit P is foreseen. The parity bits calculation is based on the measurement selection bits $M_6..M_0$. If the number of ones in the given data set $[M_6..M_0]$ is odd, the even parity bit P shall be set to 1, making the total number of ones in the set $[M_6..M_0, P]$ even.
The SPI invalid flag will be set when the parity bit does not correspond to the calculated parity bit.

After upload of a SM/SD command, no other commands will be accepted till *DR* is high. This is done to avoid too much disturbances in the analog part. Once *DR* is high, the next command will be accepted. An exception however is the Chip Reset command. This will always be accepted.

Note that none of the SM/SD commands are available in Standby Mode.

9.2.2.7. RO – Start Read-Out

When the state of the *DR* pin changed into a high state, the measurement data is available for read-out. The RO command shall be uploaded to start a read-out cycle and to start reading out the data that was stored in the internal registers.

To make sure that no memory effects can occur, all data registers are cleared at the end of each read-out cycle.

A typical timing diagram is given in Figure 12 below:

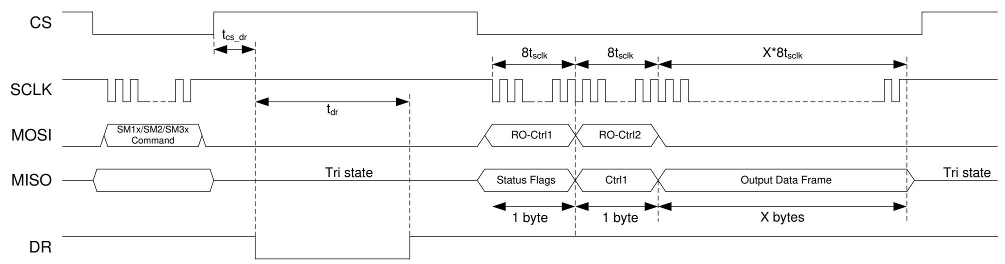


Figure 12 : Timing diagram for Read-Out

The data that appears on the *MISO* pin depends on the type of measurement that was done (i.e. it depends on the command that was uploaded: SM/SD and the selected measurement bits $M_6..M_0$).

The table below shows the Output Data Frame when all measurements are selected :

Data Byte Number	Output Data Frame Contents	Comments
Byte 3	Temperature (8 MSB)	Depends on M_6
Byte 4	Temperature (8 LSB)	Depends on M_6
Byte 5	Ambient light channel C measurement (8 MSB)	Depends on M_5 + on EN_CH_C
Byte 6	Ambient light channel C measurement (8 LSB)	Depends on M_5 + on EN_CH_C
Byte 7	Ambient light channel D measurement (8 MSB)	Depends on M_5 + on EN_CH_D
Byte 8	Ambient light channel D measurement (8 LSB)	Depends on M_5 + on EN_CH_D
Byte 9	not used	
Byte 10	not used	
Byte 11	DC measurement of IR channel A, before the active light burst measurement (8 MSB)	Depends on M_4
Byte 12	DC measurement of IR channel A, before the active light burst measurement (8 LSB)	Depends on M_4
Byte 13	DC measurement of IR channel B, before the active light burst measurement (8 MSB)	Depends on M_4
Byte 14	DC measurement of IR channel B, before the active light burst measurement (8 LSB)	Depends on M_4
Byte 15	Active light burst measurement of IR channel A (8 MSB)	Depends on M_1 + LED selection depends on M_3/M_2
Byte 16	Active light burst measurement of IR channel A (8 LSB)	Depends on M_1 + LED selection depends on M_3/M_2
Byte 17	Active light burst measurement of IR channel B (8 MSB)	Depends on M_0 + LED selection depends on M_3/M_2
Byte 18	Active light burst measurement of IR channel B (8 LSB)	Depends on M_0 + LED selection depends on M_3/M_2
Byte 19	DC measurement of IR channel A, after the active light burst measurement (8 MSB)	Depends on M_4
Byte 20	DC measurement of IR channel A, after the active light burst measurement (8 LSB)	Depends on M_4
Byte 21	DC measurement of IR channel B, after the active light burst measurement (8 MSB)	Depends on M_4
Byte 22	DC measurement of IR channel B, after the active light burst measurement (8 LSB)	Depends on M_4
Byte 23	CRC (8 bit)	Output always

Table 16 : SM Output Data Frame

Note : When certain measurements are disabled, the corresponding data bytes are omitted from the Output Data Frame.

Cyclic Redundancy Check Calculation

In all Output Data Frames, a CRC byte is included as last byte. This byte provides a way to detect transmission errors between slave and master. An easy method to check if there were no transmission errors is to calculate the CRC of the whole read-out frame as defined in previous tables. When the calculated CRC results in 0x00, the transmission was error free. If the resulting CRC is not equal to zero, then an error occurred in the transmission and all the data should be ignored. For more information regarding the CRC calculation, please refer to section 9.8.

9.2.2.8. SM+RO - Start Measurement combined with Read-Out

If after upload of the SM command, extra clocks are given (without putting *CS* high!), the data stored in the internal registers will appear on the *MISO* pin. At the end of the read-out phase the internal registers will be cleared to avoid memory effects in the next read-outs.
The newly uploaded SM command will be executed after the read-out, when the *CS* pin goes high.

The two figures below show the difference between the two modes of operation :

- Figure 13 : Separated SM - RO (X value is defined in Figure 6)shows the operation with separate SM and RO commands. After upload of a SM command, the measurement cycle will start and the internal registers will be filled. Once the *DR* pin is high, the RO command can be uploaded to start the read-out cycle. All data of the internal registers will be transferred and at the end of the read-out the registers will be cleared.

- Figure 14 : Combined SM - RO (X value is defined in Figure 6) shows the operation with the combined SM and RO. First one has to upload a SM command to start a measurement. The data is available for read-out when the *DR* pin goes high. Instead of uploading a RO command, a SM command can be uploaded again to combine read-out and the start of the next measurement cycle. If extra clocks are given after upload of the SM command, the data of the internal registers becomes available on the *MISO* pin. Note that the *CS* pin shall not be set high until the read-out is finished. Once *CS* pin goes high, the *DR* pin is set low and a new measurement cycle will be started. A time t_{dr} later the *DR* pin goes high to indicate that the data is available.

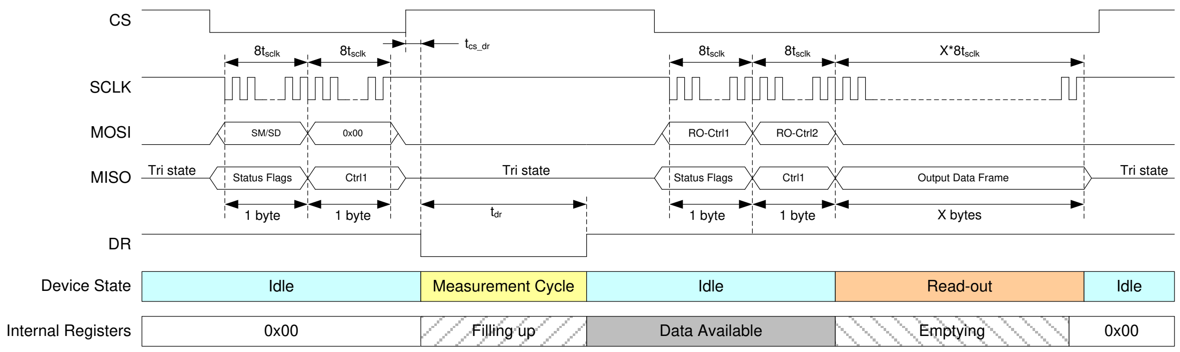


Figure 13 : Separated SM - RO (X value is defined in Figure 6)

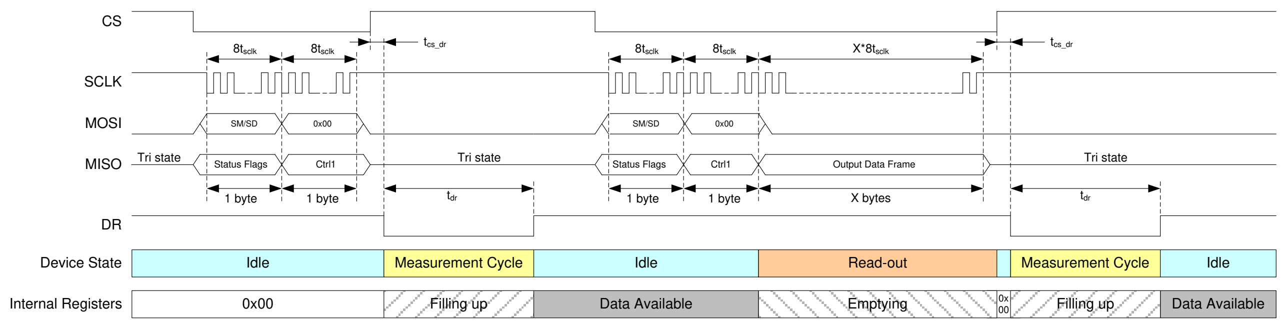


Figure 14 : Combined SM - RO (X value is defined in Figure 6)

9.2.2.9. WR/RR – Write/Read Register

The slave contains several user registers that can be read and written by the master.
The WR and RR commands are used for that.

The WR command writes the contents of an 8-bit register addressed by bits $A_{3..0}$ with data $D_{7..0}$. Data is sent to the device over the *MOSI* pin. Control2 Byte contains the 8 bit data that shall be written into the target register. Control3 Byte contains the address of the target register.
The WR command is defined in the table below:

Control1 Byte	Control2 Byte	Control3 Byte
1000 0111	$D_7D_6D_5D_4$ $D_3D_2D_1D_0$	$A_3A_2A_1A_0$ $P_1P_0$00
$D_7D_6D_5D_4$ $D_3D_2D_1D_0$ $A_3A_2A_1A_0$ P_1P_0	Data contents of register to be written Address of target register Parity bits (P_1 = odd parity bit, P_0 = even parity bit)	
Data1 Byte	**Data2 Byte**	**Data3 Byte**
Status Flag Byte	1000 0111	0000 0000

Table 17 : Write Register command

In order to detect some transmission errors while writing data towards the slave device, the micro-controller has to compute an odd and an even parity bit of the Control2 and the 4 MSB's of the Control3 byte and send these parity bits to the slave. The slave will check if the parity bits are valid. The data will only be written into the registers if the parity bits are correct. If the parity bits are not correct, bit 7 of the internal Status Flag Byte will be set high, indicating that the command was invalid. This can be seen when uploading a NOP command (when one is only interested in reading back the internal status flags) or during upload of the next command.
In case the parity bits were not correct, the data of the registers will not be changed.

The parity bits calculation is based on the data $D_7..D_0$ and $A_3..A_0$. If the number of ones in the given data set [$D_7..D_0$, $A_3..A_0$] is odd, the even parity bit P_0 shall be set to 1, making the total number of ones in the set [$D_7..D_0$, $A_3..A_0$, P_0] even.
Similar: if the number of ones in the given data set [$D_7..D_0$, $A_3..A_0$] is even, the odd parity bit P_1 shall be set to 1, making the total number of ones in the set [$D_7..D_0$, $A_3..A_0$, P_1] odd.

Note that the parity bits can be generated with XOR instructions: P_1 = XNOR($D_7..D_0$, $A_3..A_0$) and P_0 = XOR($D_7..D_0$, $A_3..A_0$). The odd parity bit P_1 should always be the inverse of the even parity bit P_0.

The RR command returns the contents of an 8-bit register addressed by bits $A_{3..0}$. Data is read back over the *MISO* pin. The Data1 Byte contains the Internal Status Flag byte. Data2 Byte contains the copy of the Control1 Byte. Data3 Byte contains the 8 bits of the target register.
The RR command is defined in the table below:

Control1 Byte	Control2 Byte	Control3 Byte
1000 1110	$A_3A_2A_1A_0$ 0000	0000 0000
$A_3A_2A_1A_0$	Address of target register	
Data1 Byte	**Data2 Byte**	**Data3 Byte**
Status Flag Byte	1000 1110	$D_7D_6D_5D_4$ $D_3D_2D_1D_0$
$D_{7..0}$	Data contents of register read	

Table 18 : Read Register command

Note that the WR and RR commands are commands that require 3 bytes instead of 2 bytes.

An overview of the user registers that can be accessed with WR/RR commands and more general information concerning the user registers can be found in section 9.4

9.2.2.10. SD – Start Diagnostics

The SD command will start a measurement cycle in which internal signals will be measured and converted. With this command it is possible to test some circuits in the chip and check if they are functioning as expected.

The SD command behaves in much the same way as the SM commands: instead of uploading a SM command, a SD command can be uploaded. This starts the measurement cycle and conversion of some internal signals. The pin *DR* goes high when the cycle is completed, indicating that a read-out can be started. With the RO command it is possible to read out the data and check if all the data values are within certain ranges.
After upload of a SD command, no other commands will be accepted till *DR* is high. This is done to avoid too much disturbances in the analog part. Once *DR* is high, the next command will be accepted. An exception however is the Chip Reset command. This will always be accepted. The SD command is not available in Standby Mode.

Similar to the SM command, the SD command has some measurement selection bits $M_6..M_0$ in the Control2 Byte. Different measurements can be selected with these bits:

- M_6: setting this bit high enables the ADC diagnostics
- M_5: setting this bit high enables the DAC-ADC diagnostics
- M_4: setting this bit high enables the Ambient Diode checks
- $M_3..M_0$: (reserved)

Table 19 gives an overview of some execution times t_{dr} for the basic types of measurements.

Measurement Type	Min. t_{dr} (µs)	Max. t_{dr} (µs)
ADC Diagnostics	224	249
DAC-ADC Diagnostics	91	102
Ambient Diode checks	370	410
ADC + DAC-ADC + Ambient Diode Diagnostics	680	752

Table 19: Basic Measurement Execution Times t_{dr}

If all possible measurements are selected, the Output Data Frame is defined in the table below:

Data Byte Number	Data Byte Contents after SD command	Comments
Byte 3	ADCtest0 (8 MSB)	Depends on M_6
Byte 4	ADCtest0 (8 LSB)	Depends on M_6
Byte 5	ADCtest1 (8 MSB)	Depends on M_6
Byte 6	ADCtest1 (8 LSB)	Depends on M_6
Byte 7	ADCtest2 (8 MSB)	Depends on M_6
Byte 8	ADCtest2 (8 LSB)	Depends on M_6
Byte 9	ADCtest3 (8 MSB)	Depends on M_6
Byte 10	ADCtest3 (8 LSB)	Depends on M_6
Byte 11	ADCtest4 (8 MSB)	Depends on M_6
Byte 12	ADCtest4 (8 LSB)	Depends on M_6
Byte 13	DAC-ADC Test (8 MSB)	Depends on M_5
Byte 14	DAC-ADC Test (8 LSB)	Depends on M_5
Byte 15	00000 + CD_x Ambient Diodes Detection (3 bit)	Depends on M_4
Byte 16	CRC (8 bit)	Output always

Table 20 : SD Output Data Frame
When certain measurements are disabled, the corresponding data bytes are omitted from the Output Data Frame.

ADCtest0/1/2/3/4
These measurements are AD conversions of some internal reference voltages:
- ADCtest0 is typically at 1/16 of the ADC range: ADCtest0 = 0x0E00 .. 0x1200.
- ADCtest1 is typically at 1/4=4/16 of the ADC range: ADCtest1 = 0x3E00 .. 0x4200.
- ADCtest2 is typically at 3/4=12/16 of the ADC range: ADCtest2 = 0xBE00 .. 0xC200.
- ADCtest3 is typically at 15/16 of the ADC range: ADCtest3 = 0xEE00 .. 0xF200.

ADCtest4 is similar to ADCtest0/1/2/3: an AD conversion of an internal reference voltage is made. However, an independent voltage reference is used as input for the ADC in case of ADCtest4. In the case of ADCtest0/1/2/3, the reference voltages are generated from the references used for the ADC.
The typical output for ADCtest4 will be as listed in below table:

			min	typ	max	
ADCtest4 values		@ Vs=3.0V	33400	35400	37400	LSB
		@ Vs=3.3V	30400	32400	34400	LSB
		@ Vs=3.6V	27400	29400	31400	LSB

DAC-ADC test
A DAC-ADC test measurement is performed in the following way: the DAC output is connected to the ADC input. The DAC input will be DACA<7:0> from register 'SetAH'. This DAC-input will be converted to an analog output voltage that will be converted again by the ADC to give a digital value. This digital value is given in the bytes DAC-ADC Test.

Ambient Diodes Detection
During the Diagnostics measurement, the status of the external photo diodes connected to the ambient light channel inputs is checked.
Three bits CDx are output: when the bit C is set high, an error on the photo diode channel C is present.
In a similar way, bit D indicate if errors on ambient light channels D is present or not.

9.3. Internal Status Flags

Bit 7: Previous Command invalid/valid
When an uploaded command is considered invalid, bit 7 will be set high. This bit can be read out when the next command will be uploaded. If the next command is valid, bit 7 will be cleared again.

A command is considered invalid in case:
- a command is unknown (i.e. all commands that are not mentioned in Table 13)
- the parity bit in the SM or SD command is not correct
- the parity bits in a WR command are not correct
- when a command (except the CR command) was sent during a measurement cycle (i.e. after uploading a SM/SD command, when *DR* is still low)
- when a RO command was sent when *DR* is low (at any time, i.e. not only after uploading a SM/SD command)
- if a '1' is written into one of the bits of the 'Err' register
- if an ambient measurement is requested in case all bits EN_CH_C/EN_CH_D/EN_DIAGAMB are zero

Bit 6..5: Power State, Bit 4: Sleep request, Bit 3: Standby request
The behaviour of the power state and the sleep request bits is explained in Figure 15 : Power State and Sleep Request bits. First a RSLP command is uploaded to the sensor. As a result of that, the sensor will put the status flag bit 4 (sleep request flag) high. The master can read out that flag by uploading a NOP command, or when uploading other commands.
The master can confirm to go into sleep mode by uploading a CSLP command. The request flag will be reset and the sensor will switch into sleep state. The status flag bits 6 and 5 will be set accordingly.

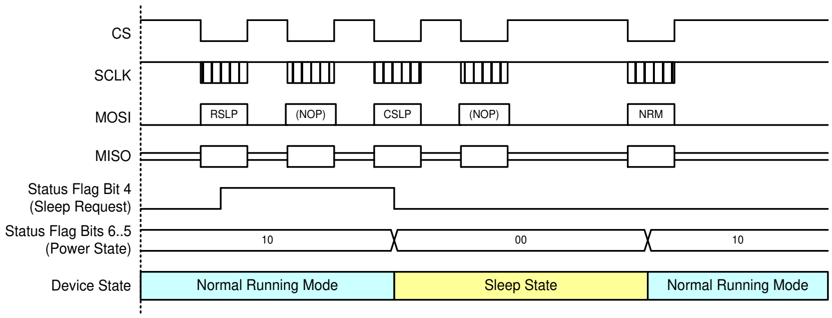


Figure 15 : Power State and Sleep Request bits

To go into standby mode, the same procedure shall be applied: uploading a RSTBY command makes the request standby flag going high. Uploading a CSTBY will make the device going into standby mode, whereby the request standby flag will be cleared and the power state bits will be set accordingly.

Bit 2: Device in TestMode/Normal Mode
To make the sensor efficiently testable in production, several test modes are foreseen to get easy access to different blocks. The status flag bit 2 indicates if the device is operating in Test Mode or Normal Mode.
If the device enters test mode by accident, the application will still work like normal. However, the status flag bit 2 will be set high. The master can take actions to get out of test mode by uploading a CR command.

Bit 1: Internal Oscillator is enabled/disabled
This bit is high when the internal oscillator is enabled. Once the RCO is shut down the bit will be set low.

Bit 0: Critical Error is detected/not detected
During each measurement cycle there is a monitoring of the voltage on critical nodes along the analog paths. When the voltage of one of these controlled nodes goes out of its normal operating range, the Critical Error Flag will be set high.

The Critical Error Flag will also be set high when a falling edge on the *WT* pin will be detected while the device is in Sleep Mode.

Following nodes are monitored:
- TIA output: when the output is clipped (either high or low), the Critical Error Flag will be set high
- Difference between DAC output and shunt-feedback
- An internal reference voltage
- Output of the common mode SC-amplifiers of the Ambient Light/Temperature Channels
- Frequency on RCO output

In case the Critical Error Flag was set high, the 'Err' register indicates which node voltages got out of their normal operating range. More info about the 'Err' register can be found in Section 9.4.7.

The Critical Error Flag remains high as long as the 'Err' register is not cleared. Once the 'Err' register is cleared, the Critical Error Flag will be cleared as well.

Note: after POR, or after wake-up from Sleep/Standby, some bits in the 'Err' register might be set. As such the Critical Error Flag might be set as well.

9.4. User Registers Overview

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SetAna	0x0	Tdem3	Tdem2	Tdem1	Tdem0	LEDDRV_HG	Tdc_pulse1	Tdc_pulse0	Unity_Gain
SetAH	0x1	DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0
SetAL	0x2	GAIN_ADJ_ AA_A2	GAIN_ADJ_ AA_A1	GAIN_ADJ_ AA_A0	BW_ADJ_ AA_A2	BW_ADJ_ AA_A1	BW_ADJ_ AA_A0	BW_SEL_ LP_A1	BW_SEL_ LP_A0
SetBH	0x3	DACB7	DACB6	DACB5	DACB4	DACB3	DACB2	DACB1	DACB0
SetBL	0x4	GAIN_ADJ_ AA_B2	GAIN_ADJ_ AA_B1	GAIN_ADJ_ AA_B0	BW_ADJ_ AA_B2	BW_ADJ_ AA_B1	BW_ADJ_ AA_B0	BW_SEL_ LP_B1	BW_SEL_ LP_B0
SetPF	0x5	NP3	NP2	NP1	NP0	EN_DCCOMP	RPF2	RPF1	RPF0
Err	0x6	-	Err6	Err5	Err4	Err3	Err2	Err1	-
Rst	0x7	DC_COMP_ IC13	DC_COMP_ IC12	DC_COMP_ IC11	DC_COMP_ IC10	-	-	TO	POR
DCComp1	0x8					DC_COMP_ IC23	DC_COMP_ IC22	DC_COMP_ IC21	DC_COMP_ IC20
DCComp2	0x9	DC_COMP_ IC33	DC_COMP_ IC32	DC_COMP_ IC31	DC_COMP_ IC30	DC_COMP_ IC43	DC_COMP_ IC42	DC_COMP_ IC41	DC_COMP_ IC40
GainBuf	0xA	-	-	-	GAIN_BUF4	GAIN_BUF3	GAIN_BUF2	GAIN_BUF1	GAIN_BUF0
Calib1	0xB	TRIM_ TC_BGI4	TRIM_ TC_BGI3	TRIM_ TC_BGI2	TRIM_ TC_BGI1	TRIM_ TC_BGI0	-	-	-
Calib2	0xC	-	-	TRIM_ TEMP5	TRIM_ TEMP4	TRIM_ TEMP3	TRIM_ TEMP2	TRIM_ TEMP1	TRIM_ TEMP0
EnChan	0xD	EN_TEMP	EN_DIAG_A	EN_DIAG_B	EN_CH_A	EN_CH_B	EN_CH_C	EN_CH_D	EN_ DIAGAMB
Tamb	0xE	DC_COMP_ IC53	DC_COMP_ IC52	DC_COMP_ IC51	DC_COMP_ IC50	-	-	Tamb1	Tamb0

Table 21. User registers overview

In the next sections, all the bits of these registers are described. The value of the register at Power-On is indicated in the line 'Init' (0 or 1 or x=unknown) and the read/write access ability is indicated in the line 'Read/Write' (R indicates Read access, W indicates Write access).

9.4.1. SetAna register

This register contains some settings of the analog chain.

	Bit	7	6	5	4	3	2	1	0
SetAna		Tdem3	Tdem2	Tdem1	Tdem0	LEDDRV_HG	Tdc_ pulse1	Tdc_ pulse0	Unity_Gain
0x0	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Init	0	0	0	0	0	1	0	1

- Tdem<3:0>: changes the demodulator delay time in the active light channel

Tdem3	Tdem2	Tdem1	Tdem0	Delay time (in µs, +/-5%)
0	0	0	0	0
0	0	0	1	0.4
0	0	1	0	0.8
0	0	1	1	1.2
0	1	0	0	1.6
0	1	0	1	2
0	1	1	0	2.4
0	1	1	1	2.8
1	0	0	0	3.2
1	0	0	1	3.6
1	0	1	0	4
1	0	1	1	4.4
1	1	0	0	4.8
1	1	0	1	5.2
1	1	1	0	5.6
1	1	1	1	6

- LEDDRV_HG: 1 = selects high gain mode of LED driver, 0 = selects low gain mode
- Tdc_pulse<1:0>: defines the time that the DC component in the active light pulse signal is enabled before the actual active light pulses start

Tdc_ pulse1	Tdc_ pulse0	Delay time (in µs, +/-5%)
0	0	50
0	1	100
1	0	200
1	1	400

- Unity_Gain: only during active light measurements: 1=ADC buffer is bypassed, 0=ADC gain stage is used (gain is set with bits GAIN_BUF<4:0> in register 'GainBuf')

9.4.2. SetAH register

This register defines the DAC level for IR channel A.

	Bit	7	6	5	4	3	2	1	0
SetAH		DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0
0x1	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Init	0	0	0	0	0	0	0	0

- DACA<7:0>: the 8 bits of the DAC level for IR channel A

9.4.3. SetAL register

This register defines the gain and cut-off frequency adjustments for IR channel A.

	Bit	7	6	5	4	3	2	1	0
SetAL		GAIN_ ADJ_ AA_A2	GAIN_ ADJ_ AA_A1	GAIN_ ADJ_ AA_A0	BW_ ADJ_ AA_A2	BW_ ADJ_ AA_A1	BW_ ADJ_ AA_A0	BW_ SEL_ LP_A1	BW_ SEL_ LP_A0
0x2	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Init	0	0	0	0	1	1	0	1

- GAIN_ADJ_AA_A<2:0>: gain adjustment of anti-aliasing filter of channel A

GAIN_ADJ_ AA_A2	GAIN_ADJ_ AA_A1	GAIN_ADJ_ AA_A0	Gain	Gain (dB)
0	0	0	2.00	6.02
0	0	1	4.29	12.64
0	1	0	6.57	16.35
0	1	1	8.86	18.95
1	0	0	11.14	20.94
1	0	1	13.43	22.56
1	1	0	15.71	23.93
1	1	1	18.00	25.11

- BW_ADJ_AA_A<2:0>: cut-off frequency adjustment of anti-aliasing filter of channel A

BW_ADJ_ AA_A2	BW_ADJ_ AA_A1	BW_ADJ_ AA_A0	3dB Cut-off Frequency (kHz)
0	0	0	18
0	0	1	20
0	1	0	22.5
0	1	1	25
1	0	0	30
1	0	1	35
1	1	0	43
1	1	1	55

- BW_SEL_LP_A<1:0>: cut-off frequency selection of low-pass filter of channel A

BW_SEL_ LP_A1	BW_SEL_ LP_A0	Cut-off Frequency (%f_0)	Cut-off Frequency (kHz @ f_0=70kHz)
0	0	≅23.5	≅16.5
0	1	≅12	≅7.8
1	0	≅5.9	≅4.2
1	1	≅3	≅2.1

9.4.4. SetBH register

This register defines the DAC level for IR channel B.

	Bit	7	6	5	4	3	2	1	0
SetBH		DACB7	DACB6	DACB5	DACB4	DACB3	DACB2	DACB1	DACB0
0x3	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Init	0	0	0	0	0	0	0	0

- DACB<7:0>: the 8 bits of the DAC level for IR channel B

9.4.5. SetBL register

This register defines the gain and cut-off frequency adjustments for IR channel B.

	Bit	7	6	5	4	3	2	1	0
SetBL		GAIN_ ADJ_ AA_B2	GAIN_ ADJ_ AA_B1	GAIN_ ADJ_ AA_B0	BW_ ADJ_ AA_B2	BW_ ADJ_ AA_B1	BW_ ADJ_ AA_B0	BW_ SEL_ LP_B1	BW_ SEL_ LP_B0
0x4	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Init	0	0	0	0	1	1	0	1

- GAIN_ADJ_AA_B<2:0>: gain adjustment of anti-aliasing filter of channel B

GAIN_ADJ_ AA_B2	GAIN_ADJ_ AA_B1	GAIN_ADJ_ AA_B0	Gain	Gain (dB)
0	0	0	2.00	6.02
0	0	1	4.29	12.64
0	1	0	6.57	16.35
0	1	1	8.86	18.95
1	0	0	11.14	20.94
1	0	1	13.43	22.56
1	1	0	15.71	23.93
1	1	1	18.00	25.11

- BW_ADJ_AA_B<2:0>: cut-off frequency adjustment of anti-aliasing filter of channel B

BW_ADJ_ AA_B2	BW_ADJ_ AA_B1	BW_ADJ_ AA_B0	3dB Cut-off Frequency (kHz)
0	0	0	18
0	0	1	20

0	1	0	22.5
0	1	1	25
1	0	0	30
1	0	1	35
1	1	0	43
1	1	1	55

- BW_SEL_LP_B<1:0>: cut-off frequency selection of low-pass filter of channel B

BW_SEL_ LP_B1	BW_SEL_ LP_B0	Cut-off Freuency (%f_0)	Cut-off Frequency (kHz @ f_0=70kHz)
0	0	≅23.5	≅16.5
0	1	≅12	≅7.8
1	0	≅5.9	≅4.2
1	1	≅3	≅2.1

9.4.6. SetPF register

This register defines the frequency settings and the number of pulses for the active light measurements.

	Bit	7	6	5	4	3	2	1	0
SetPF		NP3	NP2	NP1	NP0	EN_DC COMP	RPF2	RPF1	RPF0
0x5	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Init	0	1	0	0	0	1	0	0

- NP<3:0>: number of pulses for the active light measurements, as defined in the table below:

Bit 3 - NP3	Bit 2 - NP2	Bit 1 - NP1	Bit 0 - NP0	Number of Pulses
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
0	0	1	1	8
0	1	0	0	10
0	1	0	1	12
0	1	1	0	14
0	1	1	1	16
1	0	0	0	18
1	0	0	1	20
1	0	1	0	22
1	0	1	1	24
1	1	0	0	26
1	1	0	1	28
1	1	1	0	30
1	1	1	1	32

- EN_DCCOMP: 1 = enables the DC light compensation, 0 = disables the DC light compensation
- RPF<2:0>: frequency selection of pulses for the active light measurements, as defined below:

Bit 2 - RPF2	Bit 1 - RPF1	Bit 0 - RPF0	Frequency of Pulses (in kHz, +/-5%)
0	0	0	48.1
0	0	1	52.1
0	1	0	56.8
0	1	1	62.5
1	0	0	69.4
1	0	1	78.1
1	1	0	89.3
1	1	1	104.2

9.4.7. Err register

As described in Section 9.3 (under section 'Bit 0: Critical Error is detected/not detected'), the voltages on critical nodes are monitored continuously. When a voltage on such a critical node goes outside its operating range, the Critical Error Flag and the appropriate error bit in the 'Err' register will be set high. As such, the source of the error can be found in the 'Err' register.
The error bit remains high as long as the error condition is present, or as long as the error bit is not cleared (in case the error condition is not present anymore).

		7	6	5	4	3	2	1	0
	Bit	7	6	5	4	3	2	1	0
Err		-	Err6	Err5	Err4	Err3	Err2	Err1	-
0x6	Read/Write	R	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R
	Init	0	0	0	x**	x**	x**	0	0

The following bits are defined (0= no error detected; 1=error is detected):
- Err<7>: not implemented, read as '0'
- Err6: critical error detected on TIA output
- Err5: critical error detected on the difference between DAC output and shunt-feedback
- Err4: critical error detected on internal voltage reference: when the internal voltage reference is below 1V.
- Err3: critical error detected on one of the common mode SC-filters of the ambient light/temperature channels
- Err2: critical error detected on RCO: either a stuck-at-high or a stuck-at-low condition occurred at the output of the RCO. Note that in SLP, the error flag on the RCO will be set high.
- Err1: set to '1' when a falling edge on the *WT* pin is detected while the device is in Sleep Mode
- Err<0>: not implemented, read as '0'

*: only writing '0' is allowed. If a '1' is written, the bit value in the register will not be changed, but Bit 7 of the Internal Status Flags will be set high (Previous Command Invalid).
**: 'x' indicates that the value after POR is unknown. If the voltages of the nodes are out of range right after POR, it will be immediately reflected in the 'Err' register and the Critical Error Flag will be set. The same is valid after wake-up from Sleep/Standby.

9.4.8. Rst register

This register allows differentiation of either a POR or a reset due to a watchdog time-out + settings for the DC light compensation circuitry.

	Bit	7	6	5	4	3	2	1	0
Rst		DC_ COMP_ IC13	DC_ COMP_ IC12	DC_ COMP_ IC11	DC_ COMP_ IC10	-	-	TO	POR
0x7	Read/Write	R/W	R/W	R/W	R/W	R	R	R	R/W
	Init	0	0	0	0	0	0	0	1

- DC_COMP_IC1<3:0>: setting of the amplitude of the 1st PWL slope
- Rst<3:2>: not implemented, read as '0'
- TO: 1=a Watchdog time-out and a master reset occurred. 0=no Watchdog time-out occurred, or after Power-On, or after a falling edge at the *WT* pin
- POR: 1=a POR occurred, 0=a POR has not occurred. To detect subsequent Power-On-Resets, the POR-bit shall be cleared right after Power-On.

9.4.9. DCComp register

This register contains settings for the DC light compensation circuitry. These settings have to be calculated for the individual application (ActiveLight-channel photodiode used).

	Bit	7	6	5	4	3	2	1	0
DCComp1						DC_ COMP_ IC23	DC_ COMP_ IC22	DC_ COMP_ IC21	DC_ COMP_ IC20
0x8	Read/ Write	R	R	R	R	R/W	R/W	R/W	R/W
	Init	X	X	X	X	0	0	0	0

- DC_COMP_IC2<3:0>: setting of the amplitude of the 2nd PWL slope

	Bit	7	6	5	4	3	2	1	0
DCComp2		DC_ COMP_ IC33	DC_ COMP_ IC32	DC_ COMP_ IC31	DC_ COMP_ IC30	DC_ COMP_ IC43	DC_ COMP_ IC42	DC_ COMP_ IC41	DC_ COMP_ IC40
0x9	Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Init	0	0	0	0	0	0	0	0

- DC_COMP_IC3<3:0>: setting of the amplitude of the 3rd PWL slope
- DC_COMP_IC4<3:0>: setting of the amplitude of the 4th PWL slope

9.4.10. GainBuf register

This register contains the gain settings of the ADC input buffer. The use of this buffer is depending on bit 'Unity_Gain' in the register 'SetAna'.

	Bit	7	6	5	4	3	2	1	0
GainBuf		-	-	-	GAIN_BUF4	GAIN_BUF3	GAIN_BUF2	GAIN_BUF1	GAIN_BUF0
0xA	Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
	Init	0	0	0	1	1	0	1	0

- GainBuf<7:5>: not implemented, read as '0'
- GAIN_BUF<4:0>: defines the gain setting of the ADC input buffer

GAIN_BUF4	GAIN_BUF3	GAIN_BUF2	GAIN_BUF1	GAIN_BUF0	Gain
0	0	0	0	1	2
0	0	0	1	0	1
0	0	0	1	1	0.67
0	0	1	0	0	0.5
0	0	1	0	1	0.4
0	0	1	1	0	0.33
0	0	1	1	1	0.29
0	1	0	0	0	0.25
0	1	0	0	1	0.22
0	1	0	1	0	0.2
1	0	0	0	1	10
1	0	0	1	0	5
1	0	0	1	1	3.33
1	0	1	0	0	2.5
1	0	1	0	1	2
1	0	1	1	0	1.67
1	0	1	1	1	1.43
1	1	0	0	0	1.25
1	1	0	0	1	1.11
1	1	0	1	0	1

9.4.11. Calib1/Calib2 register

These registers contain the gain settings of the bandgap temperature coefficient correction and the temperature sensor.

	Bit	7	6	5	4	3	2	1	0
Calib1		TRIM_ TC_BGI4	TRIM_ TC_BGI3	TRIM_ TC_BGI2	TRIM_ TC_BGI1	TRIM_ TC_BGI0	-	-	-
0xB	Read/Write	R	R	R	R	R	R	R	R
	Init	x	x	x	x	x	0	0	0

- TRIM_TC_BGI<4:0>: defines the TC correction of the bandgap current
- Calib1<2:0>: not implemented, read as '0'

The Calib1 register is used to indicate the slope of the temperature sensor curve in LSB/Kelvin. The slope is calculated out of a 2-point measurement of the temperature curve and is permanently programmed in the OTP by means of a 5-Bit word and accessible via the Calib1 register, see Table 22.

Calib1 - TRIM_TC_BGI		
Dec	Bin	Slope (LSB/Kelvin)
0	0	-51
1	1	-52
2	10	-53
3	11	-54
4	100	-55
5	101	-56
6	110	-57
7	111	-58
8	1000	-59
9	1001	-60
10	1010	-61
11	1011	-62
12	1100	-63
13	1101	-64
14	1110	-65
15	1111	-66
16	10000	-67
17	10001	-68
18	10010	-69
19	10011	-70
20	10100	-71
21	10101	-72
22	10110	-73
23	10111	-74
24	11000	-75
25	11001	-76
26	11010	-77
27	11011	-78
28	11100	-79
29	11101	-80
30	11110	-81
31	11111	-82

Table 22 : 5-Bit temperature sensor slope information as it is stored in the calib1 register.

	Bit	7	6	5	4	3	2	1	0
Calib2		-	-	TRIM_TEMP5	TRIM_TEMP4	TRIM_TEMP3	TRIM_TEMP2	TRIM_TEMP1	TRIM_TEMP0
0xC	Read/Write	R	R	R	R	R	R	R	R
	Init	0	0	x	x	x	x	x	x

- Calib2<7:6>: not implemented, read as '0'
- TRIM_TEMP<5:0>: defines the calibration settings of the temperature sensor

The offset of the temperature curve is measured at one temperature (preferably 30deg. C) and permanently stored in the zenerzap OTP with 6 bit word length.
This information is accessible via the Calib2 register, see Table 23.

Calib2 - TRIM_TEMP			**Slope: -67 LSB/K**					
			25degC			**30degC**		
Dec	Bin	Offset (degC)	LSL	expected	USL	LSL	expected	USL
1	1	-31	10003.07	10036.51	10069.95	9668.67	9702.11	9735.55
2	10	-30	10069.95	10103.39	10136.83	9735.55	9768.99	9802.43
3	11	-29	10136.83	10170.27	10203.71	9802.43	9835.87	9869.31
4	100	-28	10203.71	10237.15	10270.59	9869.31	9902.75	9936.19
5	101	-27	10270.59	10304.03	10337.47	9936.19	9969.63	10003.07
6	110	-26	10337.47	10370.91	10404.35	10003.07	10036.51	10069.95
7	111	-25	10404.35	10437.79	10471.23	10069.95	10103.39	10136.83
8	1000	-24	10471.23	10504.67	10538.11	10136.83	10170.27	10203.71
9	1001	-23	10538.11	10571.55	10604.99	10203.71	10237.15	10270.59
10	1010	-22	10604.99	10638.43	10671.87	10270.59	10304.03	10337.47
11	1011	-21	10671.87	10705.31	10738.75	10337.47	10370.91	10404.35
12	1100	-20	10738.75	10772.19	10805.63	10404.35	10437.79	10471.23
13	1101	-19	10805.63	10839.07	10872.51	10471.23	10504.67	10538.11
14	1110	-18	10872.51	10905.95	10939.39	10538.11	10571.55	10604.99
15	1111	-17	10939.39	10972.83	11006.27	10604.99	10638.43	10671.87
16	10000	-16	11006.27	11039.71	11073.15	10671.87	10705.31	10738.75
17	10001	-15	11073.15	11106.59	11140.03	10738.75	10772.19	10805.63
18	10010	-14	11140.03	11173.47	11206.91	10805.63	10839.07	10872.51
19	10011	-13	11206.91	11240.35	11273.79	10872.51	10905.95	10939.39
20	10100	-12	11273.79	11307.23	11340.67	10939.39	10972.83	11006.27
21	10101	-11	11340.67	11374.11	11407.55	11006.27	11039.71	11073.15
22	10110	-10	11407.55	11440.99	11474.43	11073.15	11106.59	11140.03
23	10111	-9	11474.43	11507.87	11541.31	11140.03	11173.47	11206.91
24	11000	-8	11541.31	11574.75	11608.19	11206.91	11240.35	11273.79
25	11001	-7	11608.19	11641.63	11675.07	11273.79	11307.23	11340.67
26	11010	-6	11675.07	11708.51	11741.95	11340.67	11374.11	11407.55
27	11011	-5	11741.95	11775.39	11808.83	11407.55	11440.99	11474.43
28	11100	-4	11808.83	11842.27	11875.71	11474.43	11507.87	11541.31
29	11101	-3	11875.71	11909.15	11942.59	11541.31	11574.75	11608.19
30	11110	-2	11942.59	11976.03	12009.47	11608.19	11641.63	11675.07
31	11111	-1	12009.47	12042.91	12076.35	11675.07	11708.51	11741.95
32	100000	0	12076.35	12109.79	12143.23	11741.95	11775.39	11808.83
33	100001	1	12143.23	12176.67	12210.11	11808.83	11842.27	11875.71
34	100010	2	12210.11	12243.55	12276.99	11875.71	11909.15	11942.59
35	100011	3	12276.99	12310.43	12343.87	11942.59	11976.03	12009.47
36	100100	4	12343.87	12377.31	12410.75	12009.47	12042.91	12076.35

37	100101	5	12410.75	12444.19	12477.63	12076.35	12109.79	12143.23
38	100110	6	12477.63	12511.07	12544.51	12143.23	12176.67	12210.11
39	100111	7	12544.51	12577.95	12611.39	12210.11	12243.55	12276.99
40	101000	8	12611.39	12644.83	12678.27	12276.99	12310.43	12343.87
41	101001	9	12678.27	12711.71	12745.15	12343.87	12377.31	12410.75
42	101010	10	12745.15	12778.59	12812.03	12410.75	12444.19	12477.63
43	101011	11	12812.03	12845.47	12878.91	12477.63	12511.07	12544.51
44	101100	12	12878.91	12912.35	12945.79	12544.51	12577.95	12611.39
45	101101	13	12945.79	12979.23	13012.67	12611.39	12644.83	12678.27
46	101110	14	13012.67	13046.11	13079.55	12678.27	12711.71	12745.15
47	101111	15	13079.55	13112.99	13146.43	12745.15	12778.59	12812.03
48	110000	16	13146.43	13179.87	13213.31	12812.03	12845.47	12878.91
49	110001	17	13213.31	13246.75	13280.19	12878.91	12912.35	12945.79
50	110010	18	13280.19	13313.63	13347.07	12945.79	12979.23	13012.67
51	110011	19	13347.07	13380.51	13413.95	13012.67	13046.11	13079.55
52	110100	20	13413.95	13447.39	13480.83	13079.55	13112.99	13146.43
53	110101	21	13480.83	13514.27	13547.71	13146.43	13179.87	13213.31
54	110110	22	13547.71	13581.15	13614.59	13213.31	13246.75	13280.19
55	110111	23	13614.59	13648.03	13681.47	13280.19	13313.63	13347.07
56	111000	24	13681.47	13714.91	13748.35	13347.07	13380.51	13413.95
57	111001	25	13748.35	13781.79	13815.23	13413.95	13447.39	13480.83
58	111010	26	13815.23	13848.67	13882.11	13480.83	13514.27	13547.71
59	111011	27	13882.11	13915.55	13948.99	13547.71	13581.15	13614.59
60	111100	28	13948.99	13982.43	14015.87	13614.59	13648.03	13681.47
61	111101	29	14015.87	14049.31	14082.75	13681.47	13714.91	13748.35
62	111110	30	14082.75	14116.19	14149.63	13748.35	13781.79	13815.23
63	111111	31	14149.63	14183.07	14216.51	13815.23	13848.67	13882.11

Calib2 - TRIM_TEMP			Slope: -67 LSB/K					
			85degC			105degC		
Dec	Bin	Offset (degC)	LSL	expected	USL	LSL	expected	USL
1	1	-31	5990.27	6023.71	6057.15	4652.67	4686.11	4719.55
2	10	-30	6057.15	6090.59	6124.03	4719.55	4752.99	4786.43
3	11	-29	6124.03	6157.47	6190.91	4786.43	4819.87	4853.31
4	100	-28	6190.91	6224.35	6257.79	4853.31	4886.75	4920.19
5	101	-27	6257.79	6291.23	6324.67	4920.19	4953.63	4987.07
6	110	-26	6324.67	6358.11	6391.55	4987.07	5020.51	5053.95
7	111	-25	6391.55	6424.99	6458.43	5053.95	5087.39	5120.83
8	1000	-24	6458.43	6491.87	6525.31	5120.83	5154.27	5187.71
9	1001	-23	6525.31	6558.75	6592.19	5187.71	5221.15	5254.59
10	1010	-22	6592.19	6625.63	6659.07	5254.59	5288.03	5321.47
11	1011	-21	6659.07	6692.51	6725.95	5321.47	5354.91	5388.35
12	1100	-20	6725.95	6759.39	6792.83	5388.35	5421.79	5455.23
13	1101	-19	6792.83	6826.27	6859.71	5455.23	5488.67	5522.11
14	1110	-18	6859.71	6893.15	6926.59	5522.11	5555.55	5588.99
15	1111	-17	6926.59	6960.03	6993.47	5588.99	5622.43	5655.87
16	10000	-16	6993.47	7026.91	7060.35	5655.87	5689.31	5722.75
17	10001	-15	7060.35	7093.79	7127.23	5722.75	5756.19	5789.63
18	10010	-14	7127.23	7160.67	7194.11	5789.63	5823.07	5856.51
19	10011	-13	7194.11	7227.55	7260.99	5856.51	5889.95	5923.39
20	10100	-12	7260.99	7294.43	7327.87	5923.39	5956.83	5990.27
21	10101	-11	7327.87	7361.31	7394.75	5990.27	6023.71	6057.15
22	10110	-10	7394.75	7428.19	7461.63	6057.15	6090.59	6124.03
23	10111	-9	7461.63	7495.07	7528.51	6124.03	6157.47	6190.91
24	11000	-8	7528.51	7561.95	7595.39	6190.91	6224.35	6257.79
25	11001	-7	7595.39	7628.83	7662.27	6257.79	6291.23	6324.67
26	11010	-6	7662.27	7695.71	7729.15	6324.67	6358.11	6391.55
27	11011	-5	7729.15	7762.59	7796.03	6391.55	6424.99	6458.43
28	11100	-4	7796.03	7829.47	7862.91	6458.43	6491.87	6525.31
29	11101	-3	7862.91	7896.35	7929.79	6525.31	6558.75	6592.19
30	11110	-2	7929.79	7963.23	7996.67	6592.19	6625.63	6659.07
31	11111	-1	7996.67	8030.11	8063.55	6659.07	6692.51	6725.95
32	100000	0	8063.55	8096.99	8130.43	6725.95	6759.39	6792.83
33	100001	1	8130.43	8163.87	8197.31	6792.83	6826.27	6859.71
34	100010	2	8197.31	8230.75	8264.19	6859.71	6893.15	6926.59
35	100011	3	8264.19	8297.63	8331.07	6926.59	6960.03	6993.47
36	100100	4	8331.07	8364.51	8397.95	6993.47	7026.91	7060.35
37	100101	5	8397.95	8431.39	8464.83	7060.35	7093.79	7127.23
38	100110	6	8464.83	8498.27	8531.71	7127.23	7160.67	7194.11
39	100111	7	8531.71	8565.15	8598.59	7194.11	7227.55	7260.99
40	101000	8	8598.59	8632.03	8665.47	7260.99	7294.43	7327.87
41	101001	9	8665.47	8698.91	8732.35	7327.87	7361.31	7394.75
42	101010	10	8732.35	8765.79	8799.23	7394.75	7428.19	7461.63
43	101011	11	8799.23	8832.67	8866.11	7461.63	7495.07	7528.51
44	101100	12	8866.11	8899.55	8932.99	7528.51	7561.95	7595.39
45	101101	13	8932.99	8966.43	8999.87	7595.39	7628.83	7662.27
46	101110	14	8999.87	9033.31	9066.75	7662.27	7695.71	7729.15
47	101111	15	9066.75	9100.19	9133.63	7729.15	7762.59	7796.03
48	110000	16	9133.63	9167.07	9200.51	7796.03	7829.47	7862.91

49	110001	17	9200.51	9233.95	9267.39	7862.91	7896.35	7929.79
50	110010	18	9267.39	9300.83	9334.27	7929.79	7963.23	7996.67
51	110011	19	9334.27	9367.71	9401.15	7996.67	8030.11	8063.55
52	110100	20	9401.15	9434.59	9468.03	8063.55	8096.99	8130.43
53	110101	21	9468.03	9501.47	9534.91	8130.43	8163.87	8197.31
54	110110	22	9534.91	9568.35	9601.79	8197.31	8230.75	8264.19
55	110111	23	9601.79	9635.23	9668.67	8264.19	8297.63	8331.07
56	111000	24	9668.67	9702.11	9735.55	8331.07	8364.51	8397.95
57	111001	25	9735.55	9768.99	9802.43	8397.95	8431.39	8464.83
58	111010	26	9802.43	9835.87	9869.31	8464.83	8498.27	8531.71
59	111011	27	9869.31	9902.75	9936.19	8531.71	8565.15	8598.59
60	111100	28	9936.19	9969.63	10003.07	8598.59	8632.03	8665.47
61	111101	29	10003.07	10036.51	10069.95	8665.47	8698.91	8732.35
62	111110	30	10069.95	10103.39	10136.83	8732.35	8765.79	8799.23
63	111111	31	10136.83	10170.27	10203.71	8799.23	8832.67	8866.11

Table 23: 6-Bit Temperature curve offset information for a typical slope of -67 LSB/K.

9.4.12. EnChan register

This register contains bit to enable/disable active light and ambient light channels.

	Bit	7	6	5	4	3	2	1	0
EnChan		EN_ TEMP	EN_ DIAG_A	EN_ DIAG_B	EN_ CH_A	EN_ CH_B	EN_ CH_C	EN_ CH_D	EN_ DIAGAMB
0xD	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Init	1	1	1	1	1	1	1	1

- EN_TEMP: 1 = temperature channel is in use, 0 = temperature channel is not in use
- EN_DIAG_A: 1 = enables diagnostics on active light channel A, 0 = disables the diagnostics
- EN_DIAG_B: 1 = enables diagnostics on active light channel B, 0 = disables the diagnostics
- EN_CH_A: 1 = active light channel A is enabled (TIA + Demodulator + Anti-Aliasing Filter + SC-LPF), 0 = active light channel A is completely switched off to reduce current consumption
- EN_CH_B: 1 = active light channel B is enabled (TIA + Demodulator + Anti-Aliasing Filter + SC-LPF), 0 = active light channel B is completely switched off to reduce current consumption
- EN_CH_C: 1 = ambient light channel C is in use, 0 = ambient light channel C is not in use
- EN_CH_D: 1 = ambient light channel D is in use, 0 = ambient light channel D is not in use
- EN_DIAGAMB: 1= ambient diagnosis is possible, 0= ambient diagnosis is not possible

The bits EN_CH_A/EN_CH_B/EN_DIAGAMB can be used to switch off channels that are not needed, and thus reducing the current consumption.
When going into Sleep or Standby the setting of these bits is ignored, all channels will be switched off independently of EN_CH register contents.

The bits EN_TEMP/EN_CH_C/EN_CH_D/EN_DIAGAMB are used to indicate which channels are in use and which channels are not in use. Terminals, which are not connected, must be disabled in the ENChan register. Otherwise error flags might occur.

In case all EN_CH_C/D/DIAGAMB bits are set to zero, but an ambient measurement is requested, then the Command Invalid status flag will be set high. The measurement itself will not be executed.

9.4.13. Tamb register

This register contains settings for the DC light compensation circuitry + controls the repetition rate of the auto-zero timer.

	Bit	7	6	5	4	3	2	1	0
Tamb		DC_ COMP_ IC53	DC_ COMP_ IC52	DC_ COMP_ IC51	DC_ COMP_ IC50	-	-	Tamb1	Tamb0
0xE	Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
	Init	0	0	0	0	0	0	1	0

- DC_COMP_IC5<3:0>: setting of the amplitude of the 5th PWL slope
- Tamb<3:2>: not implemented, read as '0'
- Tamb<1:0>: controls the repetition rate of the auto-zero timer
-

Tamb1	Tamb0	Repetition Rate (ms +/-5%)
0	0	1.25
0	1	2.5
1	0	5
1	1	10

9.5. Window Watchdog Timer

The internal watchdog timer is a watchdog based on two different windows: an open and a closed window. During the open window the master can restart the watchdog timer. During the closed window, no restarts are accepted.

The restart (re-initialisation) of the watchdog timer happens via the *WT* (Watchdog Trigger) pin: when a falling edge is detected on the *WT* pin, the watchdog will be restarted.
The low time on the *WT* pin should be at least a time t_{wt_l}.

After a POR or a reset issued by the watchdog and after a wake-up from Sleep Mode (either by uploading the NRM command, or by using the *WAKE_UP* pin), the window watchdog will open an active window of a time t_{wdt_init}, during which a watchdog restart must be issued by the µC. If no watchdog restart is received by the end of the open window, the µC will be reset.
After this initial period, the window watchdog is programmed to wait a time t_{wdt_closed} during which no watchdog restarts are allowed. If a watchdog restart is sent during the closed window time, the watchdog will reset the master via the *MR* (Master Reset) pin.
After a closed window, an open window of a time t_{wdt_open} will follow during which a watchdog restart is expected. If no watchdog restart is received till the end of the open window, the µC will be reset via the *MR* pin.

Changing mode between Normal Running Mode and Standby Mode will not influence the watchdog timing or state. Also a CR command will not change the used window times. The watchdog counter will not be influenced when changing mode between NRM and STBY or when uploading a CR command.

The Watch Dog Timer is disabled in Sleep Mode. A falling edge on the *WT* pin in the Sleep Mode will set an error flag in the register 'Err'. Coming back from Sleep Mode to Normal Running Mode always restarts the watchdog with the initial timing window.

This figure shows what timing windows are used in the different operating modes:

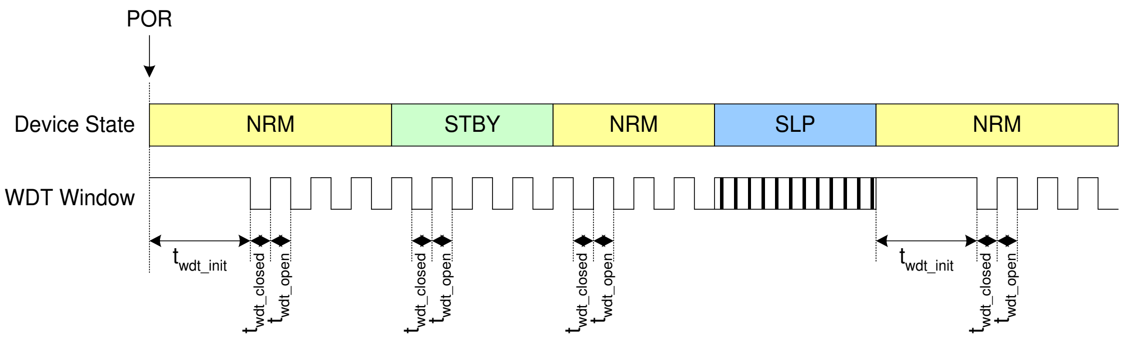
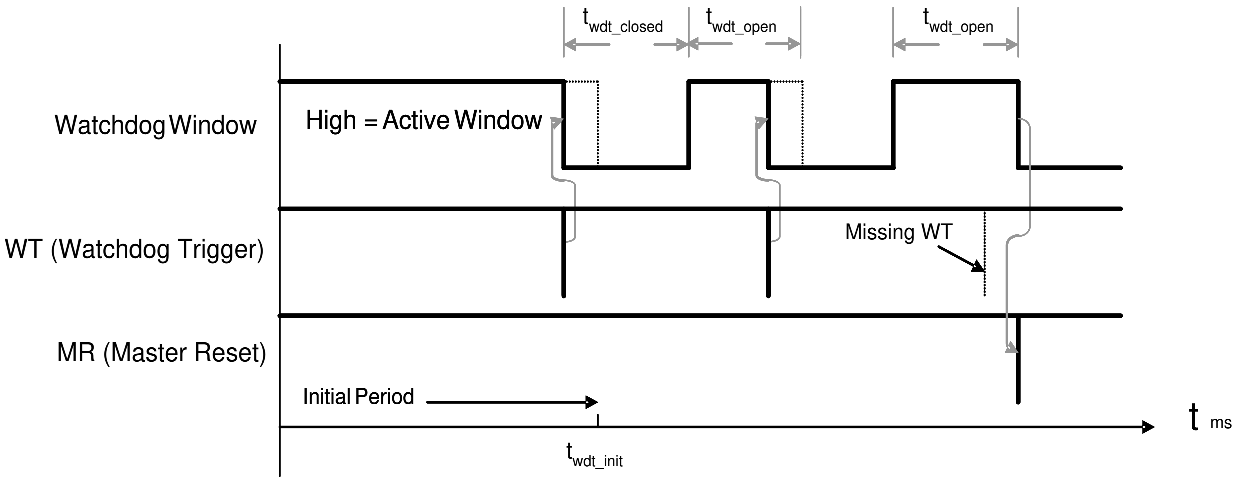


Figure 16 : Window times during different operating modes

The two diagrams below show the functionality of the watchdog timer:



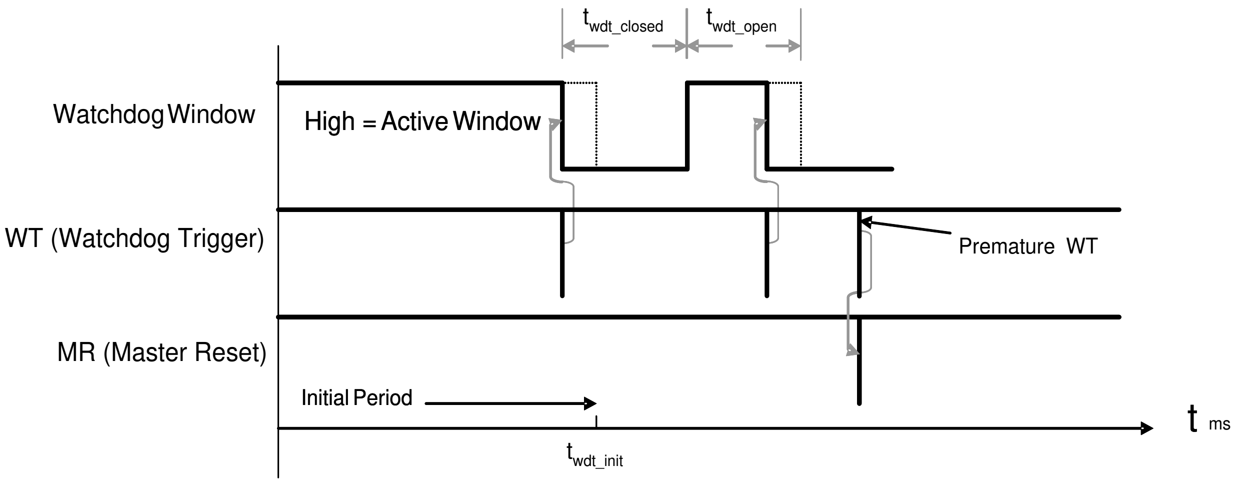


Figure 17 : Functionality of the window watchdog timer

A reset of the µC due to time-out of the watchdog is achieved by setting the *MR* pin low during a time t_{MR} (default state of the *MR* pin is high).

When the device is operating in Sleep or Standby Mode, the *WAKE_UP* pin will be monitored. When a falling edge is detected on that pin, the device will switch to Normal Running Mode and, when waking up from Sleep Mode, the Watchdog Timer will be started (with an initial window time of t_{wdt_init}).

Note that no pull-up or pull-down resistor is foreseen on the *WAKE_UP* pin. To avoid that parasitic spikes can wake up the device, the *WAKE_UP* input is debounced (typical debounce time is in the range of 2µs). The low time on the *WAKE_UP* pin should be at least a time t_{wu_l}.

9.6. Reset Behaviour

Power-On Reset
After a Power-On Reset, the device is operating in Normal Running Mode. All internal data registers are set to their initial state:

- the device state is Normal Running Mode
- the Watchdog counter is initialized to generate the initial window time
- all registers containing (diagnostic) measurement data are initialized to 0x00
- bits 7, 4, 3 of the Internal Status Flags are cleared
- the user settings registers are set to their initial values (see Section 9.4)
- the 'Err' register will initialize to 0x00. However, as some voltages are continuously measured, it will reflect immediately if an error is detected or not.

The *MR* pin will be initialized to '1'. The *DR* pin will be initialized to '0', but after the time $t_{startup}$ it will switch to '1' to indicate that the device is ready to accept the first command (see also Section 9.9).

The output of the *MISO* pin is depending on the *CS* state: if *CS* is high, the *MISO* pin is in tri-state. If *CS* is low, the output of the *MISO* pin is undefined.

CR Command
At every upload of the CR command, the device returns to the state like it is after a Power-On-Reset, except for the Watchdog counter and the state of the *MR* line. The Watchdog counter and the state of the *MR* line will not be influenced by uploading a CR command. Also, the CR command will not change the contents of the 'Rst' register.

After a CR command the DR pin will be kept low during a time $t_{startup}$.

Read-out
At the end of each read-out, all registers containing (diagnostic) measurement data are cleared to 0x00.

Watchdog time-out
When a reset occurs due to a watchdog time-out, the *MR* pin will go low for a time t_{MR}. The Watchdog counter will be initialized with the window time t_{wdt_init}. All other states, lines and registers of the ASIC will not be affected.

Changing operation mode
When changing operation mode (RSLP, CSLP, RSTBY, CSTBY, NRM) the right status flags are set.
Changing operation mode will not affect the user settings registers and the (diagnostic) measurement data registers.

The *DR* pin will be set to '0' and after the time t_{wakeup_slp} resp. t_{wakeup_stby} it will be set to '1', when waking up from Sleep resp. Standby Mode.

9.7. Wake-up from Sleep or Standby

The figure below shows what happens when switching operation mode, and the behaviour of the *DR* pin and the watchdog timer.

The *WAKE_UP* pin is only monitored during Sleep and Standby. When a falling edge is detected during Sleep or Standby, the following will happen:
- the *DR* pin goes low for a time t_{wakeup_stby} or t_{wakeup_slp}
- the watchdog timer is initialised and starts counting, when waking up from Sleep
- the device changes to Normal Running Mode, enabling the appropriate blocks

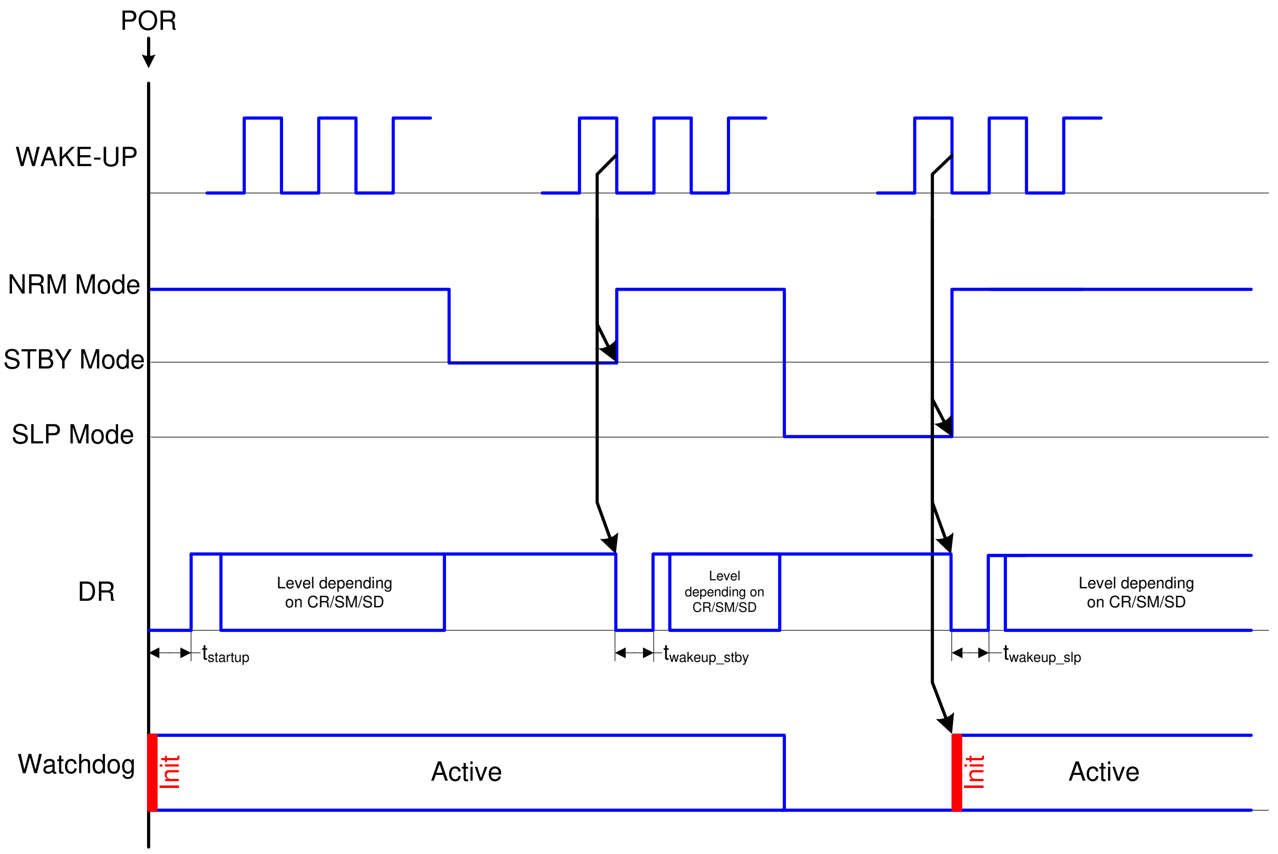


Figure 18 : Behaviour of DR and Watchdog when switching mode

9.8. CRC Calculation

The 8-bit CRC calculation will be based on the polynomial $x^8 + x^2 + x^1 + x^0$. This polynomial is widely used in the industry, it is e.g. used for generating:

- the Header Error Correction field in ATM (Asynchronous Transfer Mode) cells
- the Packet Error Code in SMBus data packets

Some probabilities of detecting errors when using this polynomial:

- 100% detection of one bit errors
- 100% detection of double bit errors (adjacent bits)
- 100% detection of two single-bit errors for frames less than 128 bits in length
- 100% detection of any odd number of bits in error
- 100% detection of burst errors up to 8 bits
- 99.61% detection of any random error

A possible hardware implementation using a Linear Feedback Shift Register (LFSR) is shown in the figure below:

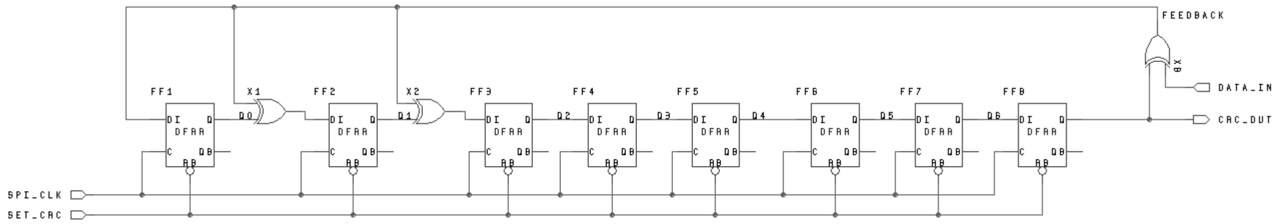


Figure 14: 8-bit CRC implementation using a LFSR

The generation of the CRC requires the following steps:

- Reset all flip-flops
- 0x00 is the initial value, shifting in all zeroes does not affect the CRC
- Shift in the read-out data bytes. First byte is Data Byte 1 (= Internal Status Flags), last byte is Data Byte (X+1) (with X defined in Figure 12).
- When the last byte has been shifted in, the flip-flops contain the CRC: CRC=FF[8..1].

An easy method to check if there were no transmission errors is to calculate the CRC of the whole read-out data stream including the CRC Byte. When the calculated CRC results in 0x00, the transmission was most likely error free. If the resulting CRC is not equal to zero, then an error occurred in the transmission and the complete data stream should be ignored.

Some CRC results for example messages are given in Table 24.

ASCII String messages	CRC result
-None-	0x00
"A"	0xC0
"123456789"	0xF4
a string of 256 upper case "A" characters with no line breaks	0x8E

Table 24: CRC examples

9.9. Global Timing Diagrams

A global timing diagram with separate SM-RO cycles is given in Figure 19. After power-up there is a Power-On-Reset phase (POR) to initialize the sensor into a reset state. When the device is ready to accept the first command, the *DR* pin goes high. In Figure 19 the first command is the WR command to define the contents of the user registers (optionally). The first measurement cycle is e.g. initiated by uploading a SM command. After completion of the measurement cycle, the *DR* goes high. This indicates that the read-out cycle can be started. A RO command has to be uploaded to bring the data on the *MISO* pin. When the read-out is completed, a new measurement cycle can be started. In Figure 19 a SM command is used. This starts a next measurement cycle. Once *DR* is high, a read-out can be done again.

In between different Measurement/Read-Out cycles, the user registers can be changed with WR commands. Optionally those registers can be read back with the RR command to check if the right values were uploaded.

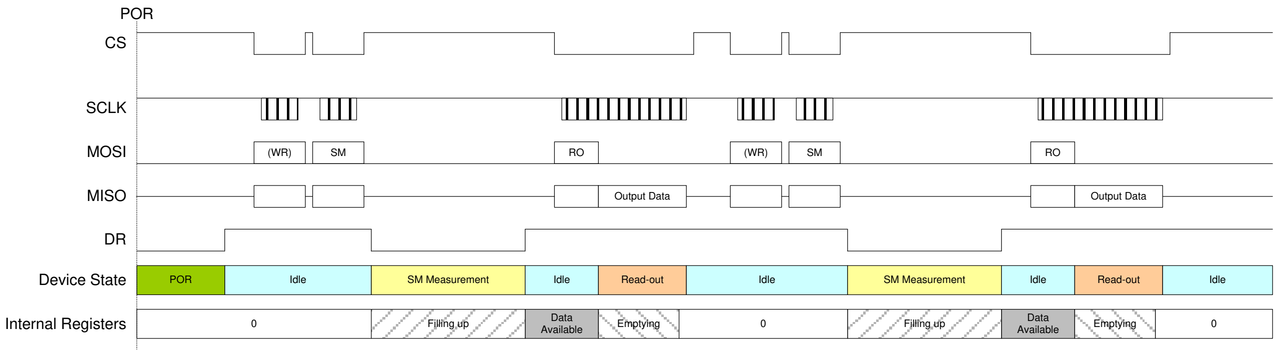


Figure 19: Global timing diagram with separate SM-RO

Figure 20 shows a timing diagram wherein separate SM-RO cycles are mixed with combined SM-RO cycles. After the Power-On-Reset phase, a SM measurement cycle is started. Once the *DR* pin is high, the data can be read out. A SM command with extra clocks is used to combine the read-out and the start of the next measurement cycle. With the extra clocks, the data of the internal registers is transferred to the *MISO* pin. When the *CS* pin goes high, the next measurement cycle (SM) will be started.
Once the *DR* pin is high, a normal RO command is uploaded to bring the data to the *MISO* pin. If needed, the settings in the user registers can be changed with the WR command and optionally the RR command can be used to check if the right values were uploaded.
A new measurement cycle can be started with e.g. a normal SM command. When the *DR* pin is high, the data can be transferred by uploading e.g. a SM command that combines the read-out and the start of a new measurement cycle.

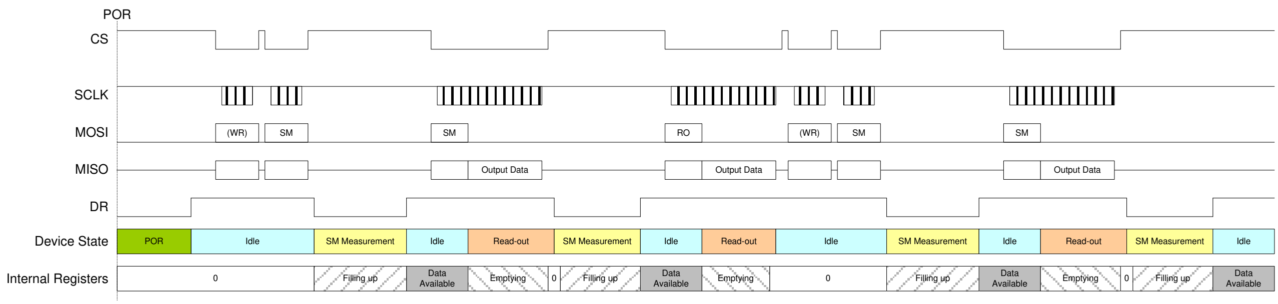
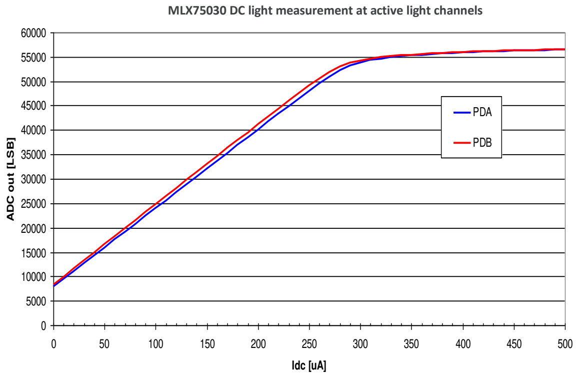


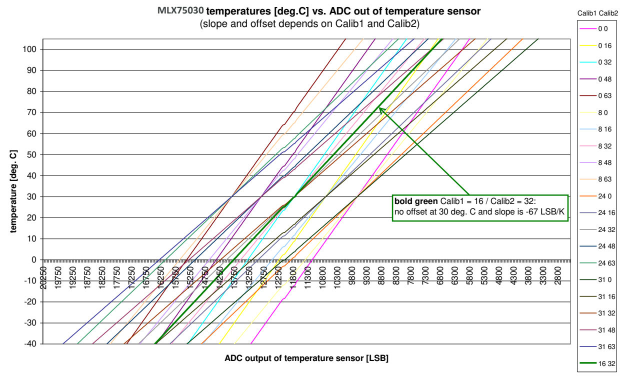
Figure 20: Global timing diagram with separate SM-RO and combined SM-RO together

10. Performance Graphs

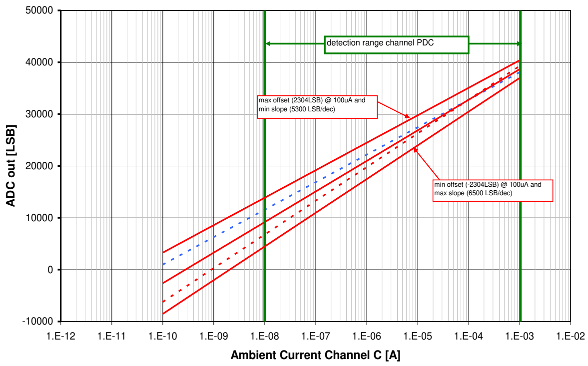
10.1. ActiveLight Channel DC Measurement



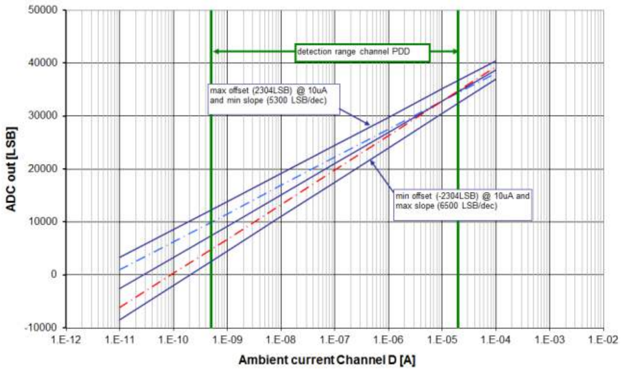
10.2. Temperature Sensor Characteristics



10.3. Ambient Light Channel C

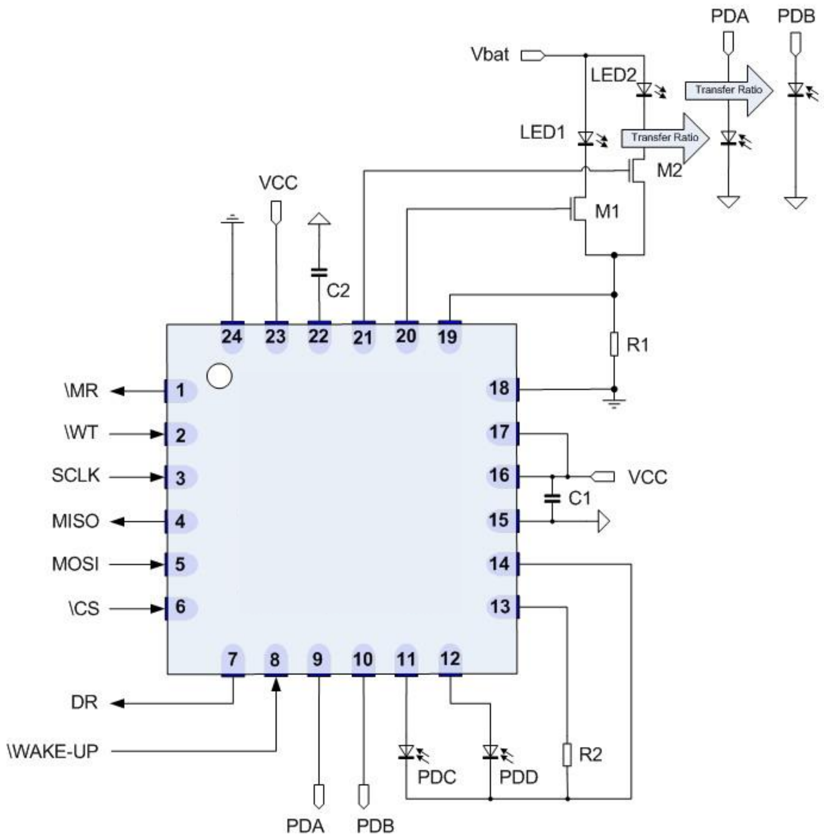


10.4. Ambient Light Channel D



11. Application Information

11.1. Application circuit for 2 ActiveLight channels and 2 ambient light channels



Component	Type	Value	Description
C1	SMD capacitor	47nF	Blocking capacitor, connected to analog GND
C2	SMD capacitor	68nF	Blocking capacitor for int. voltage regulator, connected to analog GND
R1	SMD resistor	6.4 Ohms	Shunt Resistor
R2	SMD resistor	56k Ohms	Ambient Light Diagnostic termination resistor
M1			LED driver MOSFET
M2			LED driver MOSFET
LED1/2			Active light channel Infrared LED
PDA / PDB			Active light channel infrared photodiode, daylight blocking mold
PDC			V-lambda photodiode
PDD			Photodiode

Table 25: Application circuit components for 2 ActiveLight and 2 ambient light channels

12. Application Comments

The MLX75030 is featuring very sensitive current inputs on the pins 9 and 10 for active light detection and on the pins 11 and 12 for ambient light measurements in a range over several orders of magnitude. In order to achive optimum results in the application it is recommended to consider the following hints for the design of the PCB:

1. The both supply voltage pins 16 (VDDA for analog circuit parts) and 23 (VDDD for digital circuit parts) shall be star-connected to the local (external) regulator output (3.0V-3.6V) in order to avoid digital disturbance injection into the analog supply.

2. Note that the device works with two separate ground connections: Pin 15 works as analog ground for the sensitive input circuitry whereas pin 24 works as digital ground and as ground connection of the LED path, which carries high pulse currents.

3. The Exposed Pad of the package should be star-connected to the local (external) ground pin of the regulator.

4. The external blocking capacitors C1 and C2 shall be placed as close as possible to the corresponding pins of the device.

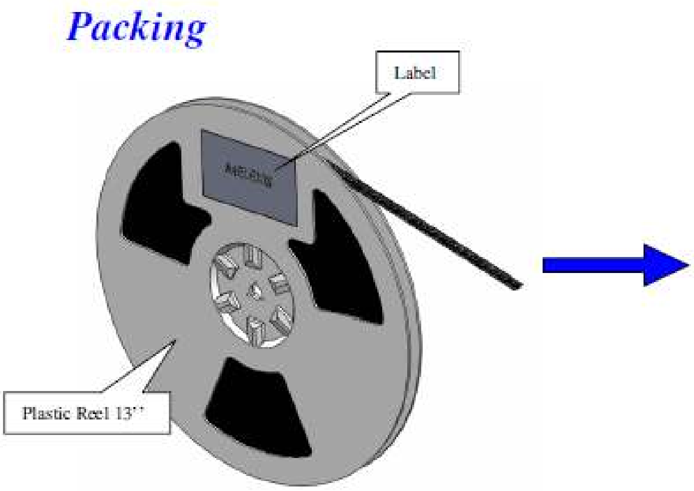
5. The external photodiodes on the active light channel inputs as well as on the ambient light inputs shall be placed as close as possible to the corresponding pins of the device. If this is not possible due to constructive reasons, the connections shall be shielded by a noise-free analog ground plane in order to avoid performance-loss due to disturbance coupling.

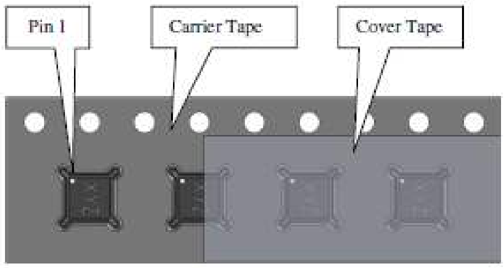
6. Notice that GNDAMB must not be connected to any GND line on the PCB. This terminal is actively switched to supply voltage during diagnosis mode.

7. Note that not connected input channels (ActiveLight, ambient light) must be disabled in the EnChan register.

8. For diagnosis purposes on pin DIAGAMB a current of 10uA is recommended. For a current in this range the diagnosis result is least sensitive to temperature.

13. Tape and Reel Specification





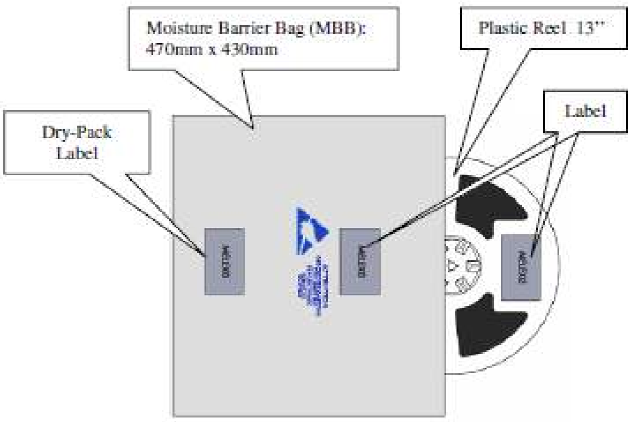
Remark:
Pay attention to the marking orientation because it is used for component (pin1) orientation. Some devices may have different marking orientation, so please consult your Melexis contact person for more information.

Plastic 13" Reel:
Made by antistatic high-impact molded polystyrene. The mechanical integrity of the reel is not affected by humidity.

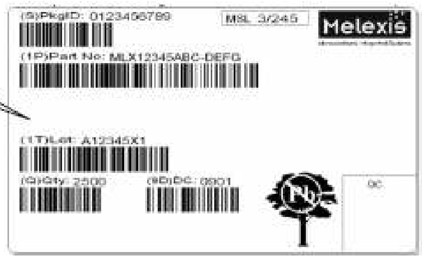
Packing Materials:

Embossed Plastic Carrier Tape:
Made by Tri-Laminate PS+C material (polystyrene with carbon).
Typical carrier tape material thickness 0,21mm.

Cover Tape:
All Cover Tapes used by Melexis are Heat Activated and antistatic.
The main ABX type of Cover Tape is constructed in two layers, a 0.0254mm thick polyester base film covered by a 0.0279mm thick heat-activated adhesive coating layer.

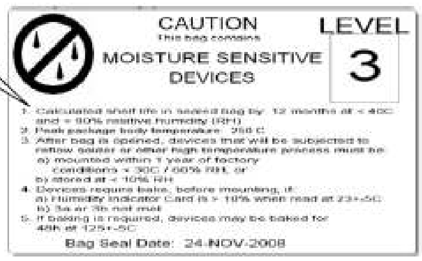


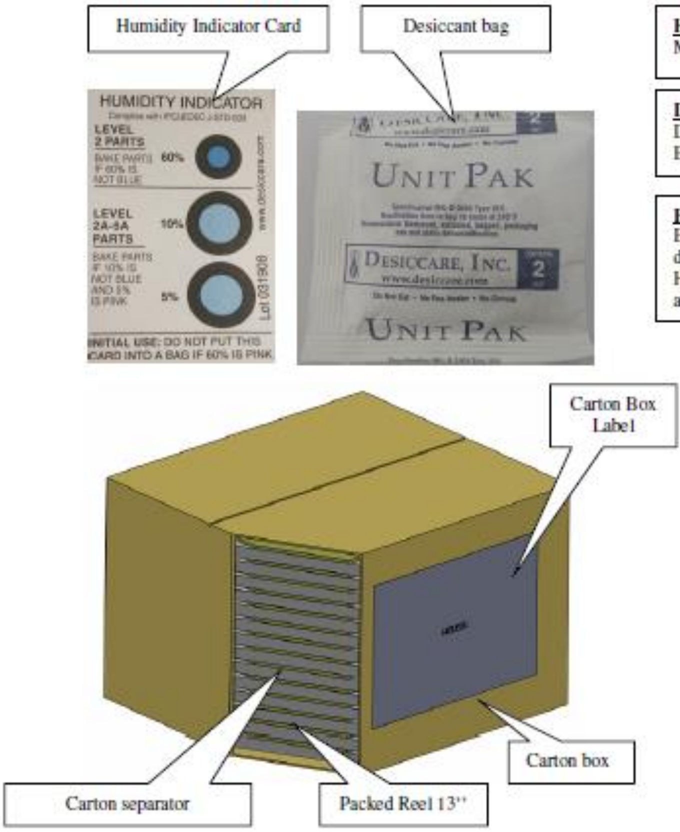
Label Sample



Moisture Barrier Bag (MBB):
Made in 5 different layers with total thickness of 0.18mm.
At the core is a layer of polyester sandwiched between aluminum shields. The outside layer: dissipative polyester, innermost layer: static dissipative polyethylene.

Dry-Pack
Label Sample

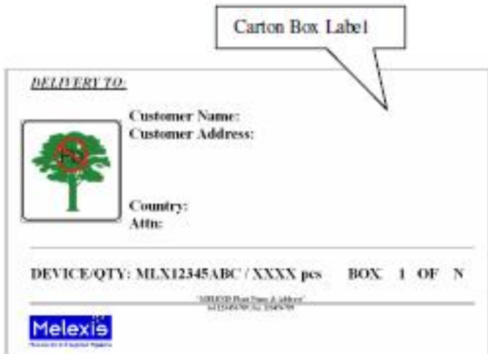




Humidity Indicator Card (HIC):
Moisture sensitive blotting paper card with 3 spots for 5%, 10% and 60%.

Desiccant bag:
Desiccant material: Bentonite Clay.
Bag size: 2Units

Packing of single reel:
Each full reel is labeled and separately packed into labeled MBB. All devices with MSL level from 2 to 6 are packed with Desiccant Bag and HIC. Devices with MSL1 are packed in MBB but without desiccant bag and HIC.

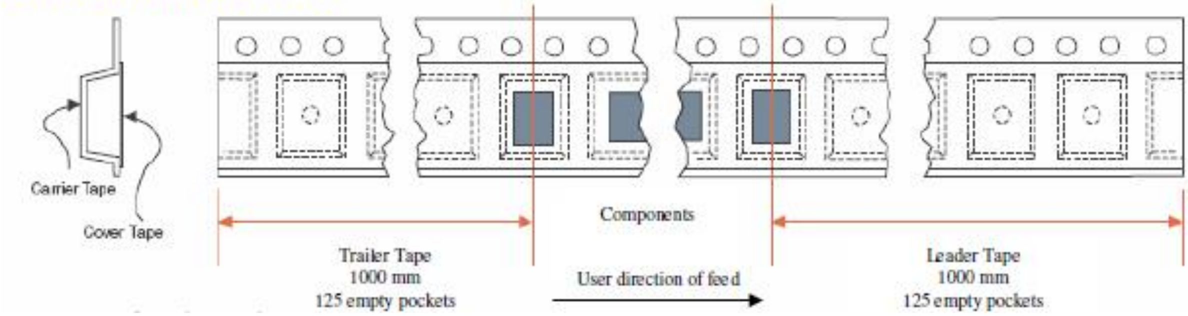


Carton Packing Description:
Each vacuum sealed MBB is horizontally placed into standard outer carton box. Carton separators are applied between each MBB package, as long as on the bottom and top of the outer box.

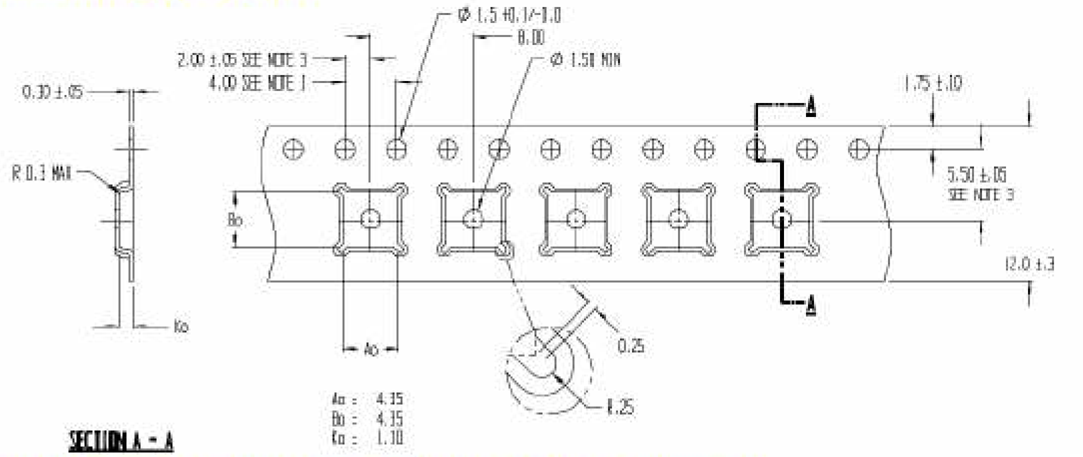
QFN4x4x0.9 – 24L Packing information		
Parameter	Carton packing type E02	
	Carton Box A	Carton Box B*
Box Size (mm)	450 x 420 x 260	450 x 420 x 160
QTY/Reel	5000pcs	5000pcs
Reel Size	13''	13''
Reels/Box	11pcs	6pcs
QTY/Box	55 000pcs	30 000pcs
Weight/Box (kg)	8	6

* Carton box B is used as last box in shipment, or when the shipping reel quantity is lower, or equal than 6 reels.

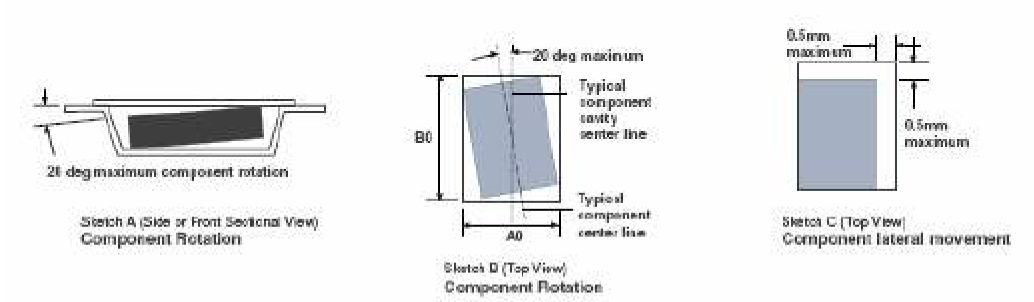
Leader and Trailer



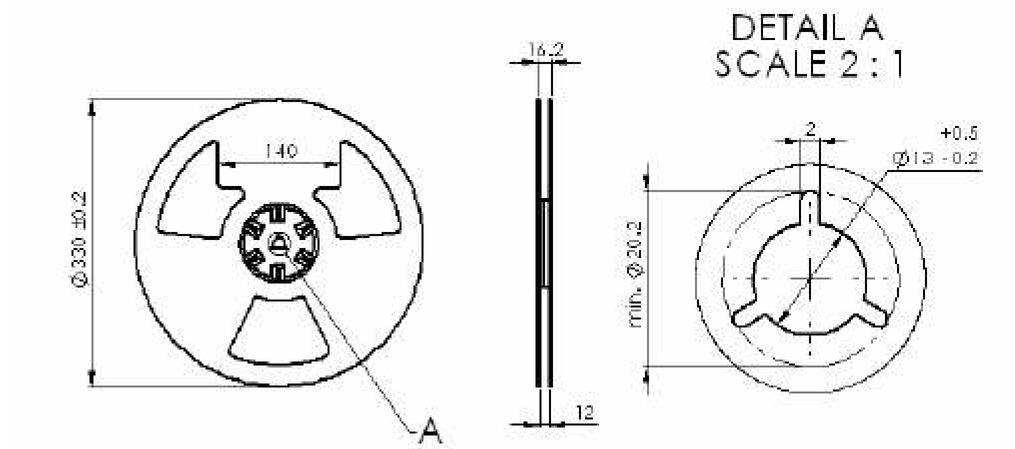
Carrier Tape Data



Component Rotation and Lateral Movement



Plastic Reel Data



14. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

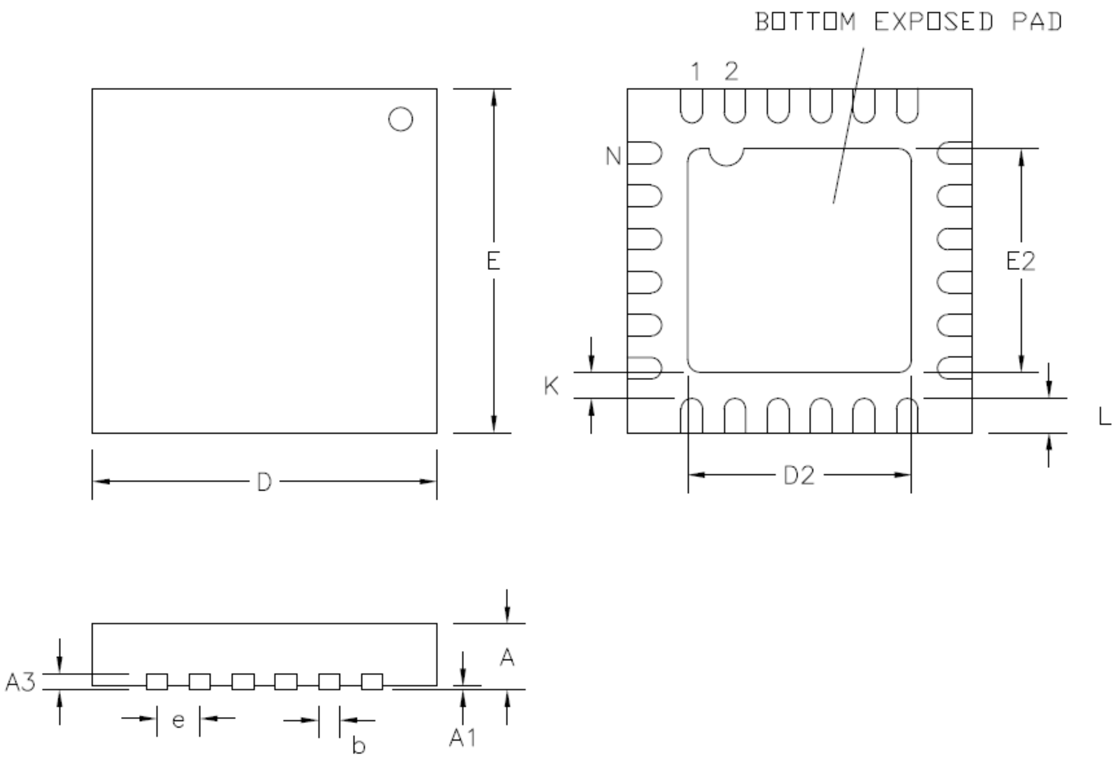
The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.asp

15. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

16. Package Information



	D x E	N	e		A	A1	A3	D2	E2	L	K	b
Quad	All dimensions in mm											
	4 x 4	24	0.50 ±0.05	min	0.80	0.00	0.20 REF	2.50	2.50	0.35	0.20	0.18
				max	1.00	0.05		2.70	2.70	0.45	–	0.30

Table 26: Package dimensions

Package	Θjc [°C/W]	Θja [°C/W] (JEDEC 1s0p board)	Θja [°C/W] (JEDEC 1s2p board)
QFN 4x4	16	154	50

Table 27: ϑJA values

17. Marking Information

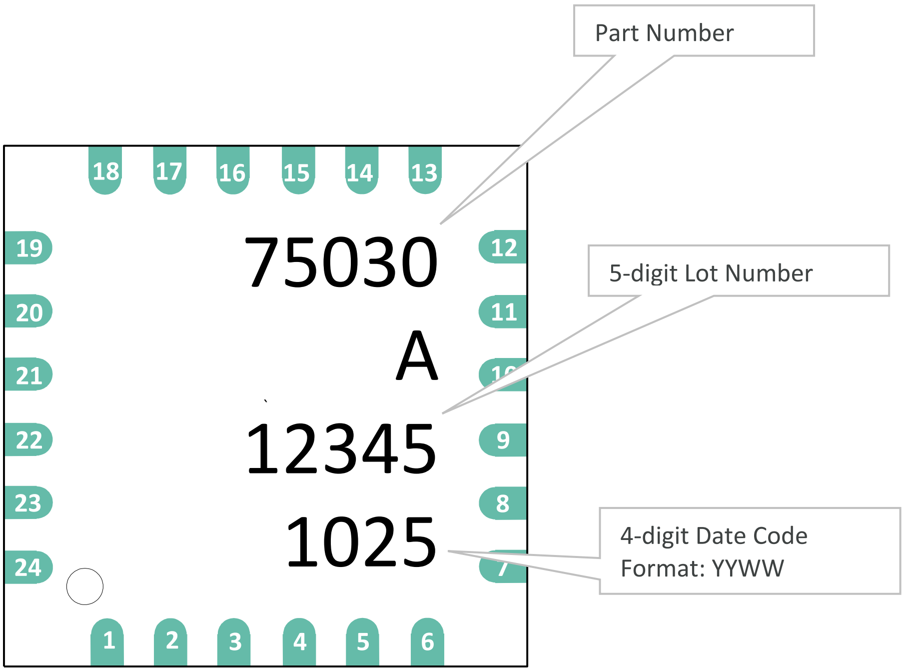


Figure 21: Package marking of the MLX75030 device in QFN24 4x4 SMD package

18. Disclaimer

For the latest version of this document, go to our website at
www.melexis.com

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