



QorIQ Multicore Processor Development

P4080 Development System

Overview

The P4080DS is a flexible development system supporting the P4080, P4040 and P4081 processors. With 1.5 GHz P4080 and rich I/O mix, the P4080DS board is intended for evaluation of P4080 and P4040 in networking, telecom and industrial applications such as enterprise and service provider routers, switches, security gateways, channel cards for LTE base stations, radio network controllers (RNCs), aerospace and defense, factory automation and more.

The P4080DS can help shorten your time to market. The board, which exercises most capabilities of the device, can serve as a reference for hardware development. It can also be used as a debug tool to check behaviors on the board compared to behaviors seen on customer boards and for software development and performance evaluation before your custom board is ready.

The P4080 processor is based upon the e500mc core, built on Power Architecture® technology, offering speeds of 1200–1500 MHz. It has a three-level cache hierarchy with 32 KB of instruction and data cache per core, 128 KB of unified backside L2 cache per core and 2 MB of shared frontside CoreNet platform cache that fronts the memory controller. The processor's I/O includes 18 SerDes lanes

running at up to 5 GHz, multiplexed across three PCI Express® Gen2 controllers, two 10 GE XAUI interface, eight 1 GE SGMII interfaces, two Serial RapidIO 1.2 interfaces running at up to 3.125 GHz, and the high-speed Aurora debug interface. It has a dual 64-bit (72-bit with ECC) DDR2 and DDR3 DRAM interfaces running at up to 1333 MHz. It includes two USB 2.0 interfaces (with ULPI interface to external PHY), two DUARTs, an SD/MMC interface, four I²C, and SPI. It also includes the accelerator blocks collectively known as Data Path Acceleration Architecture (DPAA) that offload various tasks from the core, including routine packet handling, security algorithm calculation and pattern matching.

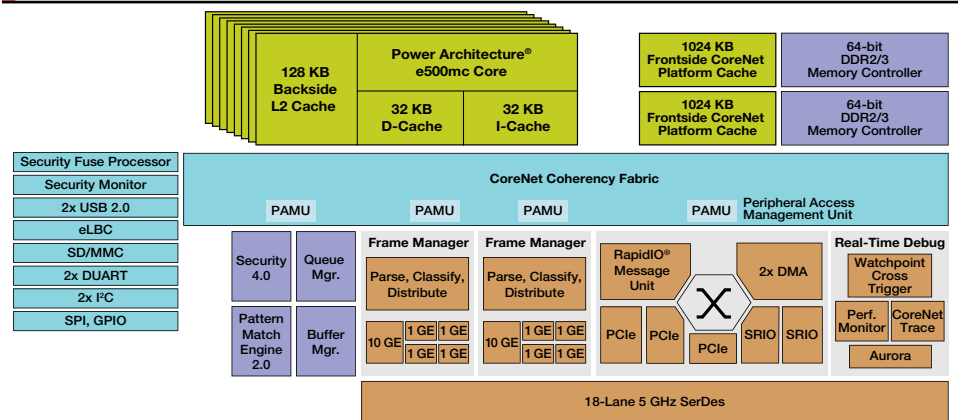
The P4080DS has significant flexibility in allocating its 18 SerDes lanes to various functions. The P4080DS platform features one RGMII port, one USB ULPI, five

controllers supporting five add-in card slots including a x4 slot for our optional SGMII-PEX-RISER, a x4 slot for the optional Freescale XAUI-RISER and the Aurora high-speed debug port. PCI Express and Serial RapidIO interfaces are also supported.

The memory system of the P4080DS supports 4 GB of DDR3 at 1333 MHz. It has 128 MB of NOR flash, three I²C controllers supporting EEPROM storage for boot sequence, a 16 MB SPI-based EEPROM memory and an SD media card slot.

The P4080DS is pre-loaded with the Freescale Linux software development kit for QorIQ processors with Data Path Acceleration. This includes a 2.6.x.x SMP Linux kernel, hugetlb file system for applications with a large memory footprint, user space DPAA for high-performance packet handling, u-boot, the GCC tool chain and Mentor System Builder.

QorIQ P4080 Communication Processor



Legend: ■ Core Complex (CPU, L2, L3 Cache) ■ Basic Peripherals and Interconnect ■ Accelerators and Memory Control ■ Networking Elements



P4080DS Board Features

Processor

- P4080, 1.5 GHz core with 1333 MHz DDR3 data rate
- Multiple SysClk inputs for generating various device frequencies

Memory

- 4 GB unbuffered DDR3 240-pin sockets supporting standard JEDEC DIMMs
- 128 MB NOR flash (fast boot)
- SPI-based 16 MB EEPROM
- SD media card slot

High-Speed Serial Port (SerDes)

- 18 lanes, dividable into many combinations
- Five add-in slots to selectably connect to five of the 16 controllers supported by the P4080
- Supports PCI Express, SGMII, Nexus/Aurora debug, XAUI and Serial RapidIO

Ethernet

- Supports one 10/100/1000 port with no add-in cards
- TSEC as RGMII to Vitesse VSC8244 PHY
- SGMII supported with optional SGMII-PEX-RISER cards
- 10 GbE supported with optional XAUI-RISER card

USB 2.0

- One USB ULPI
- Combo USB/RJ45 stack

UART

- Two serial ports at up to 115200 Kb/s

I²C

- Three I²C controllers
- I²C-based, real-time clock and battery-backed SRAM
- EEPROM storage for boot-sequencer, SystemID, ngPIXIS (FPGA) processor code

Debug

- JTAG/COP
- Aurora/Nexus debug support
- EVT support

Other

- PromJet debug port
- System Logic ngPIXIS (FPGA)
- Temperature sensor



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