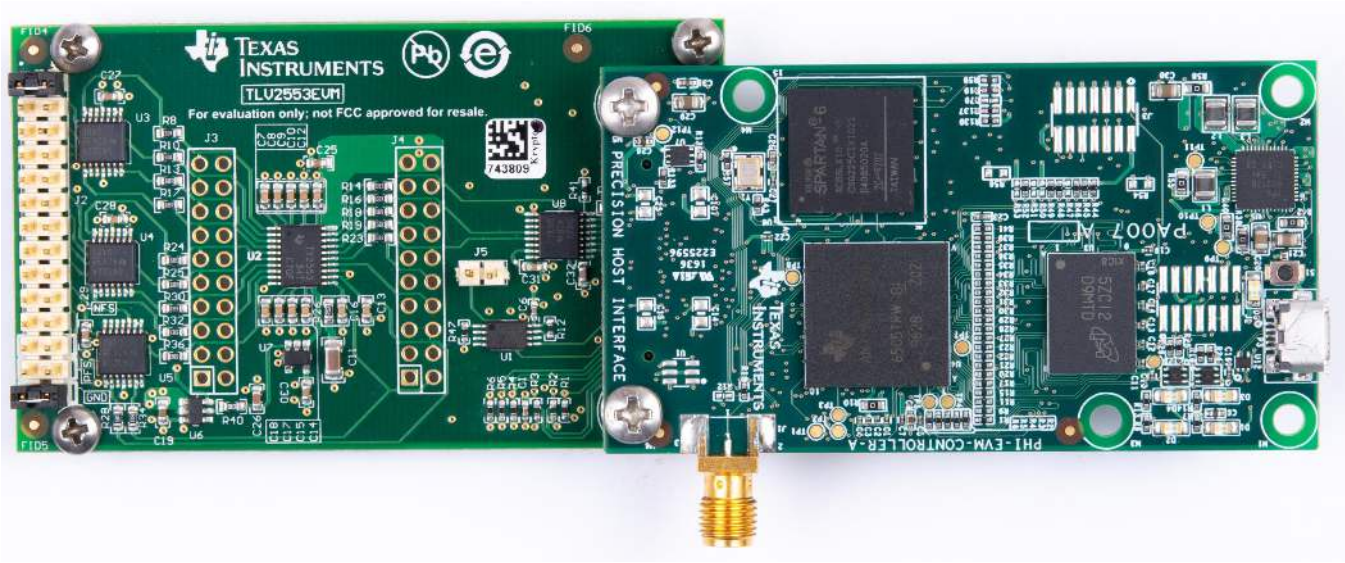
TLV2553EVM-PDK Evaluation Module



This user's guide describes the characteristics, operation, and use of the TLV2553EVM performance demonstration kit (PDK). This kit is an evaluation platform for the TLV2553, which is a 12-bit, 200-kSPS, successive approximation register (SAR), analog-to-digital converter (ADC) that features an 11-channel analog input multiplexer and a serial SPI™ digital output interface. The EVM eases the evaluation of the TLV2553 device with hardware and software for computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
TLV2553	SLAS354
OPA4322	SBOS538
OPA320	SBOS513
REF3240	SBVS058
TXB0106	SCES709
TPS7A4901	SBVS121

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1 Overview

The TLV2553EVM-PDK is a platform for evaluating the performance of the TLV2553 SAR ADC. The evaluation kit includes the TLV2553EVM board, the precision host interface (PHI) board, and accompanying computer software that enables the user to communicate with the ADC over USB, capture data, and perform data analysis.

The TLV2553EVM board includes the TLV2553 SAR ADC and all the peripheral circuits and components necessary to extract good performance from the ADC.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port.
- Provides the digital input and output signals necessary to communicate with the TLV2553EVM.
- Powers all active circuitry on the TLV2553EVM board.

Along with the TLV2553EVM and PHI controller board, this demonstration kit includes an A-to-micro-B USB cable that is required for system setup.

1.1 TLV2553EVM-PDK Features

- Includes hardware and software required for diagnostic testing as well as accurate performance evaluation of the TLV2553 ADC.
- No external power supply is necessary.
- Ships with the PHI controller that provides a convenient interface to the EVM over a USB 2.0 (or higher) for power delivery as well as digital input and output.
- Easy-to-use evaluation software for all Windows® operating systems.
- The software suite includes graphical tools for multichannel data capture, output code histogram generation, and FFT analysis, as well as a provision for exporting data to a text file for post-processing.

1.2 TLV2553EVM Features

- Onboard, precision, op-amp buffers on every analog input channel to support a high input impedance (1 MΩ) and a low impedance ADC drive for optimal performance.
- Options for driving buffer inputs close to full-scale or 0 V using onboard dc voltage sources.
- Onboard precision voltage reference and low-impedance ADC reference drive circuit.
- Includes a +5-V low-dropout regulator (LDO) to regulate supply voltages to the ADC and drive circuits.
- Includes a 5-V to 3.3-V bidirectional digital level translator to interface with the host controller.

2 EVM Analog Interface

At a system level, the analog portion of the TLV2553 consists of the 11 analog input channels and the dc reference voltage input. As with most SAR ADCs, the analog inputs of the TLV2553 are not high-impedance ports. These inputs terminate in switched-capacitor networks that draw load current when the switches are closed. The dynamic nature of the load currents produces dynamic errors in the corresponding input voltage signals and ADC accuracy can degrade if these errors are not managed carefully. Low source impedance is critical to minimizing these errors; minimizing source impedance requires careful design of the ADC input signal paths.

2.1 ADC Analog Input Signal Path

The 11 analog input signal paths are designed so that the ADC provides accurate results even with signal sources that have relatively high output impedance. The schematic (for one channel) is shown in Figure 1.

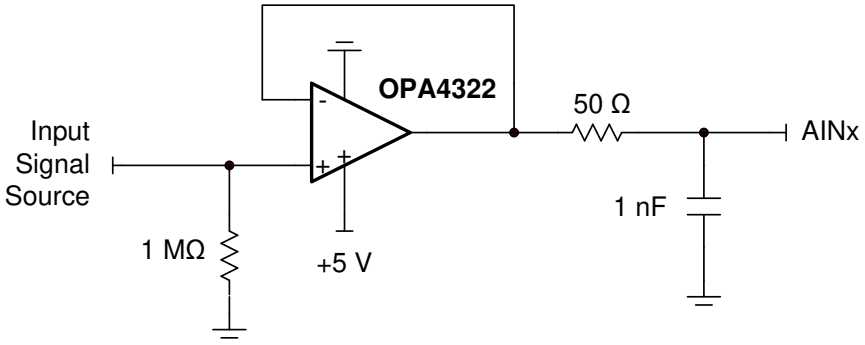

Figure 1. Input Signal Path Schematic (Single Channel)

The OPA4322 unity-gain buffers individually decouple the input signal source on each channel from the ADC input load current. The buffer inputs are pulled down to GND by the 1-MΩ resistors to ensure safe and predictable operating conditions on the board even when the inputs are left floating. Of course, the tradeoff with this approach is that the EVM analog input impedance is lower (only 1 MΩ) but the inputs can still support a wide range of source impedances without introducing significant gain error.

The buffered ADC inputs are accessible through the even-numbered pins of J2 (that is, J2.Pin2 through J2.Pin22). The odd-numbered pins of J2 (J2.Pin1 through J2.Pin27) are shorted together on the board and must be jumpered to any one of the even-numbered pins marked *GND* (J2.Pin28), *PFS* (J2.Pin26), or *NFS* (J2.Pin24), depending on whether the ADC inputs must be driven from an external source (such as a function generator, sensor, and so forth) or by one of the onboard sources.

Note that J2.Pin24 and J2.Pin26 are the outputs of the onboard dc voltage sources and have nominal values of approximately 100 mV and 4 V, respectively. These pins are useful for debugging any gross problems with the op-amp buffers or the ADC. However, for default operation (that is, inputs are from external sources), the odd-numbered pins of J2 must be connected to J2.Pin28 (GND). The jumper settings for J2 are summarized in Table 1.

Table 1. JP1 - JP2: Analog Interface Connections

ADC Input	Value	J2.Pin24 ↔ J2.Pin23	J2.Pin26 ↔ J2.Pin25	J2.Pin28 ↔ J2.Pin27
External	Any	Open	Open	Closed
PFS	4 V	Open	Closed	Open
NFS	100 mV	Closed	Open	Open

NOTE: In addition to configuring J2 according to Table 1, install shunts at the locations corresponding to the appropriate input channels as well.

2.2 Onboard ADC Reference

The EVM does not include a provision for driving the reference input of the TLV2553 from an external source. The reference input signal path is entirely self-contained on the TLV2553EVM and consists of the REF3240, a 4.096-V precision voltage reference whose output is heavily low-pass filtered and buffered by the OPA320, a precision op amp that has low output impedance over a sufficiently wide frequency range. The schematic is shown in Figure 2.

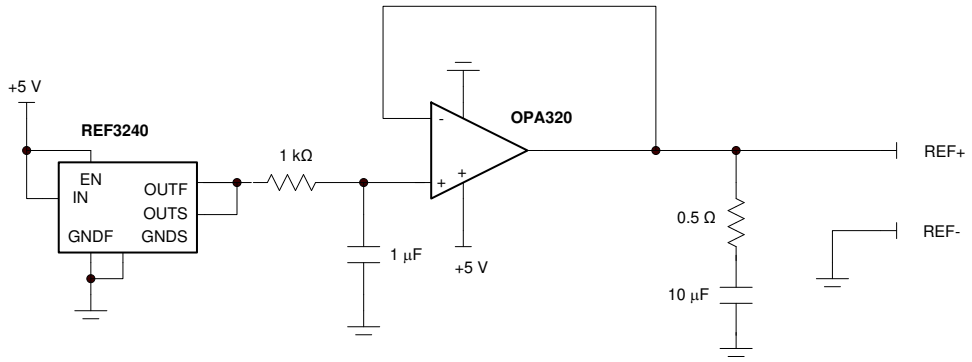

Figure 2. Onboard Reference Signal Path

The 10-µF ceramic capacitor at the output of the OPA320 provides additional load decoupling and effectively lowers the output impedance of the reference drive circuit at high frequencies.

3 Digital Interfaces

As noted in *Section 1*, the EVM interfaces with the PHI that, in turn, communicates with the computer over USB. There are two devices on the EVM with which the PHI communicates: the ADC (over SPI) and the EEPROM (over I^2C). The EEPROM comes pre-programmed with the information required to configure and initialize the TLV2553EVM-PDK platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 SPI for ADC Digital IO

The TLV2553EVM-PDK supports all three ADC interface modes (8-, 12-, and 16-bit modes), as detailed in the TLV2553 data sheet. MSB- or LSB-first options are also supported. An important note concerning the TLV2553 that is not clarified in the TLV2553 datasheet is that in 16-bit, LSB-first mode the four MSBs of the DATA OUT word are zeroes (compare this with Figure 37 of the TLV2553 datasheet).

The EVM uses a 5-V supply for powering the TLV2553, and therefore the ADC digital I/O interface operates on 5-V logic levels. However, the PHI requires 3.3-V logic levels for proper operation, and for this reason the EVM includes the TXB0106 (U8), a 5-V to 3.3-V bidirectional level translator.

The digital I/O lines also include 50-Ω series resistors to minimize ringing and delay mismatches between the SPI interface signals.

4 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the computer USB supply.

The EEPROM on the TLV2553EVM uses a common 3.3-V power supply and the digital level translator uses a separate 3.3-V supply (both directly from the PHI). On the other hand, the ADC and analog input drive circuits are powered by the TPS7A4901 onboard the EVM, which is a low-noise linear regulator that uses the 5-V supply out of a switching regulator on the PHI to generate a much cleaner 5-V output.

The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper fill areas where possible between bypass capacitors and their loads to minimize inductance along the load current path.

5 TLV2553EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for properly operating the TLV2553EVM-PDK.

5.1 Default Jumper Settings

Upon unpacking, the EVM is already configured with default jumper settings. J5 must be open and J2 must have shunts installed at the locations shown in Figure 3.

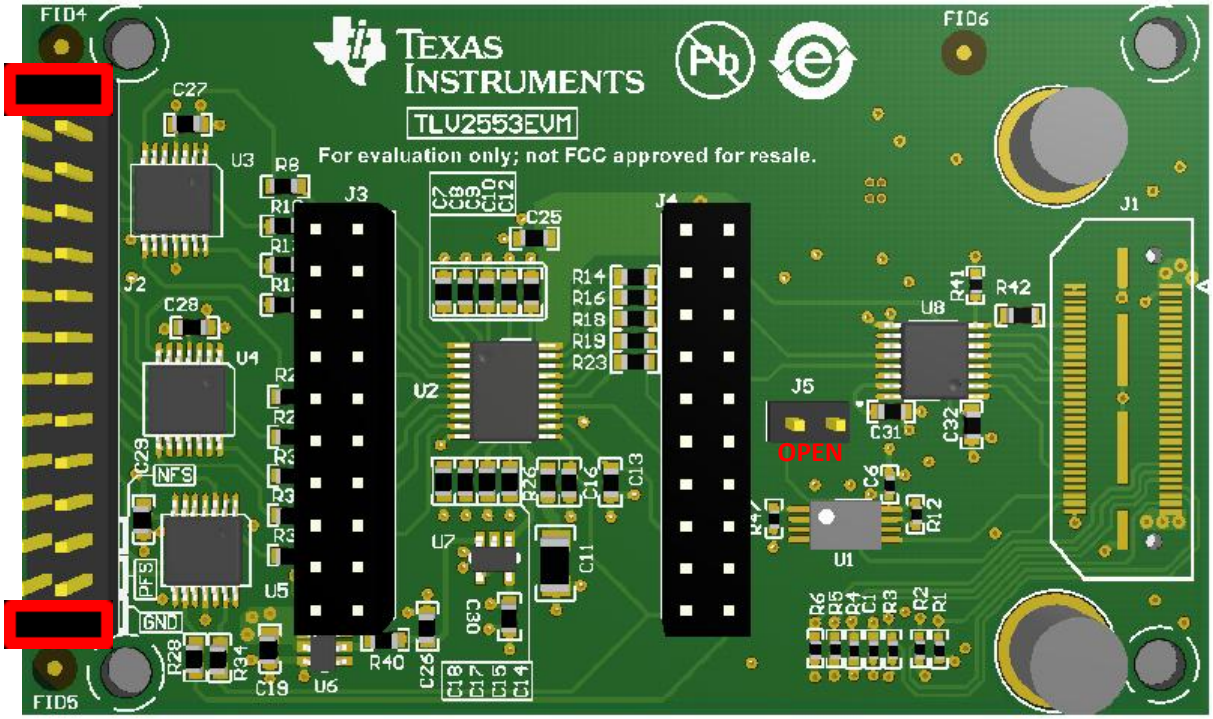

Figure 3. TLV2553EVM Default Jumper Settings

5.2 Connectors J3 and J4

J3 and J4 are for TI internal use only and are not installed by default. However, their pins can be used as test points (that is, for meter hookups only).

CAUTION

Do not drive the J3 or J4 pins with external voltage sources. Doing so may cause damage to the onboard sources.

5.3 EVM Graphical User Interface (GUI) Software Installation

The following steps describe how to install the software for the TLV2553 EVM graphical user interface (GUI).

1. Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the TLV2553EVM-PDK, and run the GUI installer to install the EVM GUI software on your computer.
2. Accept the license agreements as shown in Figure 4 and follow the onscreen instructions to complete the installation.

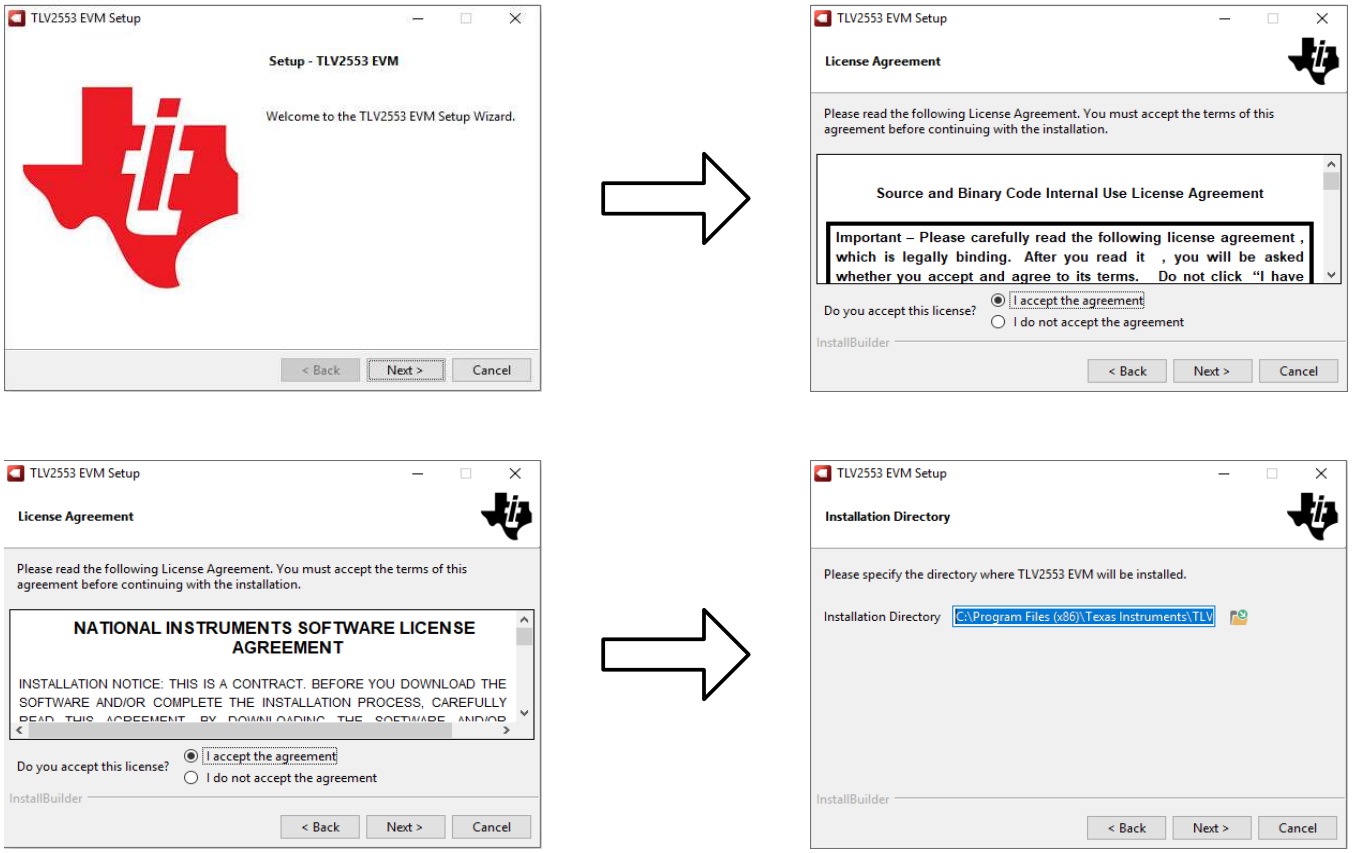

Figure 4. TLV2553 Software Installation Prompts

3. As a part of the TLV2553EVM GUI installation, a prompt with a device driver installation wizard shown in Figure 5 appears on the screen. Click the *Next* button to proceed, then click the *Finish* button when the installation is complete.

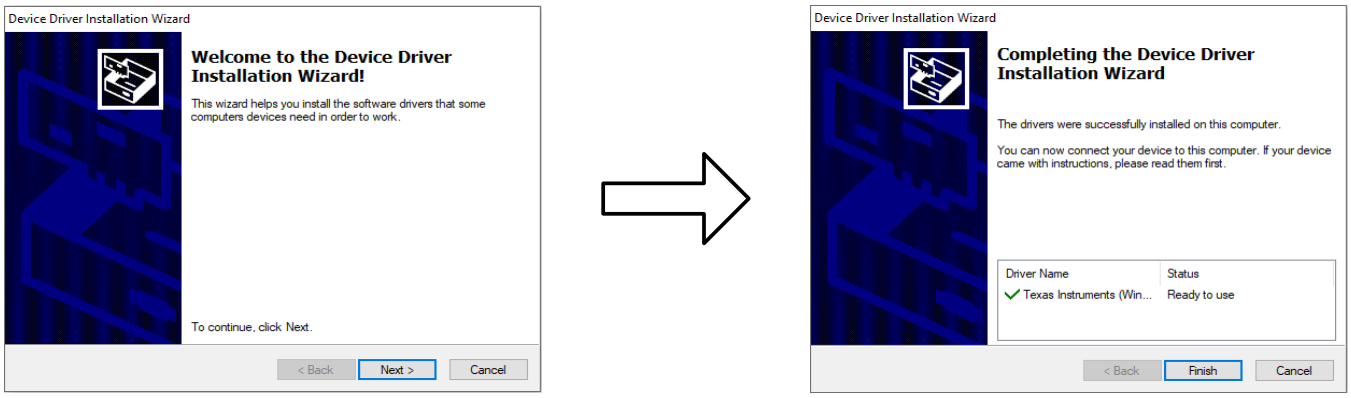

Figure 5. Device Driver Installation

NOTE: A notice may appear on the screen stating that Windows cannot verify the publisher of this driver software. Select the *Install this driver anyway* option.

The device requires the LabVIEW run-time engine (Figure 6) and may prompt for the installation of this software, if not already installed.

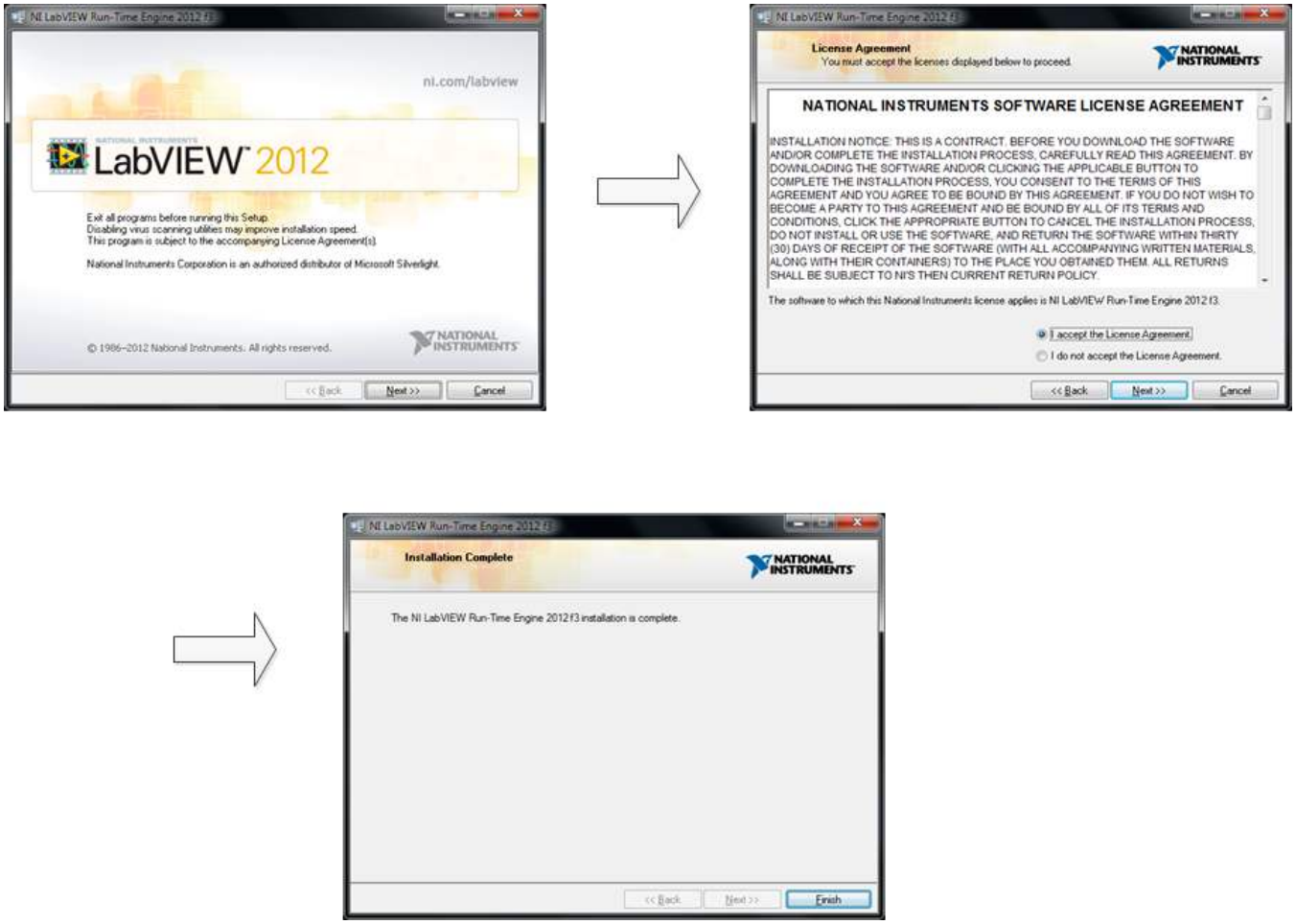

Figure 6. LabVIEW Run-Time Engine Installation

4. If you would like a Desktop shortcut, check the *Create Desktop Shortcut* box, as shown in Figure 7.

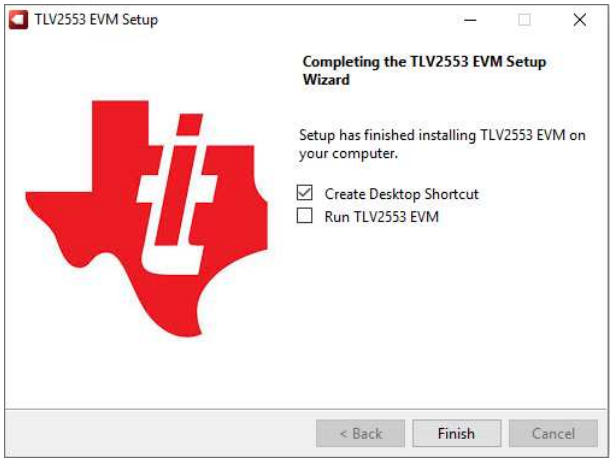

Figure 7. TLV2553EVM-PDK Installation Final Step

6 TLV2553EVM-PDK Operation

The following instructions are a step-by-step guide to connecting the TLV2553EVM-PDK to the computer and evaluating the performance of the TLV2553:

1. Ensure that no SD card is installed in the SD card slot J6. The SD card is not required to boot up the TLV2553EVM-PDK with the PHI.
2. Connect the TLV2553EVM to the PHI, and install the two screws, as indicated in Figure 8.
3. Use the USB cable provided to connect the PHI to the computer.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up.
   - LEDs D1 and D2 of the PHI starts blinking to indicate that the PHI is communicating with the EVM. The resulting LED indicators are shown in Figure 8.

Figure 8. EVM-PDK Hardware Setup and LED Indicators

4. Double-click on the *TLV2553 EVM.exe* file to launch the TLV2553EVM-PDK GUI software. TheTLV2553EVM GUI software folder is shown in Figure 9.

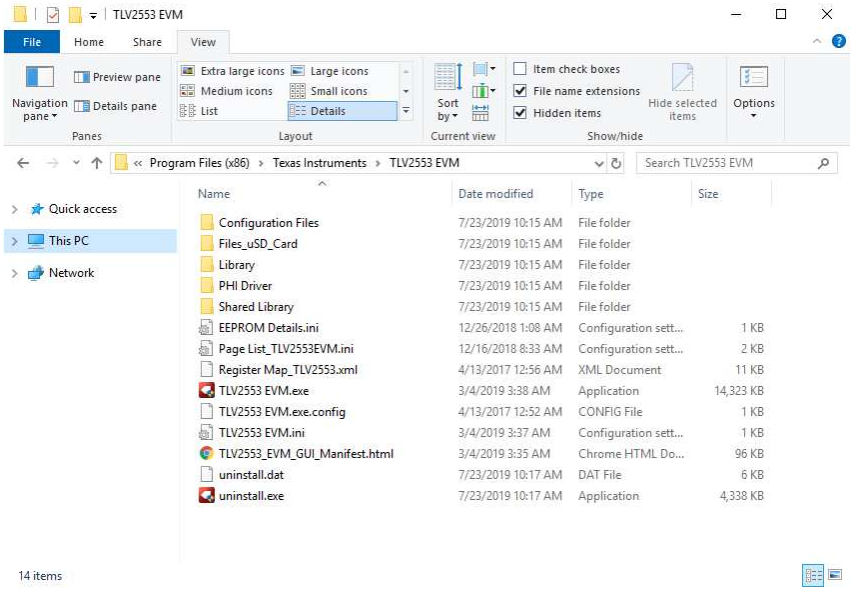

Figure 9. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the levels and timing configuration of the ADC digital interface, the EVM GUI does give users high-level control over virtually all functions of the TLV2553 (such as interface modes, sampling rate, input channel selection, and number of samples per channel). Only the software power-down and output format control are not supported.

Figure 10 identifies the input parameters of the GUI (as well as their default values) through which the various functions of the TLV2553 can be exercised. These are global settings because they persist from one tool to another (or from one page to another).

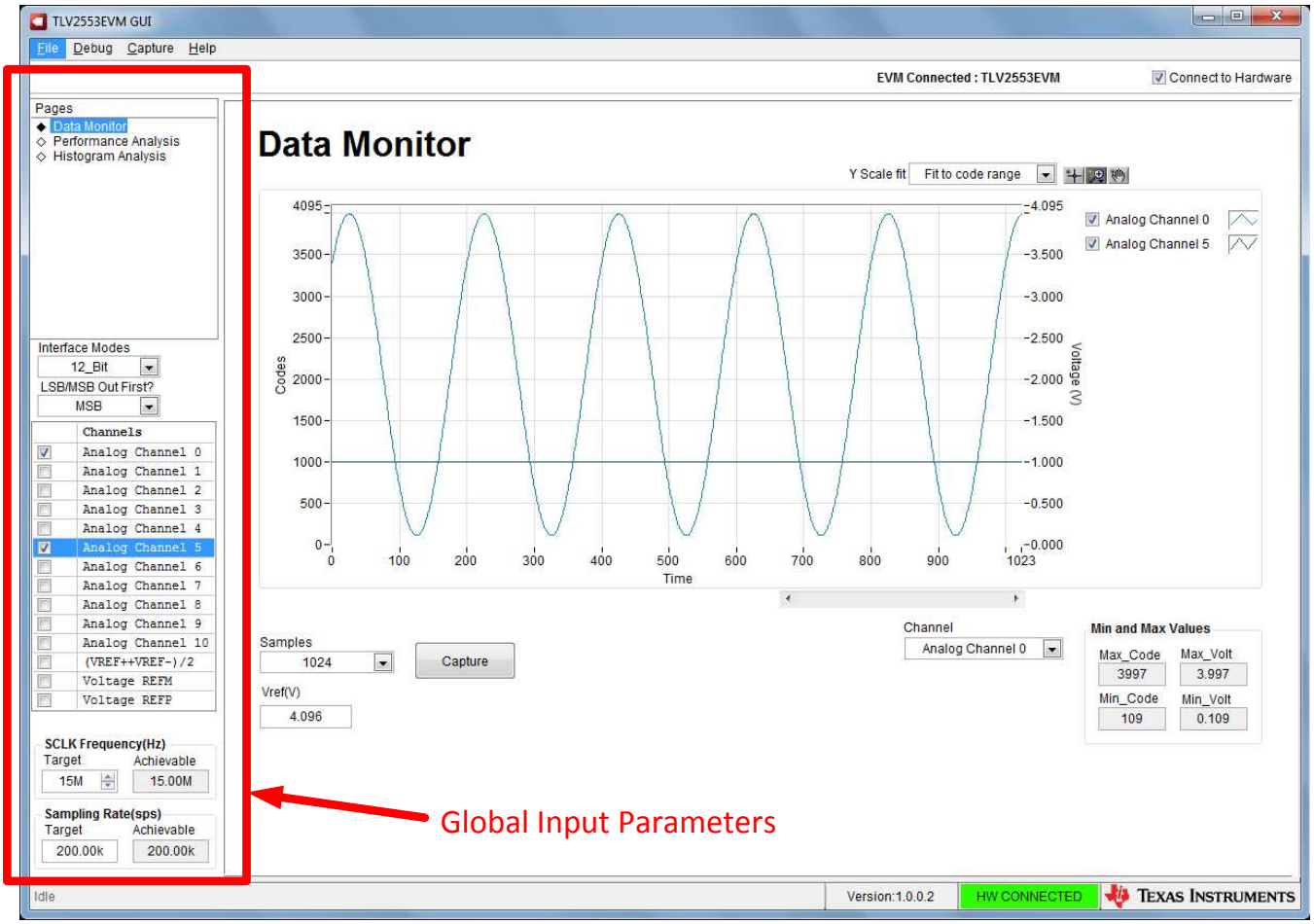

Figure 10. EVM GUI Global Input Parameters

NOTE: The GUI allows multiple input channels to be addressed, one at a time. However, channel addressing is performed only in ascending order. There is no provision for users to specify a desired channel scanning order.

NOTE: The last three of the 14 analog input channels are the internal self-test inputs, command register (CMR) addresses 11 through 13, as described in Table 2 of the TLV2553 data sheet.

Section 6.2 and *Section 6.3* describe the data collection and analysis features of the EVM GUI.

6.2 Data Capture Tool

The data capture tool allows visualization of the ADC transient response. This tool is useful for debugging any gross problems with the ADC or drive circuits.

The tool allows ADC conversion data corresponding to multiple input channels to be overlaid on the same set of axes. As shown in Figure 11, channel 0 has a full-scale sinusoidal input signal applied to it and channel 5 is at a constant 1 V.

The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. In addition, raw data can be exported to a text file, as shown in Figure 11.

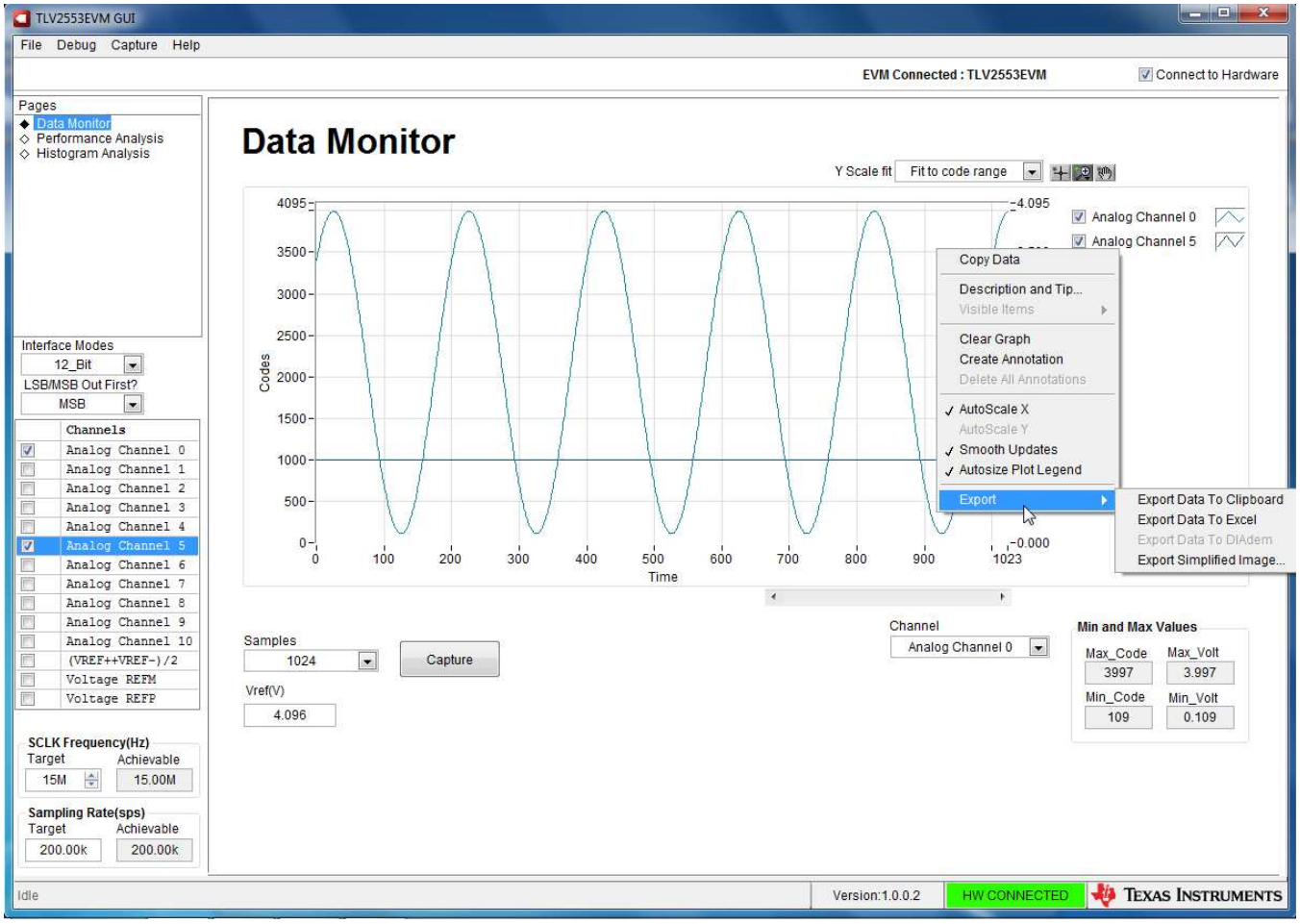

Figure 11. Multichannel Acquisition and Data Export Options

6.3 Histogram Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate *effective resolution*, which is an indicator of the number of bits of ADC resolution lost resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel. In other words, the histogram standard deviation (σDC) is equivalent to the RMS value of the ADC output noise (NRMS_ADCOUT) for a dc input, as described in Equation 1:

$$N_{RMS}\_ADCOUT = \sigma DC \rightarrow (1) \quad (1)$$

Effective resolution can then be computed by definition, as shown in Equation 2:

$$\text{Effective Resolution (bits)} = 12 - \text{LOG}_2\,(N_{RMS\_ADCOUT}) = 12 - \text{LOG}_2\,(\sigma DC) \rightarrow (2) \quad (2)$$

Note that in the case of the TLV2553EVM, the onboard ADC drive circuits and power supply are all optimized for a low noise contribution. Therefore, assuming the EVM analog inputs are driven by low-noise dc voltage sources, the ADC RMS output noise is dominated by the intrinsic thermal noise of the TLV2553 itself, which is generally less than 1-LSB RMS. As a result, Equation 2 produces a value of effective resolution that is greater than 12 bits (which is of course not possible but desirable nonetheless). If however, the input signal source has significant noise contribution, then σDC may exceed 1 LSB in which case the effective resolution drops to a value less than 12 bits, indicating a loss of resolution.

Again, the histogram tool offers multichannel functionality. However, the histogram corresponding to a single input channel is displayed at any time, as shown in Figure 12.

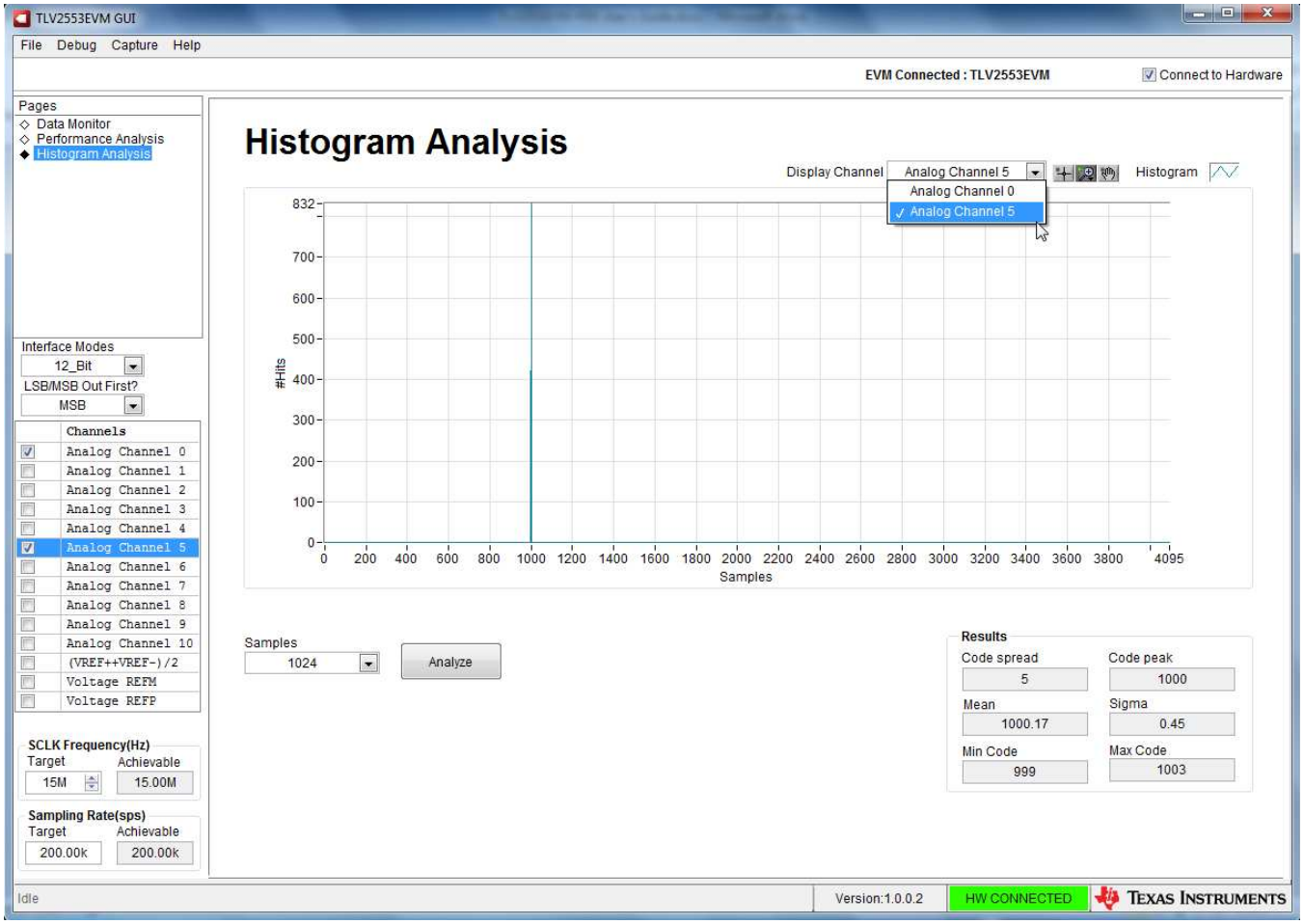

Figure 12. Histogram Tool Input Channel Selection

6.4 Performance (or FFT) Analysis Tool

This tool is for evaluating the dynamic performance of the TLV2553EVM through FFT analysis of the ADC output for time-varying inputs and computation of key dynamic range metrics (such as SNR, THD, SFDR, SINAD, and ENOB).

The analog input channel of interest can be selected as shown in Figure 13.

The expected ADC input is a sinusoidal signal of peak-to-peak amplitude close to the ADC full-scale input range (FSR). The RMS power of the input signal normalized to FSR is shown in the *Signal Power (dB)* field and must be approximately –0.5 dBFS (or approximately 95% × FSR) to avoid input clipping.

The sampling rate of the ADC can be adjusted by modifying the *Target Sampling Rate (Hz)* argument, which is a global setting (it affects all tools). The achievable ADC sampling rate may differ from the target value, depending on the applied SCLK frequency and PHI PLL settings. Note that the user is also required to specify a target SCLK frequency that the tool tries to match as exactly as possible by changing the PHI PLL settings in an iterative fashion until convergence.

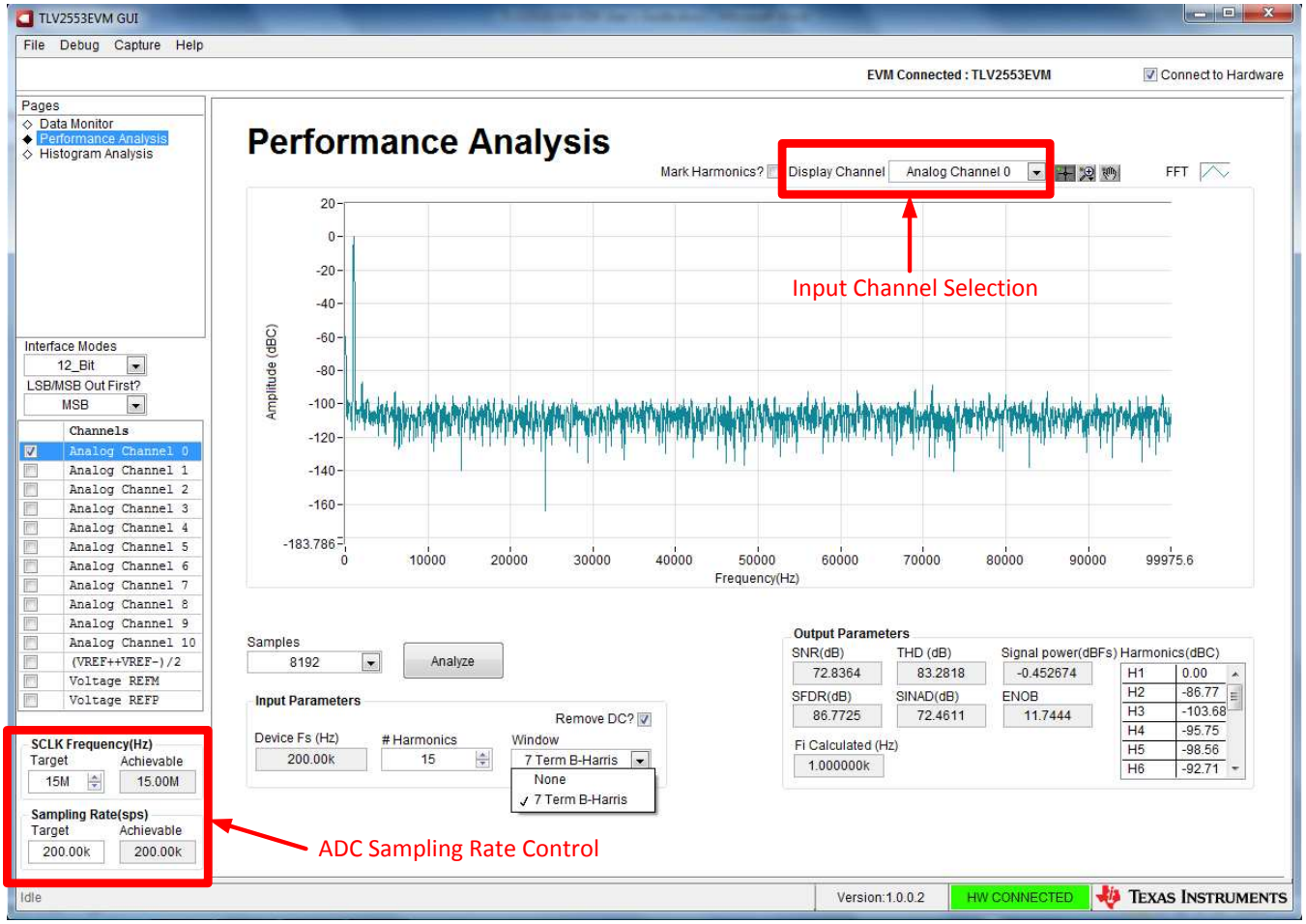

Figure 13. FFT Tool Input Parameters

Finally, the FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The *7-Term Blackman Harris* window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. Note that the *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

7 Bill of Materials, PCB Layout, and Schematics

Table 2. TLV2553EVM Bill of Materials

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
1891	4	For H1-H4	KEYSTONE ELECTRONICS	HEX STANDOFF 4-40 ALUMINUM 1/4"
9900	4	For H1-H4	KEYSTONE ELECTRONICS	MACHINE SCREW PAN PHILLIPS 4-40
RM3X4MM 2701	2	For J1	APM HEXSEAL	MACHINE SCREW PAN PHILLIPS M3
NPC02SXON-RC	2	For J2	SULLINS CONNECTOR SOLUTIONS	CONN JUMPER SHORTING .100" GOLD
C1005X7R1H104K050BB	2	C1, C6	TDK CORPORATION (VA)	CAP CER 0.1UF 50V 10% X7R 0402
GRM188R71C474KA88D	1	C19	MURATA ELECTRONICS (VA)	CAP CER 0.47UF 16V 10% X7R 0603
C1608C0G1E103J080AA	2	C21, C22	TDK CORPORATION (VA)	CAP CER 10000PF 25V 5% C0G 0603
C2012X7R1E105K125AB	1	C23	TDK CORPORATION (VA)	CAP CER 1UF 25V 10% X7R 0805
C0603C104J3RACTU	7	C25, C27-C32	KEMET (VA)	CAP CER 0.1UF 25V 5% X7R 0603
GRM188R71E105KA12D	3	C26, C33, C34	MURATA ELECTRONICS (VA)	CAP CER 1UF 25V 10% X7R 0603
CL31B106KAHNNNE	4	C3, C5, C11, C24	SAMSUNG ELECTRO-MECHANICS AMERICA, INC (VA)	CAP CER 10UF 25V 10% X7R 1206
GRM1885C1H102JA01D	11	C7-C10, C12-C18	MURATA ELECTRONICS (VA)	CAP CER 1000PF 50V 5% NP0 0603
9774050360R	2	H5, H6	WURTH ELECTRONICS INC	ROUND STANDOFF M3 STEEL 5MM
QTH-030-01-F-D-A	1	J1	SAMTEC INC	CONN HEADER 60POS 0.5MM SMT
TSW-114-07-G-D	1	J2	SAMTEC INC (VA)	CONN HEADER 28POS .100" DL GOLD
SSW-110-23-F-D	2	J3, J4	SAMTEC	CONN RECEPTACLE 20 POS .100"
TSW-102-07-G-S	1	J5	SAMTEC INC (VA)	CONN HEADER 2POS .100" SGL GOLD
5025700893	1	J6	MOLEX INC (VA)	CONN MICRO SD CARD PUSH-PUSH R/A
RC0402FR-0710KL	9	R1-R6, R12, R41, R47	YAGEO (VA)	RES SMD 10K OHM 1% 1/16W 0402
ERA-6AEB6043V	1	R21	PANASONIC ELECTRONIC COMPONENTS (VA)	RES SMD 604K OHM 0.1% 1/8W 0805
ERJ-6ENF1873V	1	R22	PANASONIC ELECTRONIC COMPONENTS (VA)	RES SMD 187K OHM 1% 1/8W 0805
RL0603FR-070R5L	1	R26	YAGEO (VA)	RES SMD 0.5 OHM 1% 1/10W 0603
ERJ-3EKF1001V	1	R40	PANASONIC ELECTRONIC COMPONENTS (VA)	RES SMD 1K OHM 1% 1/10W 0603
ERJ-3GEY0R00V	1	R42	PANASONIC ELECTRONIC COMPONENTS (VA)	RES SMD 0.0 OHM JUMPER 1/10W
RC0603FR-07240RL	2	R43, R46	YAGEO (VA)	RES SMD 240 OHM 1% 1/10W 0603
RC0603FR-0710KL	2	R44, R45	YAGEO (VA)	RES SMD 10K OHM 1% 1/10W 0603
RC0402FR-071ML	11	R7, R9, R11, R15, R20, R27, R29, R33, R35, R31, R37	YAGEO (VA)	RES SMD 1M OHM 1% 1/16W 0402
ERJ-3EKF49R9V	16	R8, R10, R13, R14, R16-R19, R23-R25, R28, R30, R32, R34, R36	PANASONIC ELECTRONIC COMPONENTS (VA)	RES SMD 49.9 OHM 1% 1/10W 0603
BR24G32FVT-3AGE2	1	U1	ROHM SEMICONDUCTOR (VA)	IC EEPROM I2C BUS 32KBIT 8TSSOP
TPS7A4901DGN	1	U12	TEXAS INSTRUMENTS	
TLV2553IPW	1	U2	TEXAS INSTRUMENTS	IC 12BIT 200KSPS SER ADC 20TSSOP
OPA4322AIPW	3	U3-U5	TEXAS INSTRUMENTS	IC OPAMP GP 20MHZ RRO 14TSSOP
REF3240AIDBV	1	U6	TEXAS INSTRUMENTS	
OPA320AIDBVR	1	U7	TEXAS INSTRUMENTS (VA)	IC OPAMP GP 20MHZ RRO SOT23-5
TXB0106PWR	1	U8	TEXAS INSTRUMENTS (VA)	IC 6BIT NON-INV TRANSLTR 16TSSOP

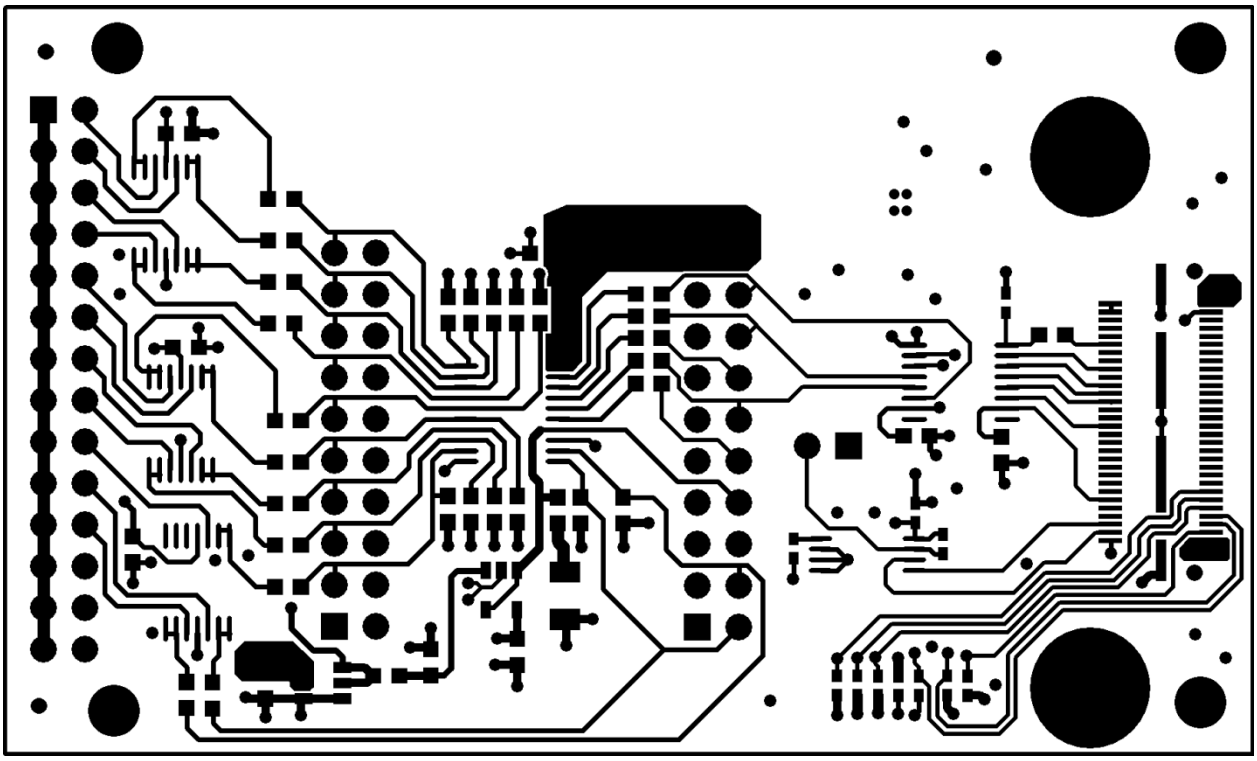

Figure 14. TLV2553EVM PCB Layer 1: Top Layer

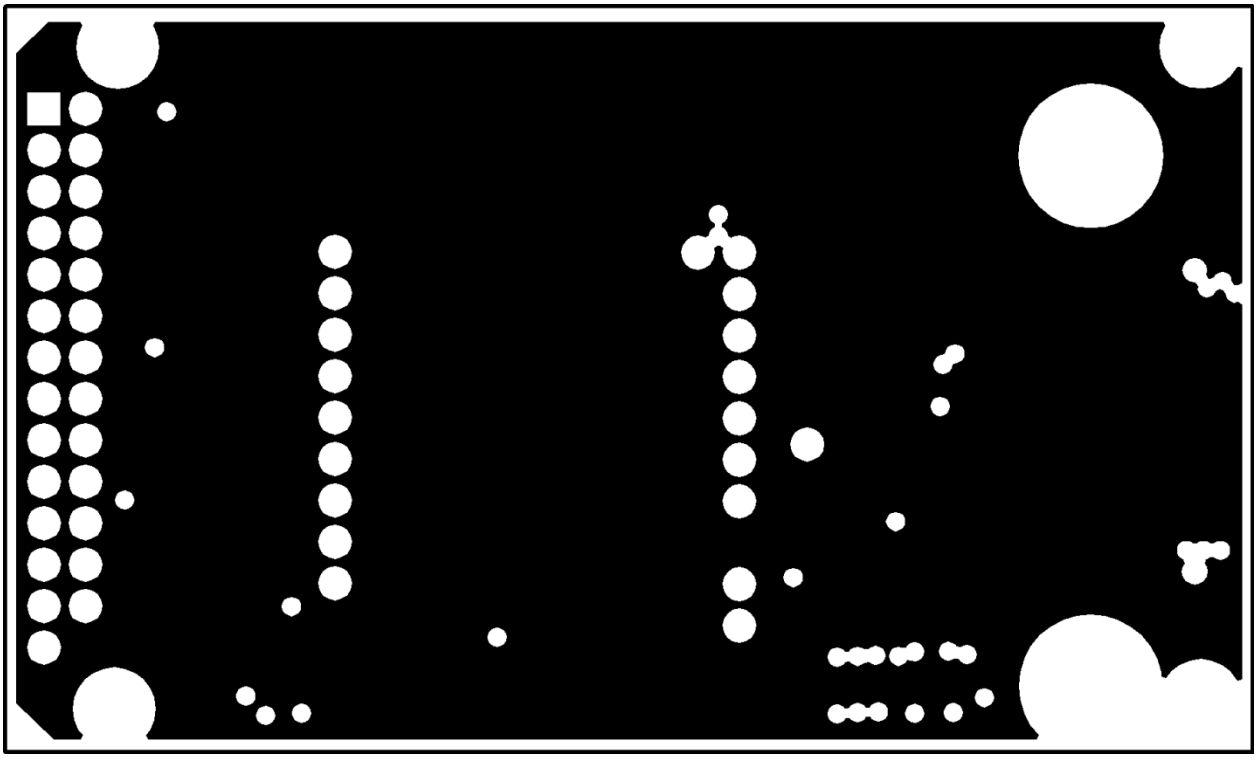

Figure 15. TLV2553EVM PCB Layer 2: GND Plane

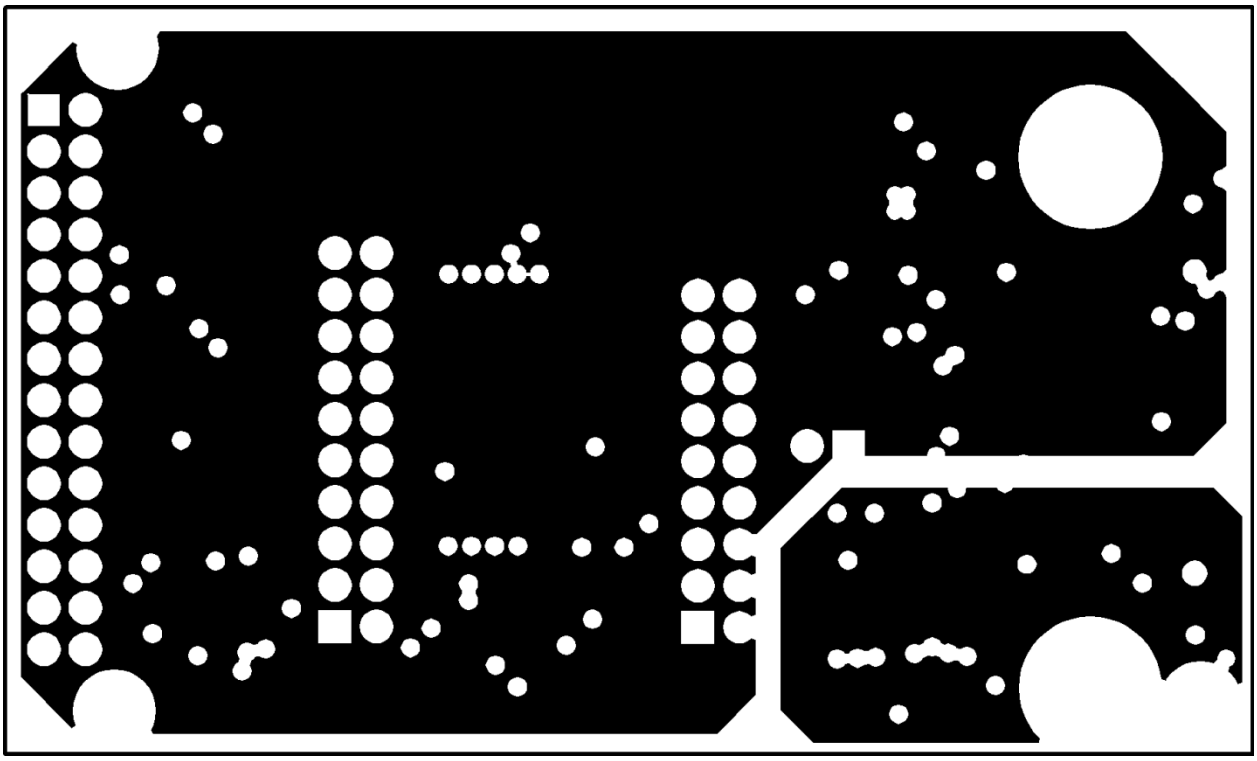

Figure 16. TLV2553EVM PCB Layer 3: Power Planes

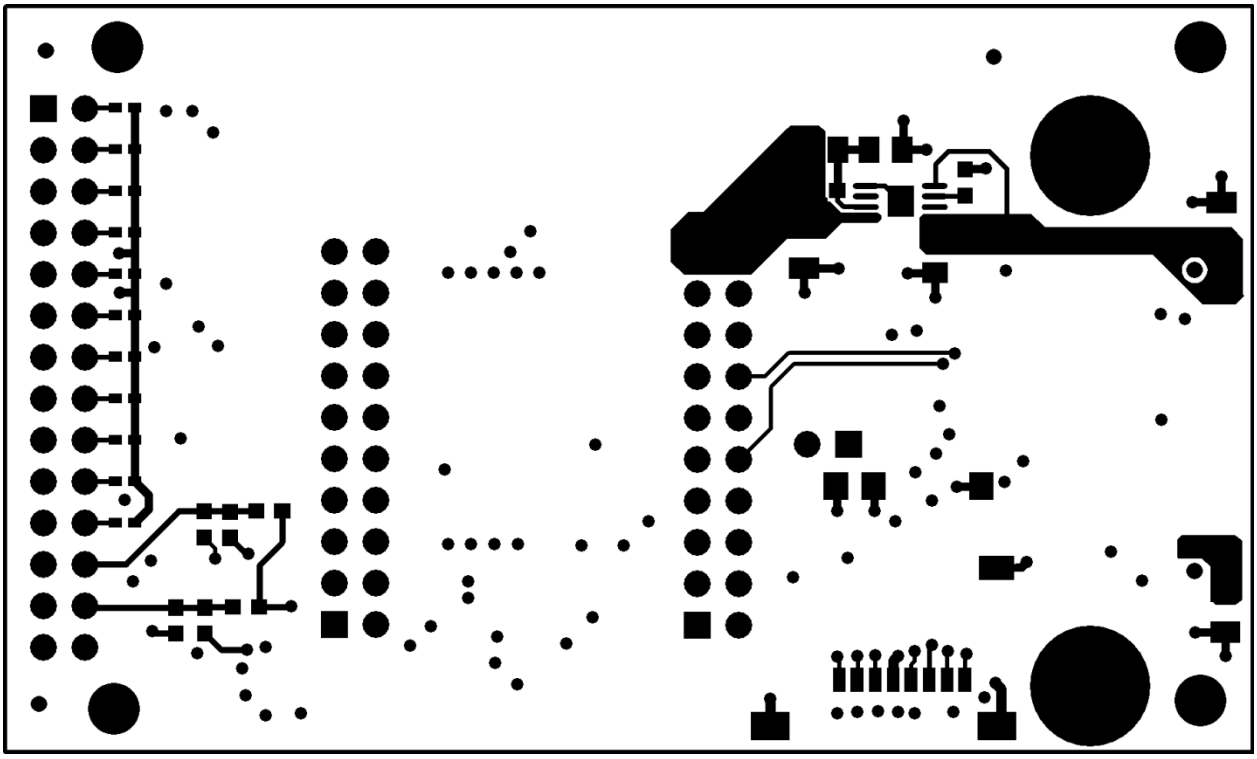

Figure 17. TLV2553EVM PCB Layer 4: Bottom Layer

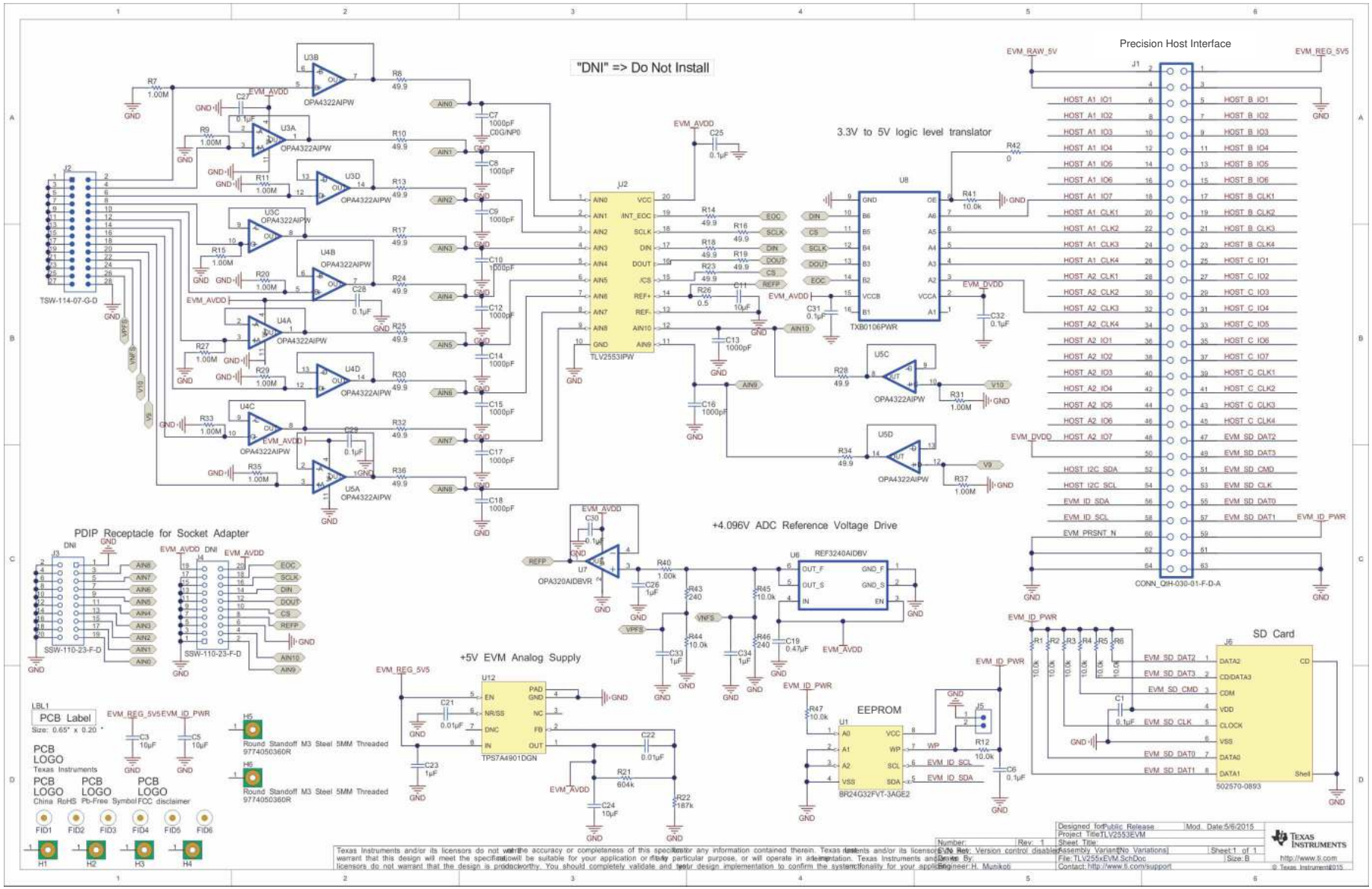

Figure 18. Schematic Diagram of the TLV2553EVM PCB

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2015) to A Revision **Page**

- Changed TLV2553EVM-PDK board image 1
- Changed SDCC to PHI throughout document 3
- Deleted all references to microSD memory card from document 3
- Changed *Windows® 7 and Windows® 8 operating systems* to *all Windows® operating systems* 3
- Changed *EVM Graphical User Interface (GUI) Software Installation* section 7
- Changed *TLV2553EVM-PDK Operation* section 10
- Deleted SD card from Bill of Materials 15

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