User's Guide
SLVU207–April 2007

TPS6120xEVM-179

The TPS6120xEVM-179 is specially designed and optimized to operate from a single-cell, two-cell, or three-cell alkaline, NiCd or NiMH, as well as a one-cell Li-Ion or Li-polymer battery. It is also used in single-cell fuel cell or solar cell battery applications where the input voltage is as low as 0.3V.

The TPS6120xEVM-179 operates from a 0.3V to 5.5V (starts up ≥ 0.5V) input rail and provides a single output voltage up to 5.5V.

The TPS6120xEVM-179 has three orderable EVMs shown in Table 1.

Table 1. EVM Description

Build	EVM	Note
-001	TPS61200EVM-179	Evaluates the TPS61200. Adjustable output voltage version which default output voltage is 3.3V.
-002	TPS61201EVM-179	Evaluates the TPS61201. Fixed 3.3V_output voltage version
-003	TPS61202EVM-179	Evaluates the TPS61202. Fixed 5.0V_output voltage version

Contents

List of Figures

List of Tables

1 Introduction

This chapter contains background information for the TPS6120xEVM-179 evaluation module.

1.1 Specifications

Table 2 provides a summary of the TPS6120xEVM-179 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 2. Specification Summary

Build	Specification	Voltage Range (V)			Current Range (A)		
		Min	Typ	Max	Min	Typ	Max
-001, -002, -003	VBAT	0.3		5.5			
-001, -002	VOUT	3.2	3.3	3.4			1.5
-003	VOUT	4.85	5	5.15			1.1

1.2 Modifications

This EVM facilitates user evaluation of the TPS61200/01/02. To facilitate user customization of the EVM, the board is designed with devices having 603 or larger footprints. Normal applications will likely occupy less total board space.

The TPS61200 provides adjustable output capability. The output is user adjustable using the feedback resistors (R4 and R5). The values for these resistors are chosen using the method described in the *Programming the Output Voltage* section of the data sheet (SLVS577). The output voltage of the TPS61201 and TPS61202 is factory programmed and cannot be changed.

2 Setup and Operation

This chapter explains the input, output, and jumper connections of the TPS6120xEVM-179. It also provides guidance on how to set up test equipment for evaluating the EVM and provides test results.

2.1 Connections and Jumpers

The DEFAULT jumper settings for the EVM are shown in Table 3.

Table 3. Default Jumper Settings

Jumper	Default Setting
JP1 – EN	GND
JP2 – PS	VBAT

J1 - VBAT: This is the positive connection to the input power supply.

J2 - GND: This is the ground connection for input power supply.

J3 – VOUT: This is the positive connection to the output voltage. VOUT regulates to 3.3V for the TPS61200 and TPS61201 EVMs, and VOUT regulates to 5V for the TPS61202 EVM.

J4 – GND: This is the ground connection for the output voltage.

JP1 - EN: This is the enable input for the device. Place a shunt across the VBAT and EN pins of JP1 to enable the IC. Place a shunt across the GND and EN pins of JP1 to disable the IC. A shunt must be installed on JP1 in either VBAT or GND positions and EN should not be left unconnected.

JP2 - PS: This jumper enables or disables the power save mode at light load. Place a shunt across the VBAT and PS pins of JP2 to disable power save mode. Place a shunt across the GND and PS pins of JP2 to enable power save mode. Note that while operating in down conversion mode (VBAT > Vout), power save mode is always enabled and the device cannot be forced into fixed frequency operation. A shunt must be installed on JP2 in either VBAT or GND positions and PS should not be left unconnected.

2.2 Setup

The power supply should have at least 2A capability. Connect an input power supply between J1 and J2. Initially the voltage range on this supply to start up the converter should be between 0.5V and 5.5V due to the minimum start up voltage requirement. Following startup, the input can be as low as 0.3V. Connect the load between J3 and J4.

Before enabling this device by connecting the EN pin to VBAT at JP1, make sure the measured input voltage between J1 and J2 does not exceed 5.5V and JP2 (PS pin) is connected to the desired setting.

In order to avoid voltage drop through the input power supply line, use at least 20 gauge wire. The output voltages can be monitored by voltmeters and/or an oscilloscope with standard high impedance voltage probes.

2.3 Operation

Once the input voltage is connected and verified, connect the EN pin to VBAT at JP1. The converter starts up and regulates to the set output voltage. The range for the output regulation is shown in Table 2.

After the converter starts up, the input voltage can go down to 0.3V. Figure 1 and Figure 2 show measured data from the EVM for maximum output current and efficiency at various input/output voltage combinations.

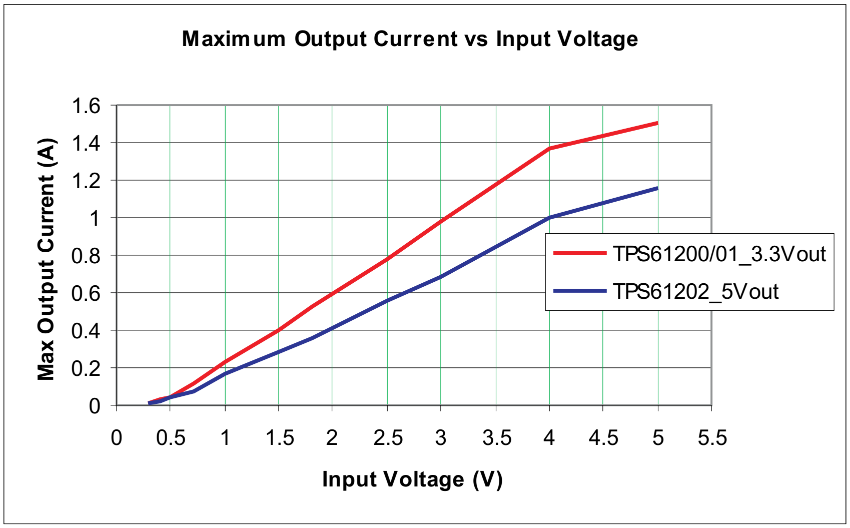

Figure 1. Maximum Output Current vs VBAT

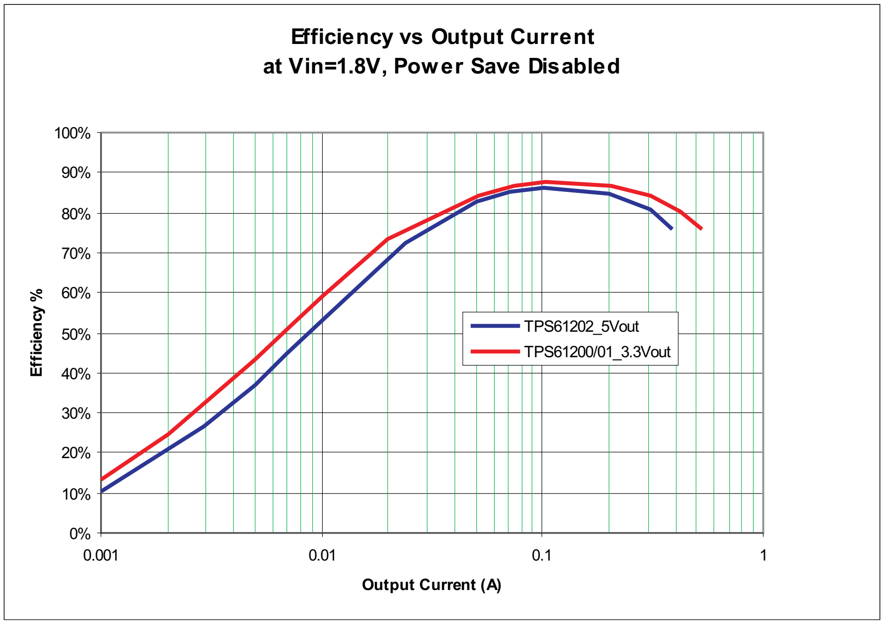

Figure 2. Efficiency vs Output Current

3 Board Layout

This chapter provides board layout recommendations as well as figures of the EVM board layers.

3.1 Board Layout Recommendations

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To layout the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can be due to superimposition of power ground current and control ground current.

3.2 Board Layers

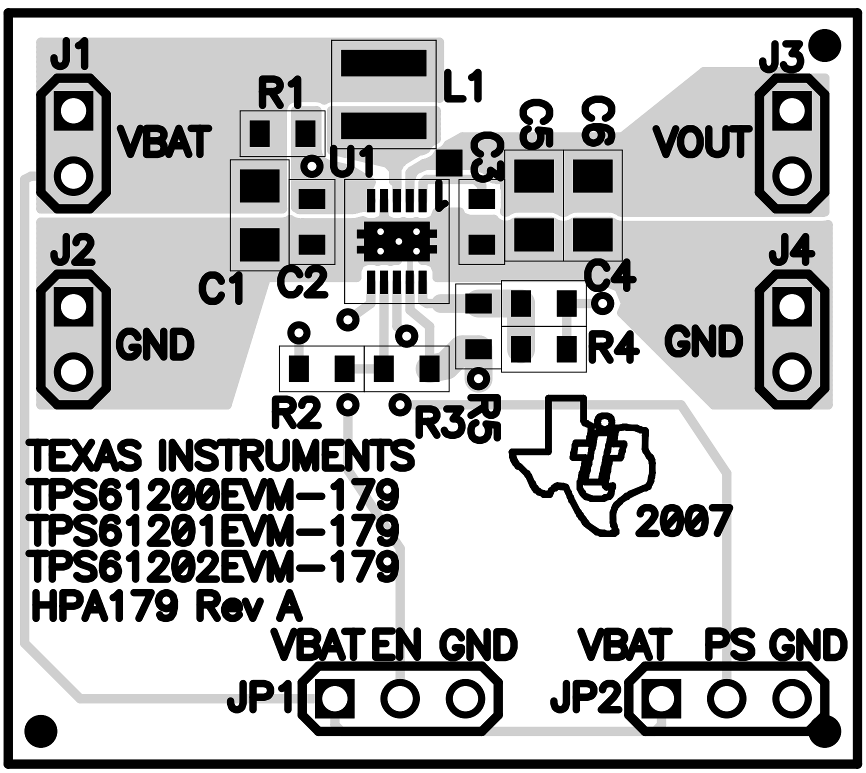

Figure 3. Top Assembly Layer

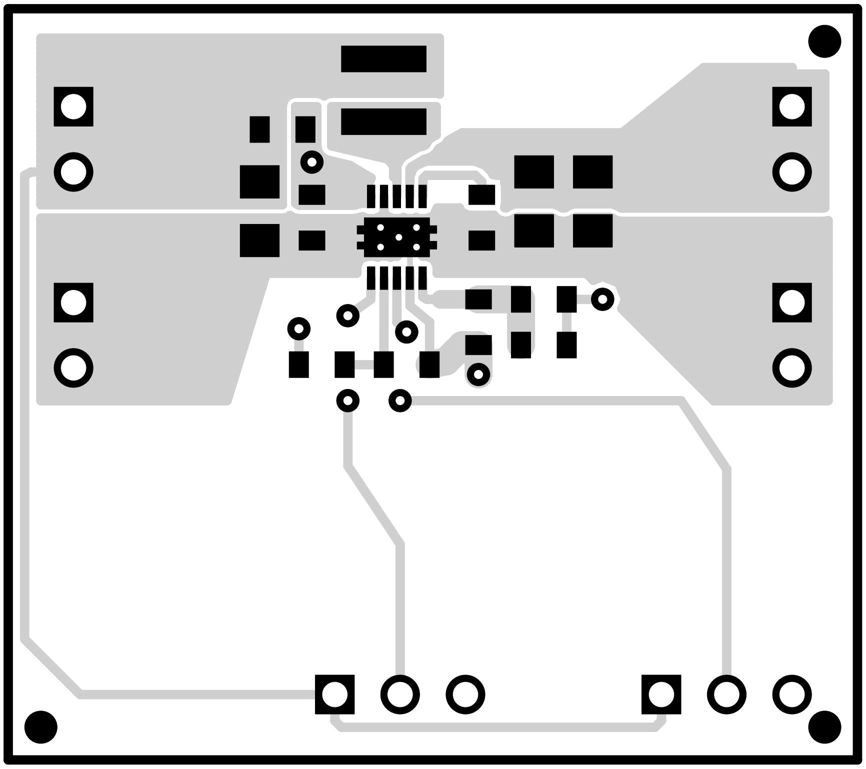

Figure 4. Top Layer

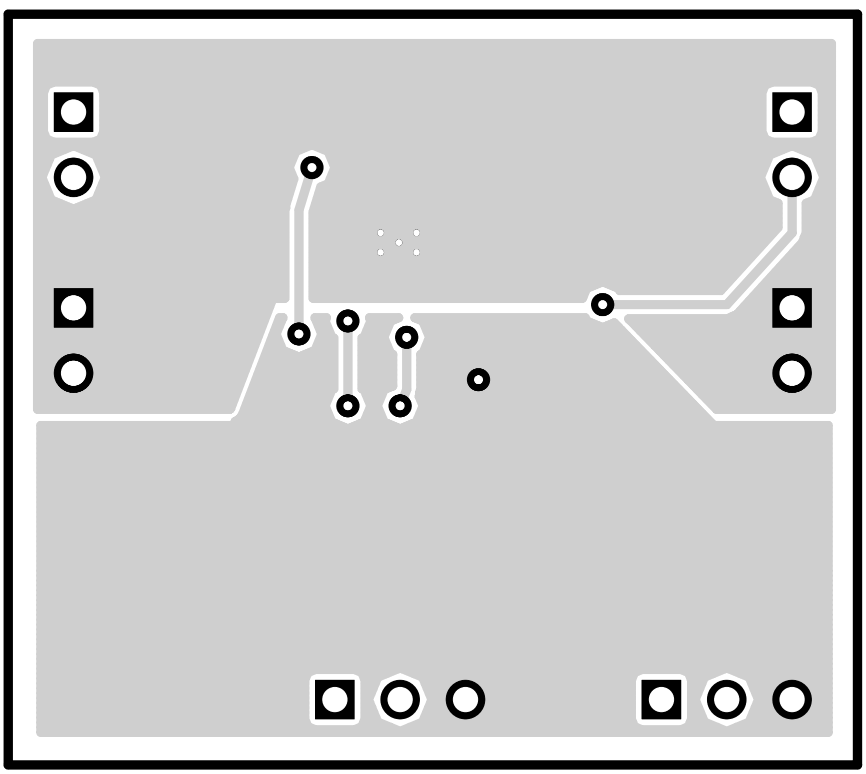

Figure 5. Bottom Layer

4 Schematic and Bill of Materials

4.1 Schematic

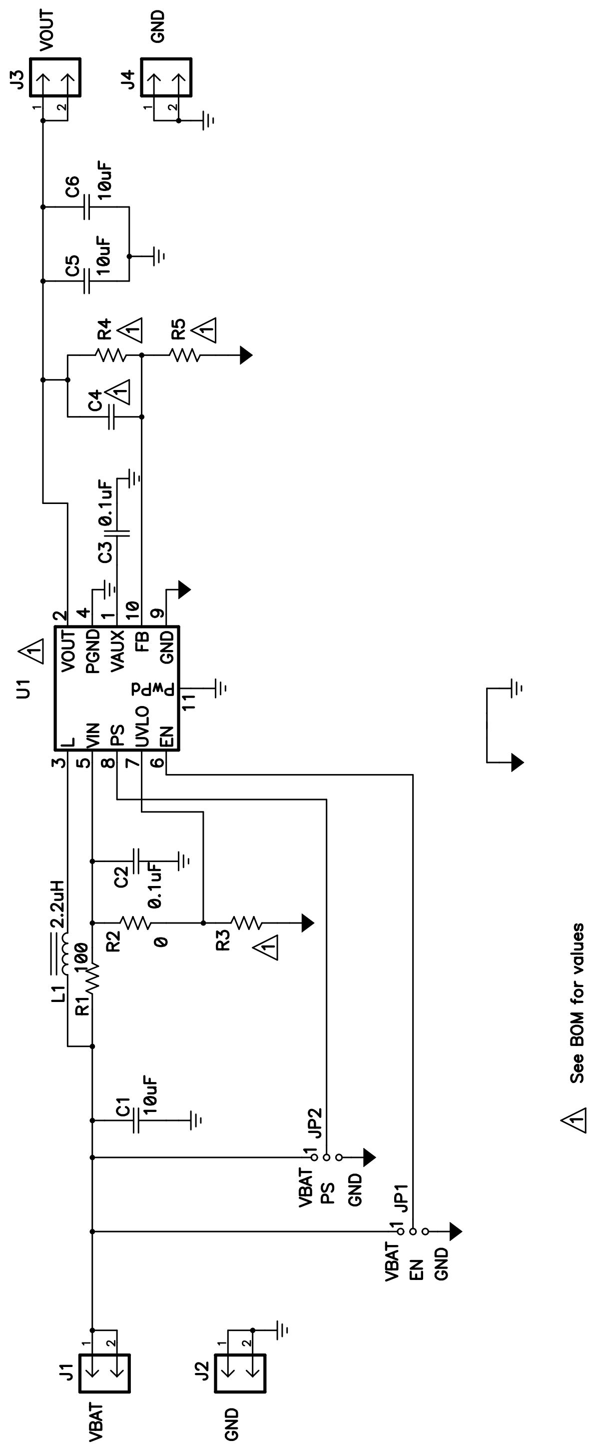

Figure 6. TPS6120xEVM-179 Schematic

4.2 Bill of Materials

Table 4. Bill of Materials

Count			RefDes	Value	Description	Size	Part Number	MFR
-001	-002	-003						
1	1	1	C1	10μF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	muRata
2	2	2	C2,C3	0.1μF	Capacitor, Ceramic, 16V, X7R, 10%	0603	C1608X7R1C104K	TDK
0	0	0	C4	Open	Capacitor, Ceramic	0603		
2	2	2	C5C6	10μF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	muRata
4	4	4	J1 – J4		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 X 2	PTC36SAAN	Sullins
2	2	2	JP1, JP2		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 X 3	PTC36SAAN	Sullins
1	1	1	L1	2.2μH	Inductor, SMT, 1.5A, 110milliohm	0.118 X 0.118	LPS3015-222ML	Coilcraft
1	1	1	R1	100Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R2	0Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
0	0	0	R3	Open	Resistor, Chip, 1/16W	0603		
1	0	0	R4	1.00MΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	1	1		0Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	0	0	R5	178kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	0	0	U1		IC, Very Low Input Voltage Sync. Boost Converter w/1.5A Switches, Adj V	SON-10	TPS61200DRC	TI
0	1	0			IC, Very Low Input Voltage Sync. Boost Converter w/1.5A Switches, 3.3V	SON-10	TPS61201DRC	TI
0	0	1			IC, Very Low Input Voltage Sync. Boost Converter w/1.5A Switches, 5V	SON-10	TPS61202DRC	TI
1	1	1	–		PCB, 1.3 In x 1.15 In x 0.062 In		HPA179	Any
2	2	2	–		Shunt, 100 mil, Black	0.100	929950-00	3M

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0.3V to 5.5V and the output voltage range of 1.8V to 5.5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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