Application Note on Sample Board Operation of the MASW-000834-13560T T/R Switch

The following is an application guide for utilization of the MASW-000834-13560T in conjunction with a supplied sample board from M/ACOM. The guide will review the operation of the T/R using a single positive supply as well as other optional dual polarity supplies.

The MASW-000834-13560T is a T/R switch with two PIN diodes in series in a common anode configuration and one PIN diode in shunt on the Rx path. The switch die along with select matching components are mounted in a standard 4mm MLP 16 lead package (Figure 1). The switch die utilizes M/ACOM's patented HMIC™ process. The backside of the switch die is thermally grounded while electrically isolated. The excellent power handling of the die is achieved through specific techniques using unique thermal conductive epoxy embedded in the die. This allows the heat to be transferred from the series connected device to ground while maintaining electrical isolation. The large backside of the pad of the package is both thermal and electrical ground. Figure 2 shows the electrical/ thermal schematic of the device.

The sample board is made of Rogers RO4350 material 10mils thick dielectric with added layers to increase the board thickness to 62mils for handling, rigidity and connector mounting. There are on-board bias networks incorporated to accommodate biasing the device without the use of expensive external bias tees. Figure 3 shows the standard board layout with component selection for optimized performance up to 6 GHz.

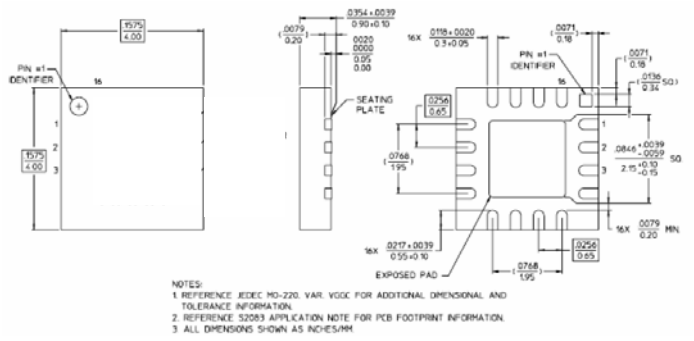

Figure 1. Package Outline Drawing

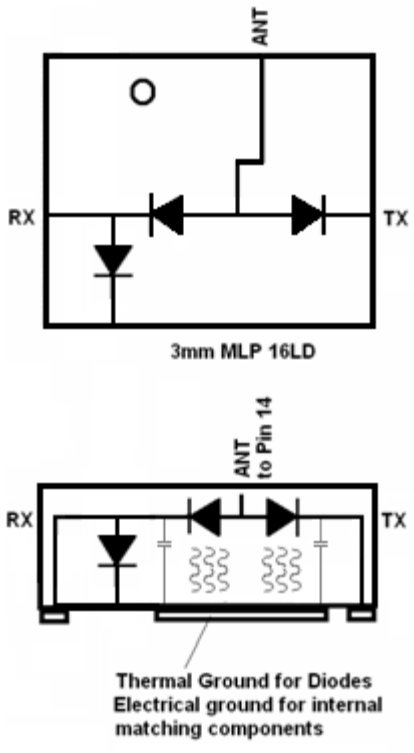

Figure 2. Electrical/Thermal Schematic

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
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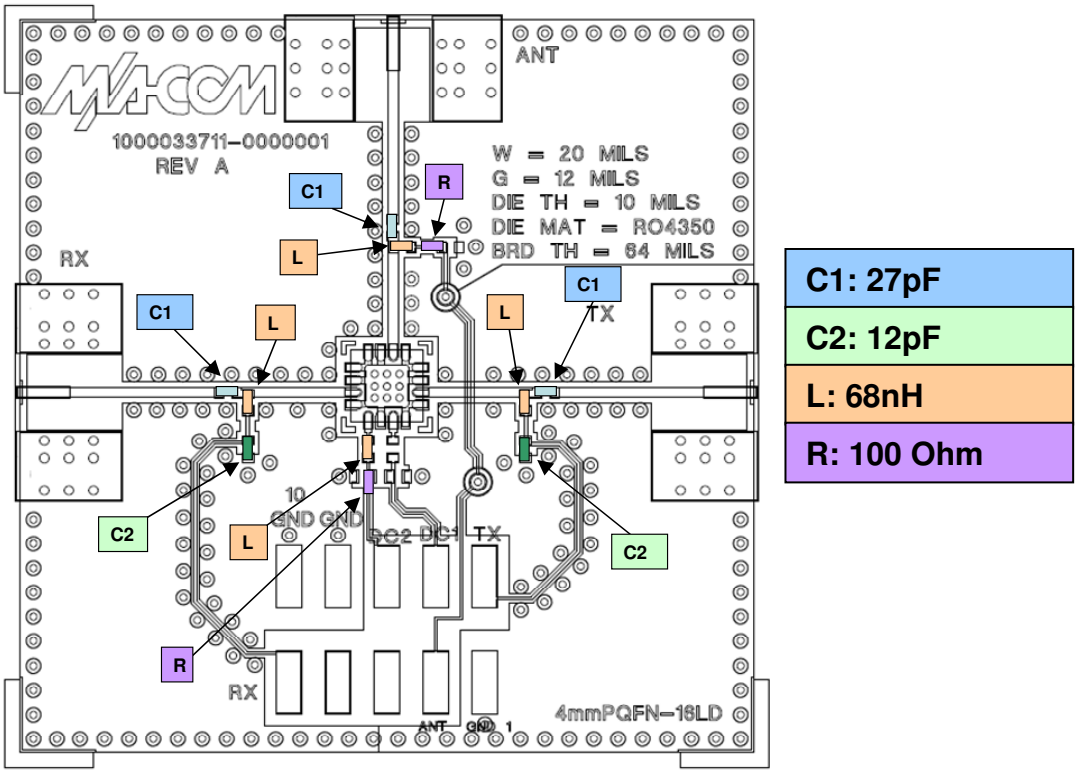

Figure 3. Sample Board Assembly Drawing

The diagram in Figure 4 is a schematic depiction of the Figure 3 sample board drawing. There are 100 Ohm resistors on the ANT path and the DC2 path. This topology allows for either an all-positive bias scheme or a positive and negative bias scheme.

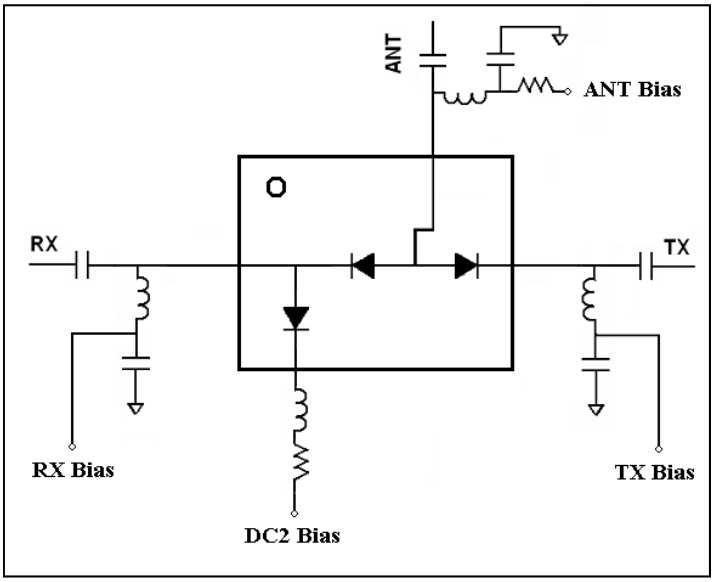

Figure 4. Sample Board Schematic

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Positive Voltage Supply

To accommodate biasing with a single positive supply, DC voltage must be applied to the Antenna, RX, TX, and DC2 ports. The resistor on the Antenna path will limit the current drawn when this voltage is applied. The resistor present on the DC2 bias path limits the current when the RX shunt diode is turned on. To achieve optimum performance, 50mA of DC bias current to the diodes is necessary. M/A-COM Tech supplies 100 Ohm resistors on these sample boards.

In order to achieve proper isolation in the "OFF" arm, the back bias (Vr) on the diodes should be large enough to sustain higher power levels. The voltage levels can range from +5V to +25V, as shown in the Figure. Minimum back bias requirements will change depending on incident peak RF Voltage and frequency of operation. Please contact M/A-COM Technology Solutions for additional guidance on required reverse bias voltages for specific application environments.

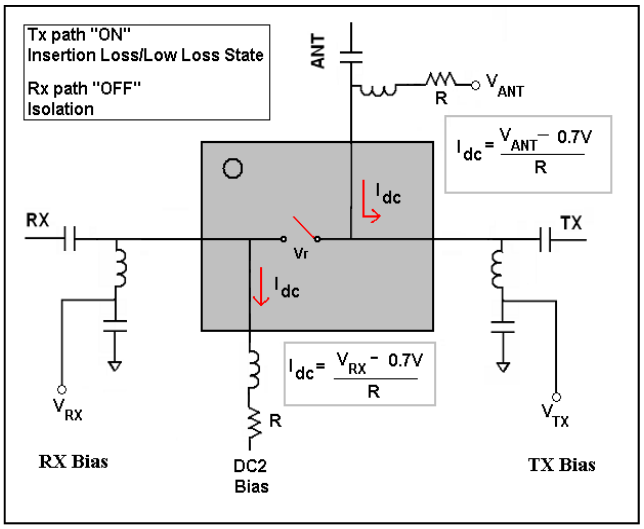

Figure 5. Transmit On, Receive Off

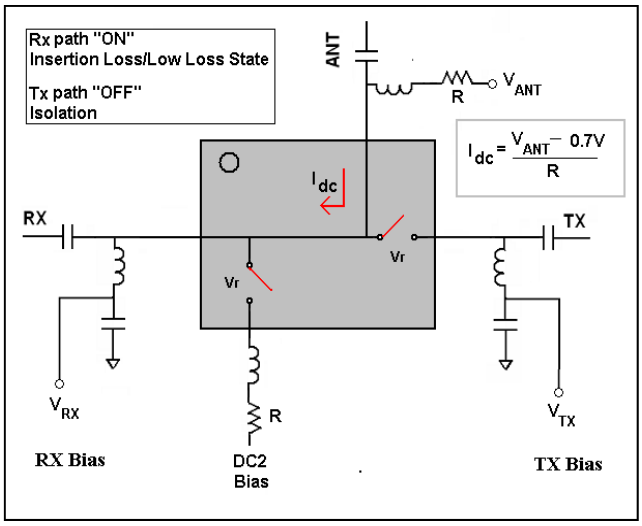

Figure 6. Transmit Off, Receive On

DC BIAS	Example Positive Bias Scheme	Tx - Antenna RF Condition	Rx - Antenna RF Condition
I_{DC} = +20 or +50 mA [ANT to TX Path ON] **V_{ANT}** = Voltage in which ANT resistor limits current to I_{DC} **V_{TX}** = 0V **V_{RX}** = Voltage in which DC2 resistor limits current to I_{DC} Must be greater than V_{ANT} [RX Path OFF / DC2 Path On] **DC2** = 0	I_{DC} = +50mA V_{ANT} = +5V V_{TX} = 0V V_{RX} = +25V DC2 = 0V	Insertion Loss	Isolation
I_{DC} = +20 or +50 mA [ANT to RX Path ON] **V_{ANT}** = Voltages in which resistors limit current to I_{DC} **V_{RX}** = 0V **V_{TX}** = Must be greater than V_{ANT} [TX Path OFF] **DC2** = Equal or higher than V_{RX} [DC2 Path OFF]	I_{DC} = +50mA V_{ANT} = +5V V_{TX} = +25V V_{RX} = +0V DC2 = +5V	Isolation	Insertion Loss

Figure 7. Single Positive Supply Biasing

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Dual Positive and Negative Voltage

The sample board can accommodate dual polarity supplies as shown in Figures 8 through 10. In this scheme, bias is applied to the Rx , Tx, and DC2 path. Unlike the single positive polarity bias scheme, bias to the ANT port is not used. A series resistor on the ANT arm and second resistor on the DC2 path will limit the current when a negative voltage is applied to the TX or RX Port. M/A-COM Tech supplies 100 Ohm resistors on these sample boards.

In order to achieve proper isolation in the "OFF" arm, the back bias (Vr) on the diodes should be large enough to sustain higher power levels. The voltage levels can range from +5V to +25V, as shown in the Figure. Minimum back bias requirements will change depending on incident peak RF Voltage and frequency of operation. Please contact M/A-COM Technology Solutions for additional guidance on required reverse bias voltages for specific application environments.

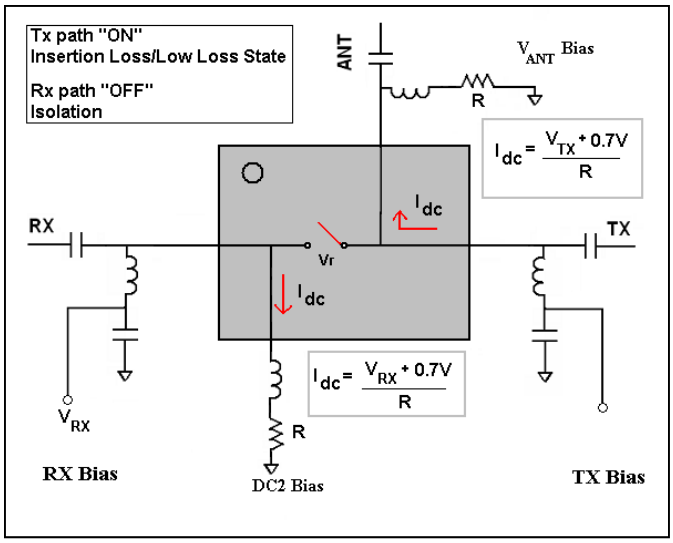

Figure 8. Transmit On, Receive Off

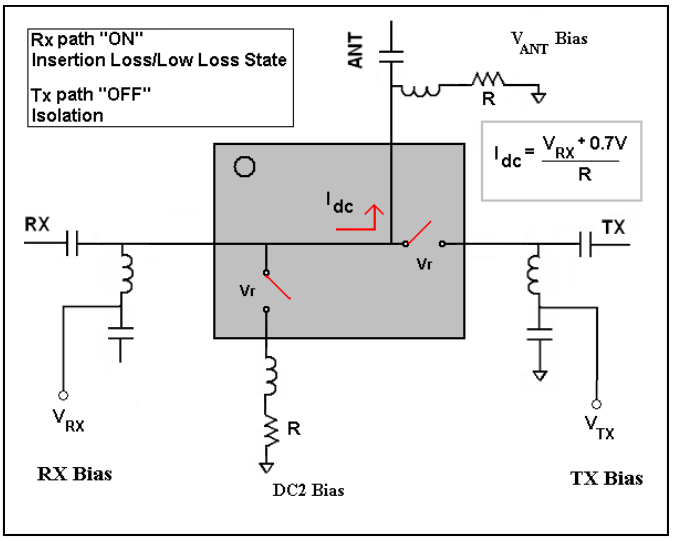

Figure 9. Transmit Off, Receive On

DC BIAS	Example Dual Bias Scheme	Tx - Antenna RF Condition	Rx - Antenna RF Condition
V_{TX} = Negative voltage in which ANT resistor limits current to I_{DC} [ANT to TX Path ON] V_{RX} = Positive voltage level, greater than 0V in which DC2 resistor limits current to I_{DC} [RX Path OFF / DC2 Path On]	V_{ANT} = 0V V_{TX} = -5V V_{RX} = +25V DC2 = 0V I_{DC} = +/- 50mA	Low Loss	Isolation
V_{RX} = Negative Voltage in which ANT resistor limits current to I_{DC} [ANT to RX Path ON] V_{TX} = Positive voltage level, greater than 0V in which DC2 resistor limits current to I_{DC} [RX Path OFF / DC2 Path On]	V_{ANT} = 0V V_{RX} = -5V V_{TX} = +25V DC2 = 0V I_{DC} = +/- 50mA	Isolation	Low Loss

Figure 10. Dual Positive and Negative Voltage Source Bias Truth Table