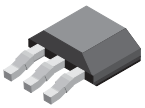
Highly Programmable Hall-Effect Switch

FEATURES AND BENEFITS

- Chopper stabilization for stable switchpoints throughout operating temperature range
- Externally programmable:
  - Operate point (through the VCC pin)
  - Output polarity
  - Output fall time for reduced EMI in automotive applications
- On-board voltage regulator for 3 to 24 V operation
- On-chip protection against:
  - Supply transients
  - Output short-circuits
  - Reverse battery condition

PACKAGES:

3-pin SIP
(suffix UA)



3-pin SIP
(suffix UA,
TS leadform)

3-pin SOT89
(suffix LT)

Not to scale

DESCRIPTION

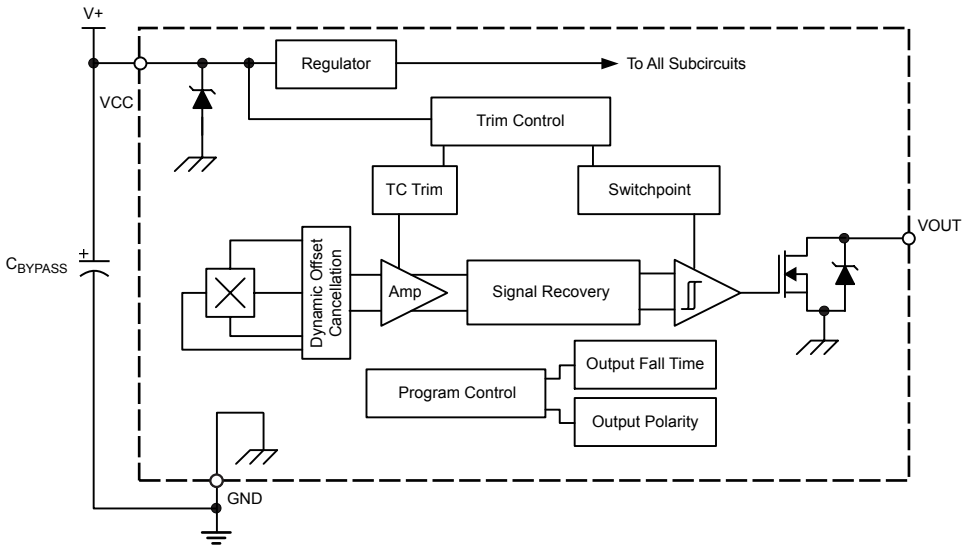
The A1128 is a field-programmable, unipolar Hall-effect switch designed for use in high-temperature applications. This device uses a chopper-stabilization technique to eliminate offset inherent in single-element devices.

The devices are externally programmable. A wide range of programmability is available on the magnetic operate point, B_{OP}, while the hysteresis remains fixed. This advanced feature allows optimization of the sensor IC switchpoint and can drastically reduce the effects of mechanical placement tolerances found in end-use production environments.

A proprietary dynamic offset cancellation technique, with an internal high-frequency clock, reduces the residual offset voltage, which is normally caused by device overmolding, temperature dependencies, and thermal stress. Having the Hall element and amplifier in a single chip minimizes many problems normally associated with low-level analog signals.

Two package styles provide a magnetically optimized package for most applications. Type LT is a miniature SOT89/TO-243AA surface mount package that is thermally enhanced with an exposed ground tab, and type UA is a three-lead ultramini SIP for through-hole mounting. The packages are lead (Pb) free, with 100% matte-tin-plated leadframes.

Functional Block Diagram



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Forward Output Voltage	V_{OUT}		26.5	V
Reverse Output Voltage	V_{ROUT}		–0.7	V
Output Sink Current	$I_{OUT(SINK)}$	VCC to VOUT	20	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

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OPERATING CHARACTERISTICS (continued): Valid with T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, V_{CC} = 12 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]

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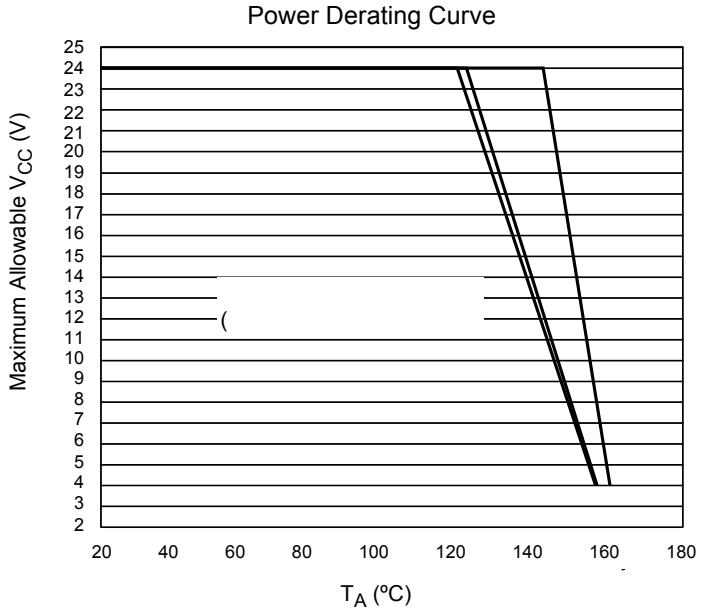
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Application Information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W
		Package LT, 1-layer PCB with copper limited to solder pads	180	°C/W
		Package LT, 2-layer PCB with 0.94 in^2 copper each side	78	°C/W

*Additional thermal information available on Allegro website.



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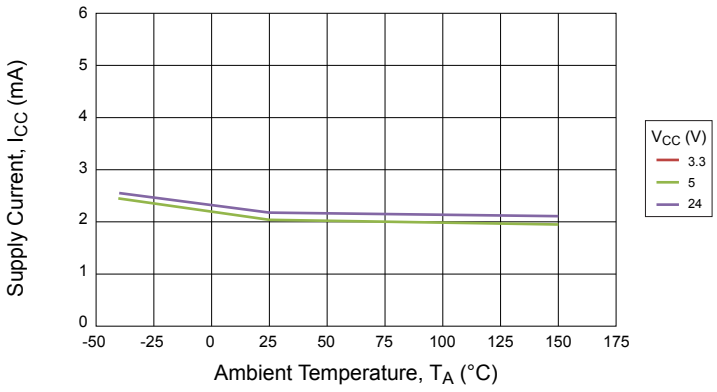
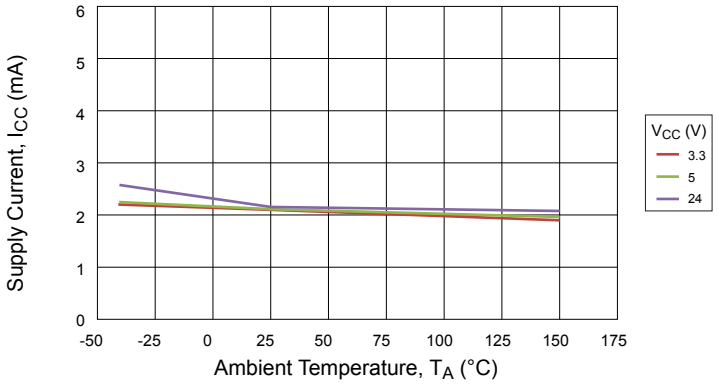
CHARACTERISTIC PERFORMANCE

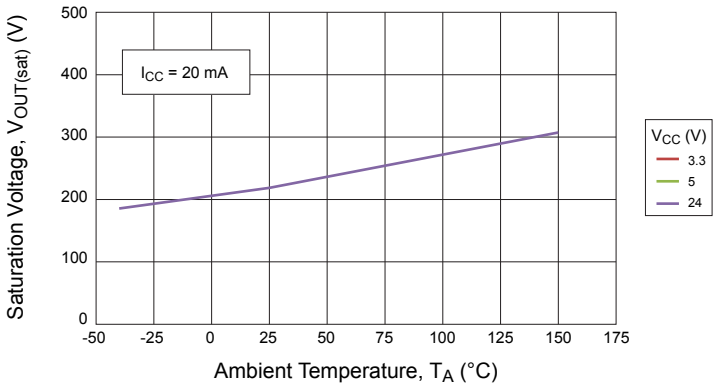
Supply Current (On) versus Ambient Temperature



Supply Current (Off) versus Ambient Temperature



Saturation Voltage versus Ambient Temperature



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APPLICATION INFORMATION

Figure 1. Typical Application Circuit

CHOPPER STABILIZATION TECHNIQUE

When using Hall-effect technology, a limiting factor for switch point accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal and stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high frequency sampling clock. For demodulation process, a sample and hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

Figure 2. Concept of Chopper Stabilization Technique

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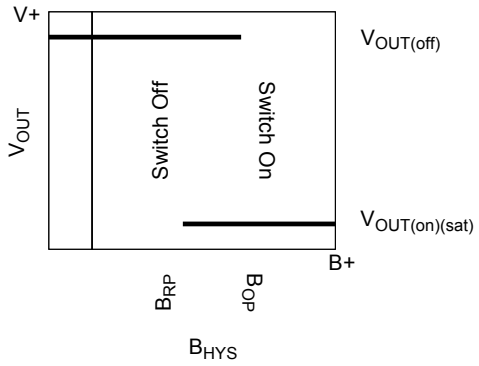
FUNCTIONAL DESCRIPTION

When the Output Polarity bit is not set (POL = 0), the A1128 output switches on after the magnetic field at the Hall sensor IC exceeds the operate point threshold, B_{OP}. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output switches off. The difference between the magnetic operate and release points is called the hysteresis of the device, B_{HYS}.
In the alternative case, in which the Output Polarity bit is set (POL = 1), the A1128 output switches off when the magnetic field at the Hall sensor IC exceeds the operate point threshold, B_{OP}. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output switches on.

Note that for the Pre-Programming B_{OP} Target, B_{OPinit}, when BOPPOL = 0 although the operating range is 0 to B+, the initial B_{OPinit} is actually negative, and likewise, when BOPPOL = 1, although the operating range 0 to B– , the initial B_{OPinit} is actually positive.



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OVERVIEW

Programming is accomplished by sending a series of input voltage pulses serially through the VCC (supply) pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a desired programmable parameter and change its value. There are three voltage levels that must be taken into account when programming. These levels are referred to as *high* (V_{PH}), *mid* (V_{PM}), and *low* (V_{PL}).

The A1128 features three programmable modes, Try mode, Blow mode, and Read mode:

- In Try mode, programmable parameter values are set and measured simultaneously. A parameter value is stored temporarily, and reset after cycling the supply voltage.
- In Blow mode, the value of a programmable parameter may be permanently set by blowing solid-state fuses internal to the device. Device locking is also accomplished in this mode.
- In Read mode, each bit may be verified as blown or not blown.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line. Note that, for all programming modes, no parameter programming registers are accessible after the device-level LOCK bit is set. The only function that remains accessible is the overall Fuse Checking feature.

Although any programmable variable power supply can be used to generate the pulse waveforms, for design evaluations, Allegro highly recommends using the Allegro Sensor IC Evaluation Kit, available on the Allegro website On-line Store. The manual for that kit is available for download free of charge, and provides additional information on programming these devices. (Note: This kit is not recommended for production purposes.)

DEFINITION OF TERMS

Register The section of the programming logic that controls the choice of programmable modes and parameters.

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Key A series of voltage pulses used to select a register or mode.

Code The number used to identify the combination of fuses activated in a bit field, expressed as the decimal equivalent of the binary value. The LSB of a bit field is denoted as code 1, or bit 0.

Addressing Increasing the bit field code of a selected register by serially applying a pulse train through the VCC pin of the device. Each parameter can be measured during the addressing process, but the internal fuses must be blown before the programming code (and parameter value) becomes permanent.

Fuse Blowing Applying a high voltage pulse of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. Once a bit (fuse) has been blown, it cannot be reset.

Blow Pulse A high voltage pulse of sufficient duration to blow the addressed fuse.

Cycling the Supply Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

Programming Procedure

Programming involves selection of a register and mode, and then setting values for parameters in the register for evaluation or fuse blowing. Figure 8 provides an overview state diagram.

REGISTER SELECTION

Each programmable parameter can be accessed through a specific register. To select a register, from the Initial state, a sequence of voltage pulses consisting of one V_{PH} pulse, one V_{PM} pulse, and then a unique combination of V_{PH} and V_{PM} pulses, is applied serially to the VCC pin (with no V_{CC} supply interruptions). This sequence of pulses is called the *key*, and uniquely identifies each register. An example register selection key is shown in figure 5.

To simplify Try mode, the A1128 provides a set of four virtual registers, one for each combination of: B_{OP} selection (BOPSEL), B_{OP} polarity (BOPPOL), and a facility for transiting B_{OP} magni-

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The four B_{OP} selecting virtual registers allow the programmer to adjust the B_{OP} parameter for use in north or south magnetic fields. In addition, values can be traversed from low to high, or from high to low. Figure 12 shows the relationship between the B_{OP} parameter and the different Try mode registers. Note: See the Output Polarity section for information about setting the POL bit before using Try mode.

The FALL and POL fields are in the same register (FALL is bits 1:0, and POL is bit 2). Therefore, in Try mode both can be programmed simultaneously by adding the codes for the two parameters, and send the sum as the code. For example, sending code 7 (111) sets FALL to 3 (x11) and sets POL (1xx).

BLOW MODE

After the required code is determined for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by selecting the register and mode selection key, followed by the appropriate bit field address, and ending the sequence with a Blow pulse. The Blow mode selection key is a sequence of eleven V_{PM} pulses followed by one V_{PH} pulse. The Blow pulse consists of a V_{PH} pulse of sufficient duration, t_{BLOW}, to permanently set an addressed bit by blowing a fuse internal to the device. The device power must be cycled after each individual fuse is blown.

Due to power requirements, a 0.1 µF blowing capacitor, C_{BLOW}, must be mounted between the VCC pin and the GND pin during programming, to ensure enough current is available to blow fuses. If programming in the application, C_{BYPASS} (see figure 1) can serve the same purpose.

The fuse for each bit in the bit field must be blown individually. The A1128 built-in circuitry allows only one fuse at a time to be blown. During Blow mode, the bit field can be considered a “one-

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Table 3. Programming Logic Table

Register Name [Selection Key]	Bit Field Address (Code)		Notes
	Binary (MSB→LSB)	Decimal Equivalent	
TRY MODE REGISTER SELECTIONS			
B_{OP}			

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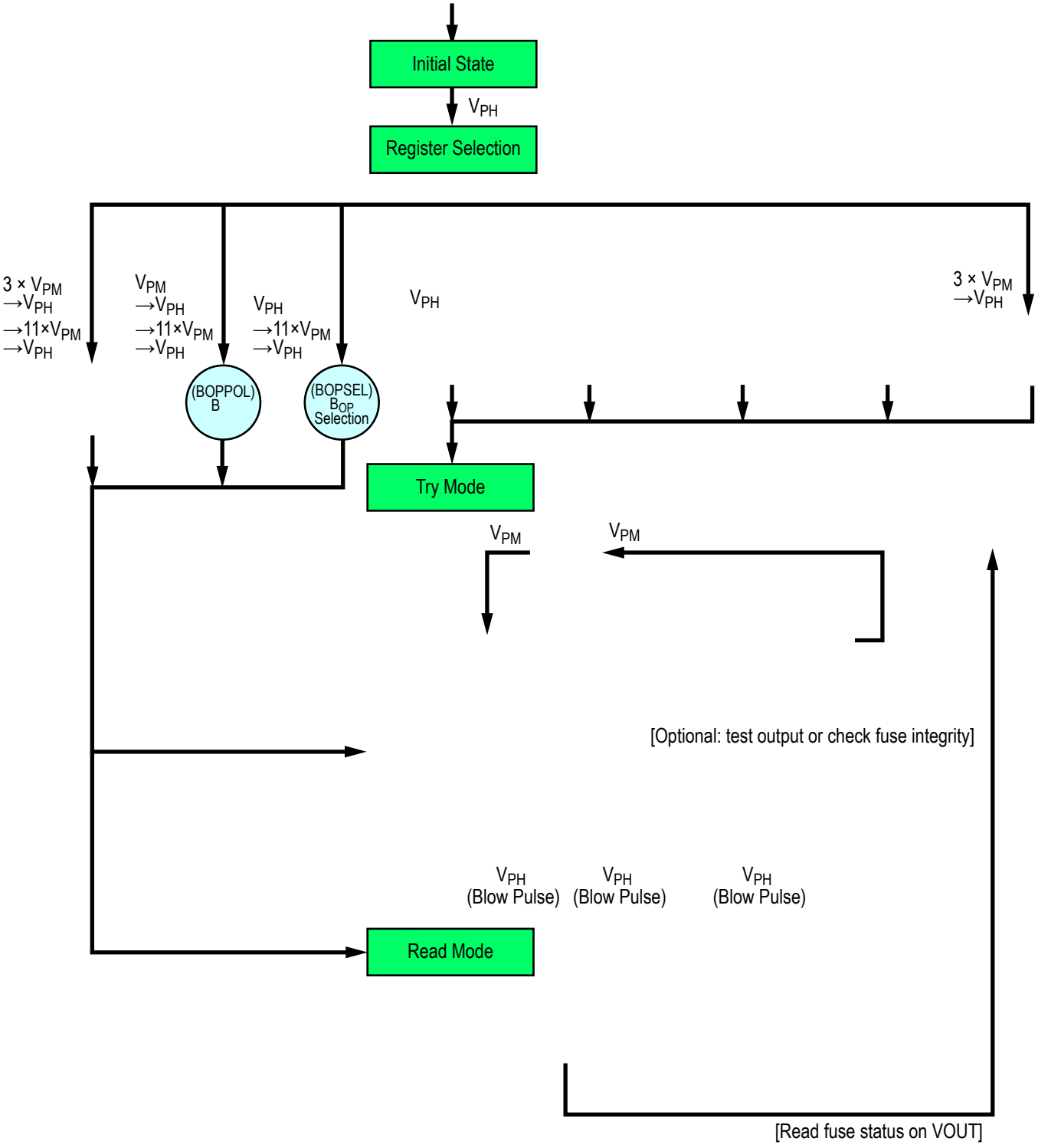

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FUSE CHECKING

Incorporated in the A1128 is circuitry to simultaneously check the integrity of the fuse bits. The fuse checking feature is enabled by using the Fuse Checking registers, and while in Try mode, applying the codes shown in table 3. The register is only valid in Try mode and is available before or after the programming LOCK bit is set.

Selecting the Fuse Threshold High register checks that all blown fuses are properly blown. Selecting the Fuse Threshold Low register checks all un-blown fuses are properly intact. The supply current, I_{CC}, increases by 250 µA if a marginal fuse is detected. If all fuses are correctly blown or fully intact, there will be no change in supply current.

OUTPUT POLARITY

When selecting the B_{OP} registers in Try mode, the output polarity is determined by the value of the Output Polarity bit (POL). The default value is POL = 0 (fuse un-blown). For applications that require the output states defined by POL = 1 (see Operating Characteristics table), it is recommended to first permanently blow the POL bit by selecting the Output / Lock bit register, and code 4. The output is then defined by POL = 1 when selecting the B_{OP} Try mode registers. See table 3 for parameter details.

ADDITIONAL GUIDELINES

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

- The power supply used for programming must be capable of delivering at least V_{PH} and 175 mA.
- Be careful to observe the t_{LOW} delay time before powering down the device after blowing each bit.
- Set the LOCK bit (only after all other parameters have been programmed and validated) to prevent any further programming of the device.

READ MODE

The

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to the MSB. Read mode is available only before the LOCK bit has been set.

After the final V_{PH} key pulse, and after each V_{PM} address pulse, if V_{OUT} is low, the corresponding fuse can be considered blown (the status of the Output Polarity bit, POL, does not affect Read mode output values, allowing POL to be tested also). If the output state is high, the fuse can be considered un-blown. During Read mode VOUT must be pulled high using a pull-up resistor (see R_{LOAD} in the Typical Application Circuit diagram).

Figure 10. Example of Try mode programming pulses applied to the VCC pin. In this example, B_{OP} Positive Trim, Down-Counting register is addressed to code 12 by the eleven V_{PM} pulses (code 1 is selected automatically at the falling edge of the register-mode selection key).

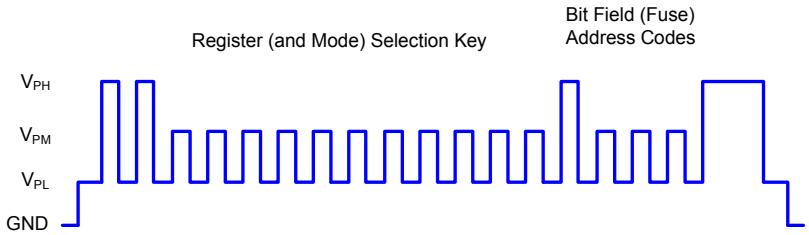

Figure 11. Example of Blow mode programming pulses applied to the VCC pin. In this example, the B_{OP} Magnitude Selection register (BOPSEL) is addressed to code 8 (bit 3, or 3 V_{PM} pulses) and its value is permanently blown.

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B_{OP} SELECTION

The A1128 allows accurate trimming of the magnetic operate point, B_{OP}, within the application. This programmable feature reduces effects due to mechanical placement tolerances and improves performance when used in proximity or vane sensing applications.

B_{OP} can be set to any value within the range allowed by the BOPSEL registers. This includes switchpoints of south or north polarity, and switchpoints at or near the zero crossing point for B. However, switching is recommended only within the Programmable B_{OP} Range, specified in the Operating Characteristics table.

Trimming of B_{OP} is typically done in two stages. In the first stage, B_{OP} is adjusted temporarily using the Try mode programming features, to find the fuse value that corresponds to the optimum B_{OP}. After a value is determined, then it can be permanently set using the Blow mode features.

As an aid to programming the A1128 has several options available in Try Mode for adjusting the B_{OP} parameter. As shown in figure 12, these allow trimming of B_{OP} for operation in north or south polarity magnetic fields. In addition the B_{OP} parameter can either trim-up, start at the B_{OP} minimum value and increase to the maximum value, or trim-down, starting at the B_{OP} maximum value and decreasing to the minimum value.

(A) B_{OP} Positive, Trim Up-Counting Register

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The device must be operated below the maximum junction temperature of the device, T_J(max) . Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \qquad (1)$$

$$\Delta T = P_D \times R$$

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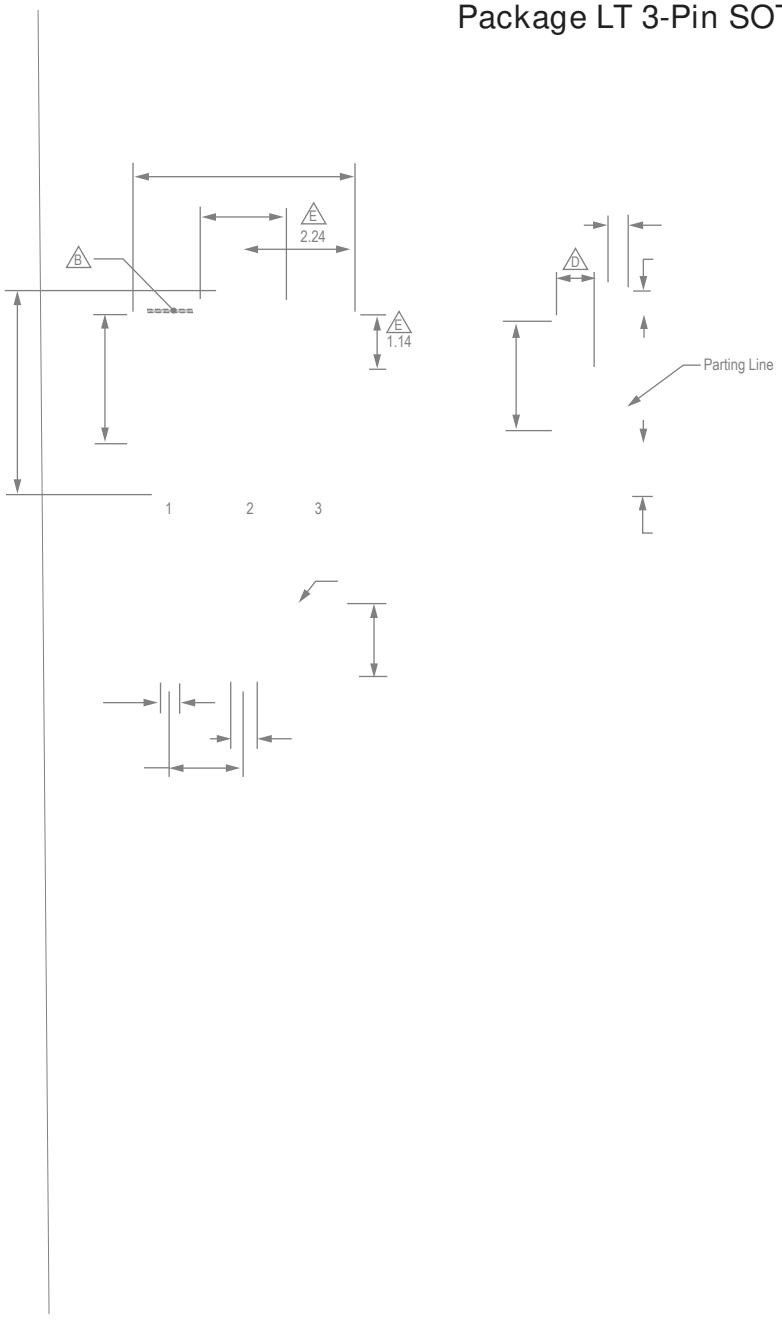
PACKAGE OUTLINE DRAWINGS

Package LT 3-Pin SOT-89



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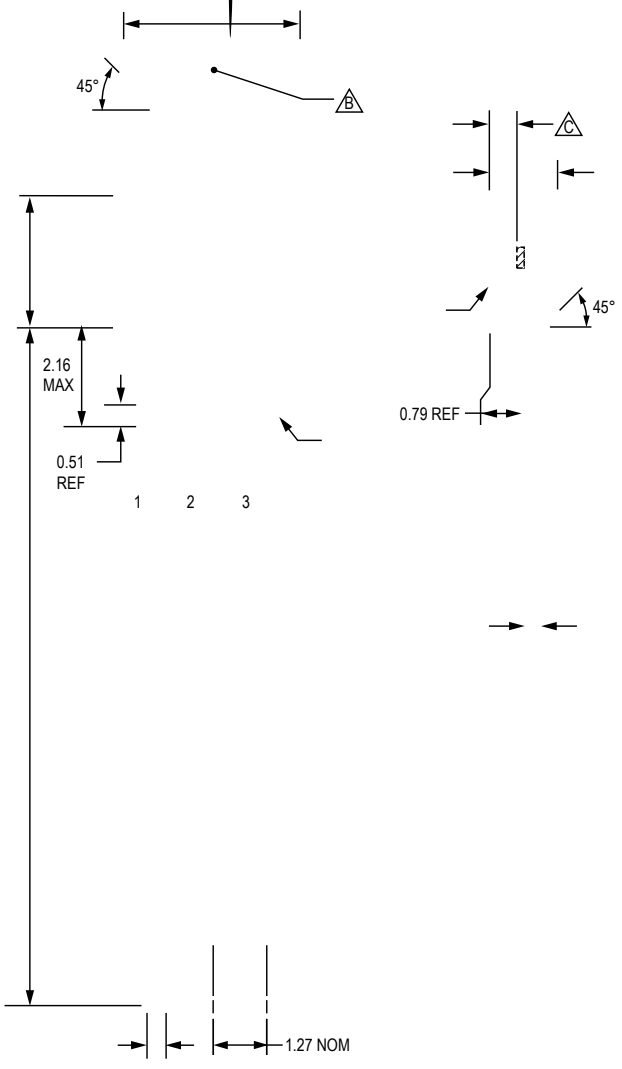
Package UA 3-Pin SIP



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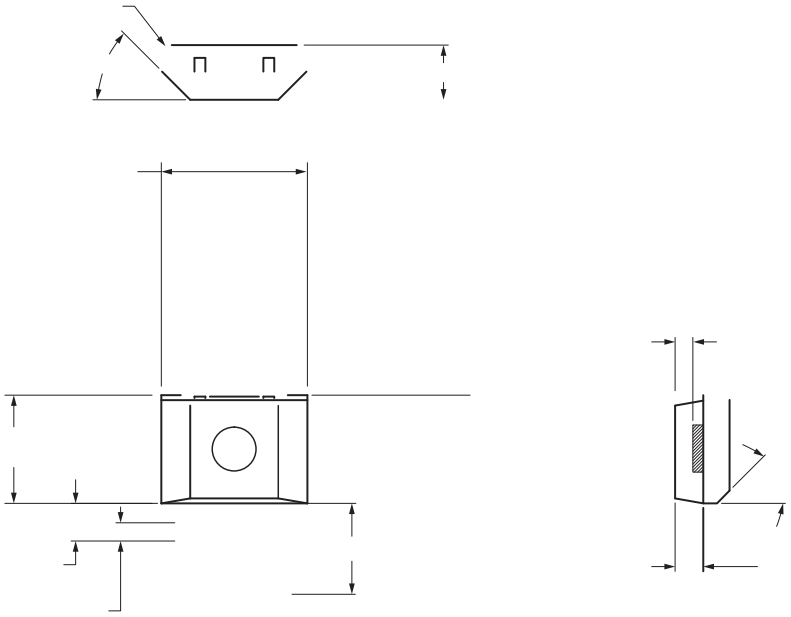
Package UA 3-Pin SIP, TS Leadform



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Revision History

Number	Date	Description
3	September 6, 2018	Minor editorial updates
4	December 7, 2018	Updated -LT package option status to Last-Time Buy; added UA package TS leadform option
5	December 12, 2019	Minor editorial updates
6	January 18, 2023	Updated UA package drawings (pages 19-20)

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