

HSD88

Silicon Schottky Barrier Diode for Detector, Mixer

REJ03G0602-0100
 (Previous: ADE-208-1386)
 Rev.1.00
 Apr 26, 2005

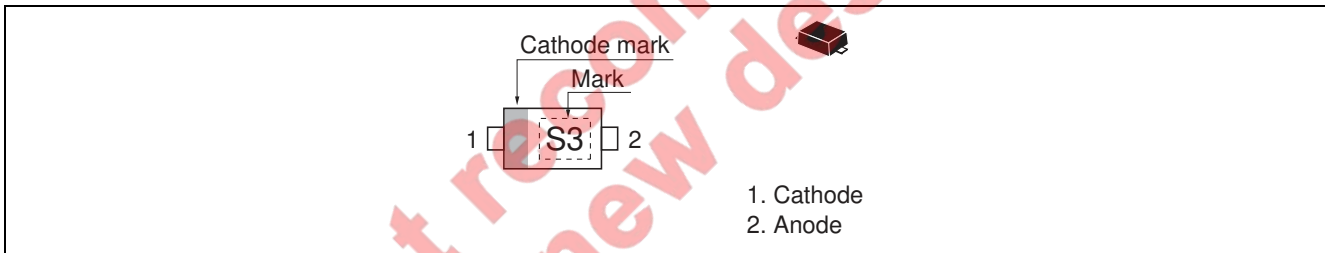
Features

- Low capacitance. (C = 0.8 pF max)
- Low forward voltage.
- Super small Flat Lead Package (SFP) is suitable for surface mount design.

Ordering Information

Type No.	Cathode Mark	Package Name	Package Code (Previous Code)
HSD88	S3	SFP	PUSF0002ZB-A (SFP)

Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Reverse voltage	V_R	10	V
Average rectified current	I_O	15	mA
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-55 to +125	°C

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Forward voltage	V_{F1}	0.350	—	0.420	V	$I_F = 1 \text{ mA}$
	V_{F2}	0.500	—	0.580		$I_F = 10 \text{ mA}$
Reverse current	I_{R1}	—	—	0.2	μA	$V_R = 2 \text{ V}$
	I_{R2}	—	—	10		$V_R = 10 \text{ V}$
Capacitance	C	—	—	0.80	pF	$V_R = 0 \text{ V}$, $f = 1 \text{ MHz}$
ESD-Capability *1	—	30	—	—	Ω	C = 200 pF, Both forward and reverse direction 1 pulse.

Notes: 1. Failure criterion ; $I_R > 0.4 \mu\text{A}$ at $V_R = 2 \text{ V}$

2. Please do not use the soldering iron due to avoid high stress to the SFP package.

Not recommended
for new design

Main Characteristic

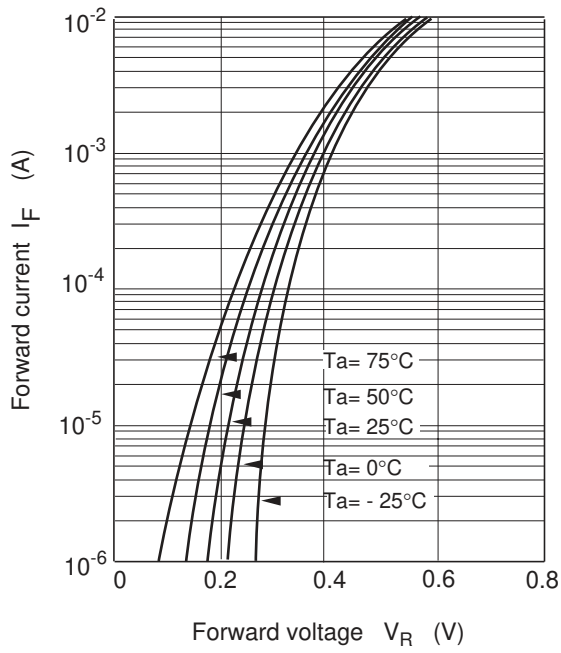


Fig.1 Forward current vs. Forward voltage

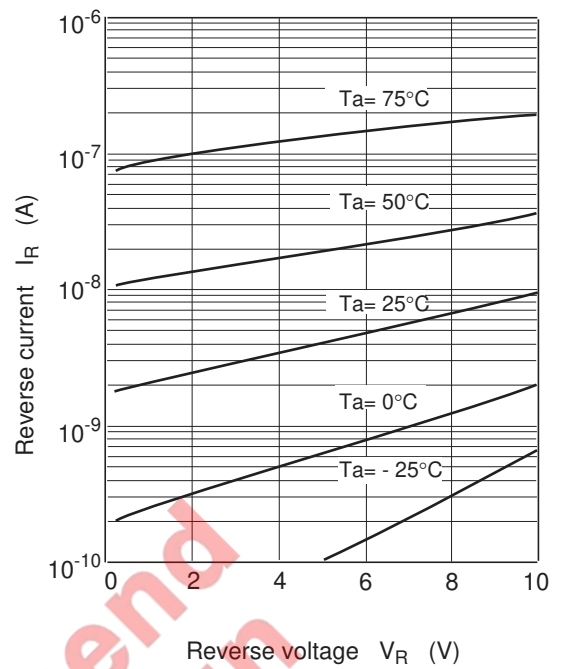


Fig.2 Reverse current vs. Reverse voltage

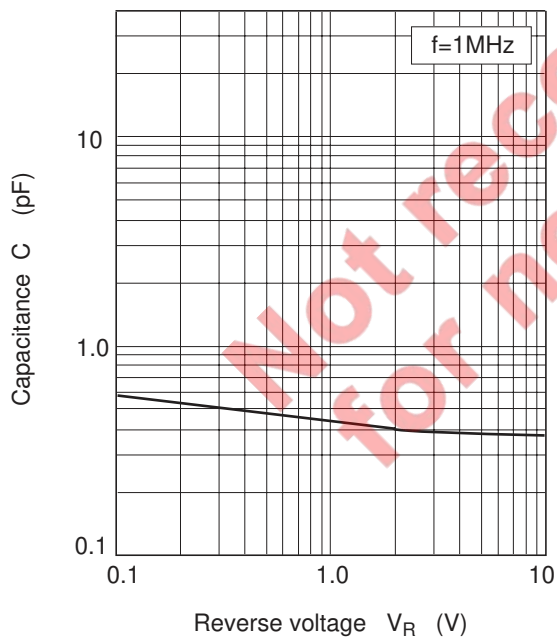
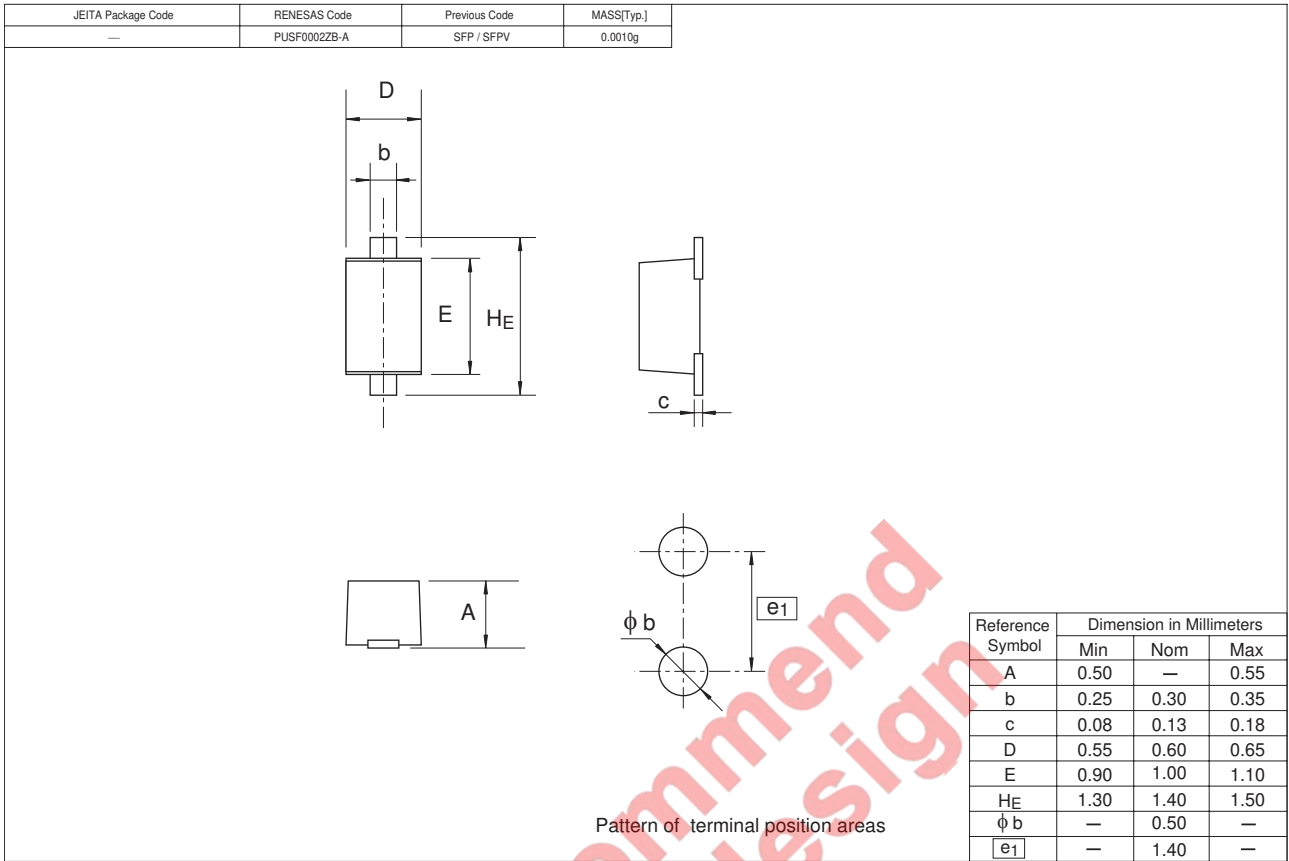


Fig.3 Capacitance vs. Reverse voltage

Package Dimensions



Not recommended for new design

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Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
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1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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April 1st, 2010
Renesas Electronics Corporation

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