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## CONTINUITY OF SPECIFICATIONS

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## CONTINUITY OF ORDERING PART NUMBERS

Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

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**S71VS/XS-R**

# MirrorBit® 1.8 V Simultaneous Read/Write Burst Mode Multiplexed Flash and Burst

## Features

- Power supply voltage of 1.7V to 1.95V
- Flash / pSRAM Burst Speed: 108 MHz, 104 MHz, 83 MHz
- MCP BGA Packages
  - 52 ball, 6.0 x 5.0 mm, 0.5 mm ball pitch
  - 56 ball, 7.7 x 6.2 mm, 0.5 mm ball pitch
  - 56 ball, 9.2 x 8.0 mm, 0.5 mm ball pitch
- Operating Temperature
  - Wireless, –25 °C to +85 °C
  - Industrial, –40 °C to +85 °C

## General Description

The S71VS-R Series is a product line of stacked Multi-Chip Package (MCP) memory solutions and consists of the following items:

- One or more S29VS-R Flash memory die
- One or more pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to their individual data sheet for further details.

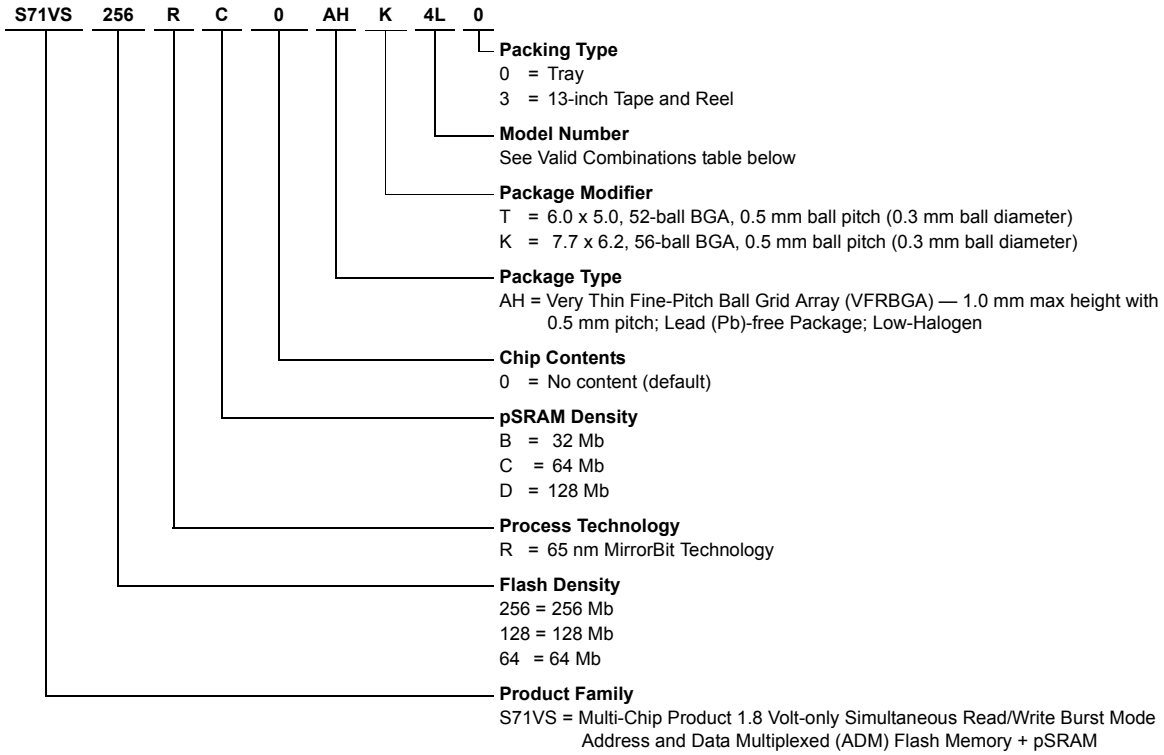
| Flash Density | pSRAM Density | Product |
|---|---|---|
| 64 Mb | 32 Mb | S71VS064RB0 |
| 128 Mb | 32 Mb | S71VS128RB0 |
| 128 Mb | 64 Mb | S71VS128RC0 |
| 256 Mb | 64 Mb | S71VS256RC0 |
| 256 Mb | 128 Mb | S71VS256RD0 |

For detailed specifications, please refer to the individual data sheets:

| Document | Cypress Document Number |
|---|---|
| S29VS256R, S29VS128R datasheet | 002-00833 |
| S29VS064R datasheet | 002-00949 |
| 32 Mb CellularRAM Address/Data multiplexed | SWM032D108M1R |
| 32 Mb CellularRAM Address/Data multiplexed | SWM032D108M3R |
| 64 Mb CellularRAM Address/Data multiplexed | SWM064D108M1R |
| 128 Mb CellularRAM Address/Data multiplexed | SWM128D108M1R |
| 128 Mb CellularRAM Address/Data multiplexed | SWM128D108M3R |

# 1. Ordering Information

The order number is formed by a valid combinations of the following:



## 1.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

| Base Ordering Part Number | Package | Model Number | Packing Type | pSRAM Type | Flash Boot | Temperature Range | Flash / pSRAM Speed | Pinout and Package Notes |
|---|---|---|---|---|---|---|---|---|
| S71VS064RB0 | AHT | 3L | 0, 3 | SWM032D108M1R | Top | Wireless | 108 MHz | Pinout: S71VS-R 52-ball Package: RLG052 |
| | | BL | | | Bottom | | | |
| | | 4L | | | Top | | | Pinout: S71VS-R 52-ball Package: RSE052 |
| | | CL | | | Bottom | | | |
| | | 0M | | SWM032D108M3R | Top | Industrial | | |
| | | 8M | | | Bottom | | | |
| | | 3M | | | Top | | | Pinout: S71VS-R 52-ball Package: RLG052 |
| | | BM | | | Bottom | | | |
| S71VS128RB0 | AHK | 3L | | SWM032D108M1R | Top | Wireless | 108 MHz | Pinout: S71VS-R 56-ball Package: RLA056 |
| | | BL | | | Bottom | | | |
| | | 4L | | | Top | | | Pinout: S71VS-R 56-ball Package: RSD056 |
| | | CL | | | Bottom | | | |
| S71VS128RC0 | AHK | 4L | | SWM064D108M1R | Top | | 108 MHz | Pinout: S71VS-R 56-ball Package: RSD056 |
| | | CL | | | Bottom | | | |
| S71VS256RC0 | AHK | 4L | | SWM064D108M1R | Top | | 108 MHz | Pinout: S71VS-R 56-ball Package: RLA056 |
| | | CL | | | Bottom | | | |
| S71VS256RD0 | AHK | 3L | | SWM128D108M1R | Top | | 108 MHz | Pinout: S71VS-R 56-ball Package: RSD056 |
| | | BL | | | Bottom | | | |
| | | 4L | | | Top | | | |
| | | CL | | | Bottom | | | |
| | | 3C | | | Top | | 83 MHz | |
| | | BC | | | Bottom | | | |
| | | 3M | | SWM128D108M3R | Top | Industrial | 108 MHz | |

***Note:***
*If a choice exists, Spansion recommends Top Boot.*

# 2. Input/Output Descriptions

Table 2.1 identifies the input and output package connections provided on the device.

**Table 2.1** Input/Output Descriptions (Sheet 1 of 2)

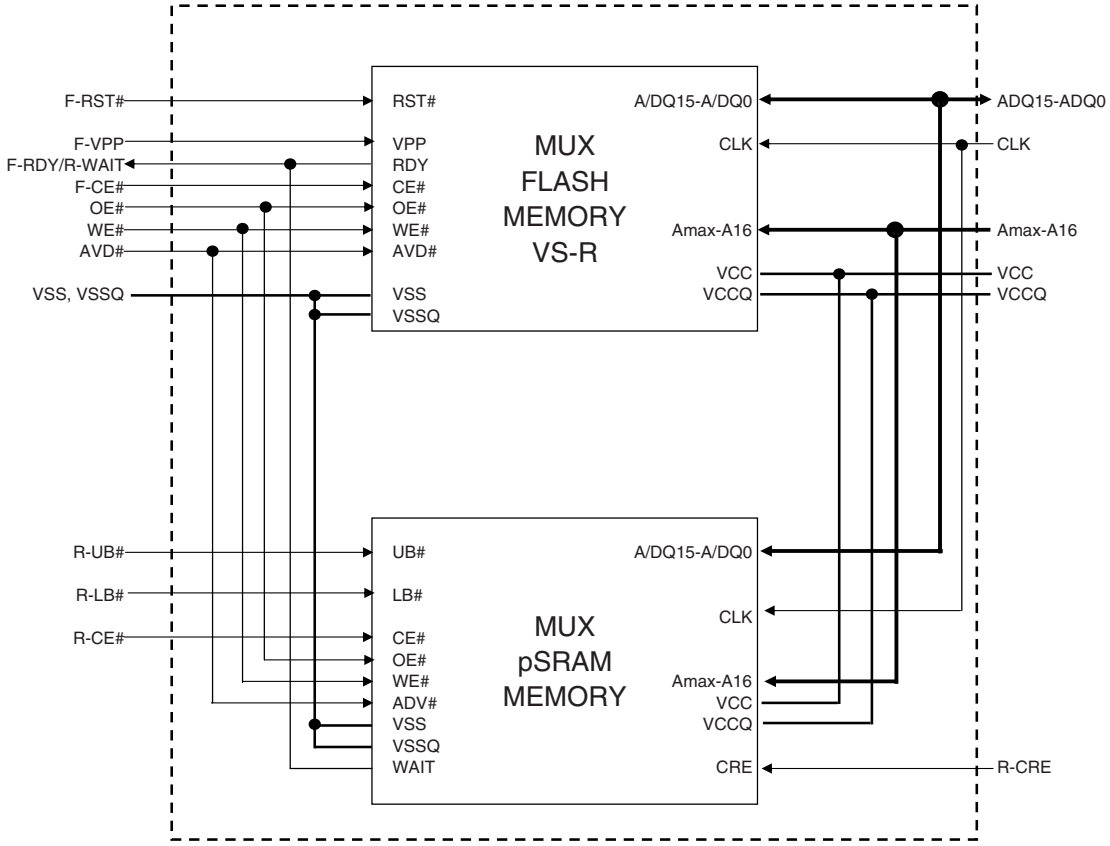
| Symbol | Description | Flash | RAM |
|---|---|---|---|
| AMAX–A16 | Address inputs. | X | X |
| A/DQ15–A/DQ0 | Multiplexed Address/Data. | X | X |
| AVD# | Address Valid input. Indicates to device that the valid address is present on the address inputs.<br>Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched.<br>High = device ignores address inputs | X | X |
| CLK | Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at $V_{IL}$ or $V_{IH}$ while in asynchronous mode. | X | X |
| DNU | Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Spansion for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at $V_{IL}$. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to $V_{SS}$. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections. | | |
| OE# | Output Enable input. Asynchronous relative to CLK for the Burst mode. | X | X |
| F-CE# | Chip-enable input for Flash. Asynchronous relative to CLK for Burst Mode. | X | |
| F-RDY/R-WAIT | Ready output; indicates the status of the Burst read.<br>Flash Memory RDY (using default “Active HIGH” configuration)<br>$V_{OL}$ = data invalid<br>$V_{OH}$ = data valid<br>Note: The default polarity for the pSRAM WAIT signal is opposite the default polarity of the Flash RDY signal.<br>pSRAM WAIT (using default “Active HIGH” configuration)<br>$V_{OL}$ = data valid<br>$V_{OH}$ = data invalid<br>To match polarities, change bit 10 of the pSRAM Bus Configuration Register to 0 (Active LOW WAIT). Alternately, change bit 10 of the Flash Configuration Register to 0 (Active LOW RDY). | X | X |
| F-RST# | Hardware reset input. Low = device resets and returns to reading array data | X | |
| F-$V_{PP}$ | Accelerated input. At $V_{HH}$, accelerates programming; automatically places device in unlock bypass mode. At $V_{IL}$, disables all program and erase functions. Should be at $V_{IH}$ for all other conditions. | X | |
| NC | Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). | | |
| R-CE# | Chip-enable input for pSRAM. | | X |
| R-CRE | Control Register Enable (pSRAM). | | X |
| R-LB# | Lower Byte Control (pSRAM). | | X |
| R-UB# | Upper Byte Control (pSRAM). | | X |

**Table 2.1** Input/Output Descriptions (Sheet 2 of 2)

| Symbol | Description | Flash | RAM |
|---|---|---|---|
| RFU | Reserved For Future Use. No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices. | | |
| $V_{CC}$ | Flash and pSRAM 1.8 Volt-only single power supply. | X | X |
| $V_{CCQ}$ | Flash and pSRAM Input/Output Power Supply. | X | X |
| $V_{SS}$ | Ground. | X | X |
| $V_{SSQ}$ | Input/Output Ground. | X | X |
| WE# | Write Enable input. | X | X |

# 3. MCP Block Diagram

**Figure 3.1** S71VS-R MCP Block Diagram



# 4. Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S71VS-R.

## 4.1 Special Handling Instructions for FBGA Packages

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150 °C for prolonged periods of time.

## 4.2 Connection Diagrams

**Figure 4.1** S71VS-R 56-ball Fine-Pitch Ball Grid Array

(Top View, Balls Facing Down)

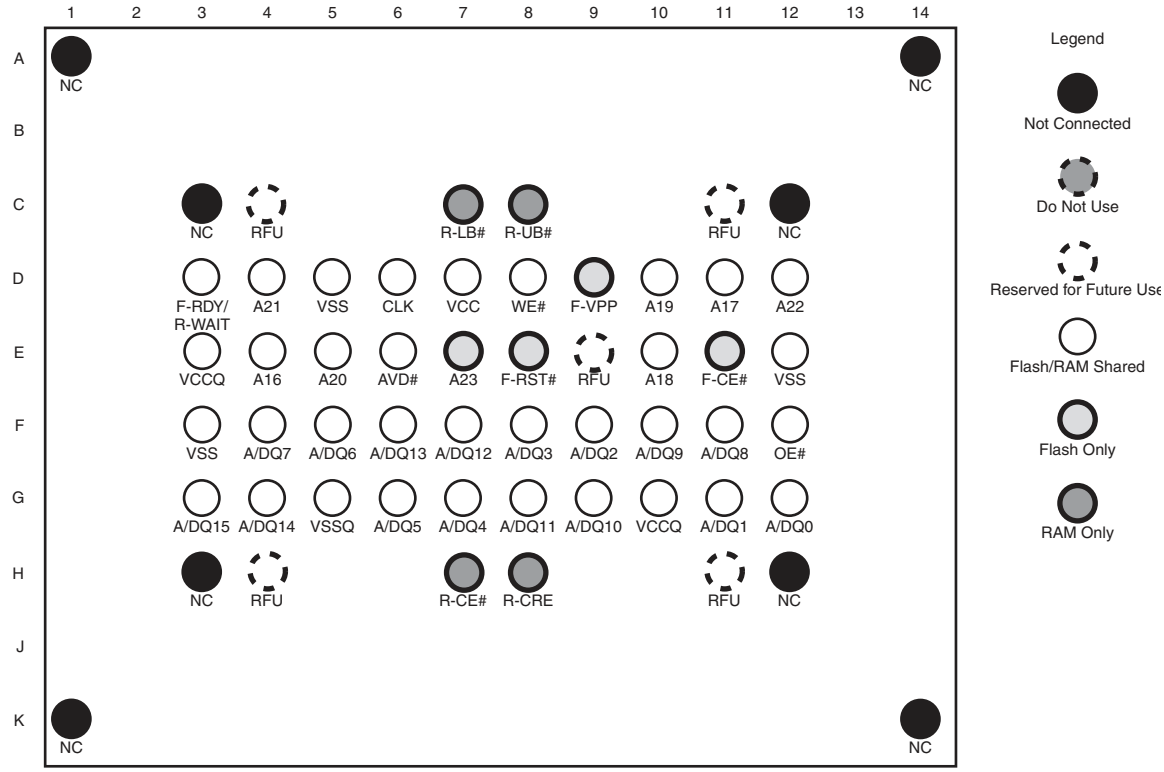
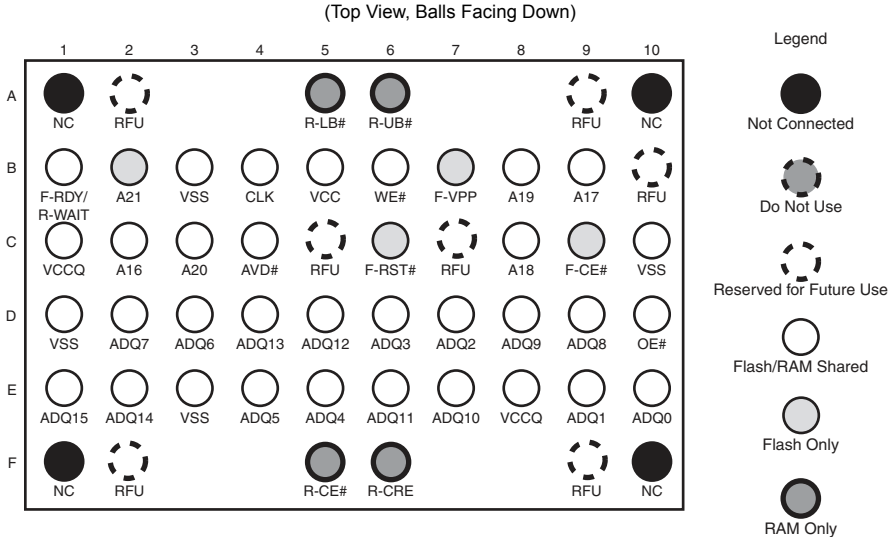


**Figure 4.2** S71VS-R 52-ball Fine-Pitch Ball Grid Array



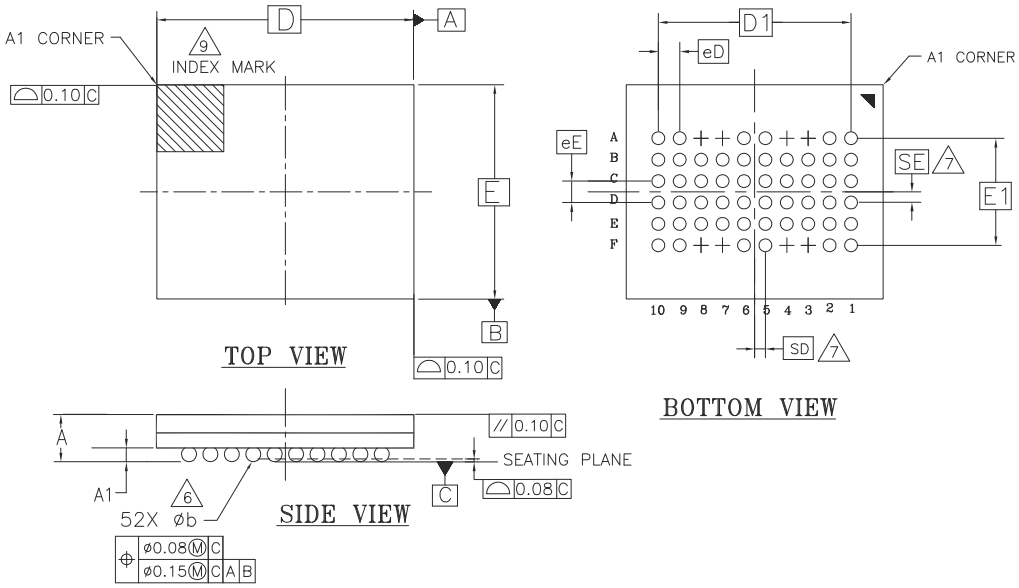

***Notes:***

1. *Addresses are shared between Flash and RAM depending on the density of the pSRAM.*
2. *$V_{SS}$ and $V_{SSQ}$ must be connected together.*

| MCP | Flash-Only Addresses | Shared Addresses | Shared ADQ Pins |
|---|---|---|---|
| S71VS064RB0 | A21 | A20–A16 | A/DQ15-A/DQ0 |
| S71VS128RB0 | A22–A21 | A20–A16 | |
| S71VS128RC0 | A22 | A21–A16 | |
| S71VS256RC0 | A23–A22 | A21–A16 | |
| S71VS256RD0 | A23 | A22–A16 | |

## 4.3 Physical Dimensions

**Figure 4.3** RLG052 - 52-ball VFRBGA 6.0 x 5.0 mm




| PACKAGE | RLG 052 | | | |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| | 6.00 mm x 5.00 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | --- | --- | 1.00 | PROFILE |
| A1 | 0.18 | --- | --- | BALL HEIGHT |
| D | 6.00 BSC. | | | BODY SIZE |
| E | 5.00 BSC. | | | BODY SIZE |
| D1 | 4.50 BSC. | | | MATRIX FOOTPRINT |
| E1 | 2.50 BSC. | | | MATRIX FOOTPRINT |
| MD | 10 | | | MATRIX SIZE D DIRECTION |
| ME | 6 | | | MATRIX SIZE E DIRECTION |
| n | 52 | | | BALL COUNT |
| ϕb | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| e | 0.50 BSC. | | | BALL PITCH |
| SE / SD | 0.25 BSC. | | | SOLDER BALL PLACEMENT |
| | | | | |
| | 3A,3F,4A,4F,7A,7F,8A,8F | | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP 95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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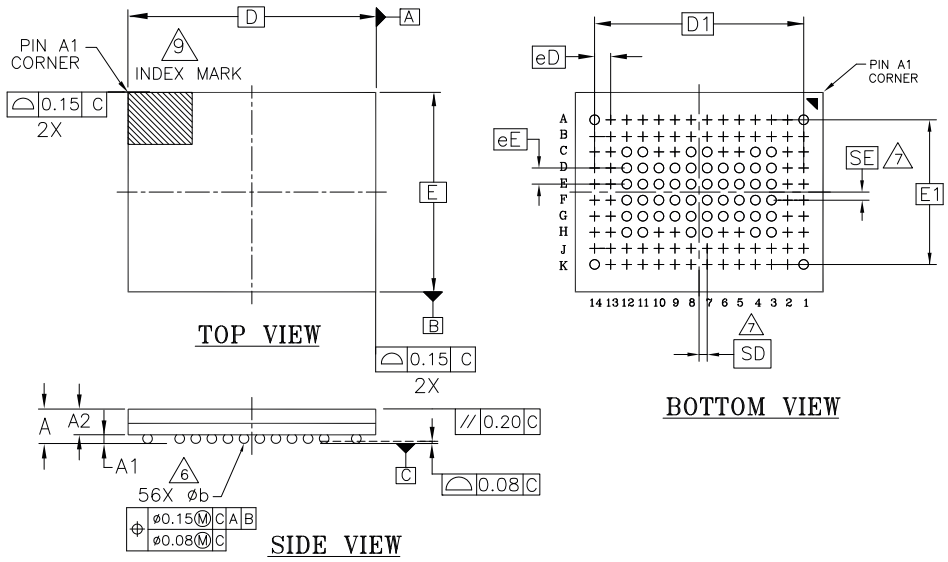
**Figure 4.4** RLA056 - 56-ball VFRBGA 7.7 x 6.2 mm




| PACKAGE | RLA 056 | | | |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D X E | 7.70 mm x 6.20 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | --- | --- | 1.00 | PROFILE |
| A1 | 0.18 | --- | --- | BALL HEIGHT |
| A2 | 0.62 | --- | 0.74 | BODY THICKNESS |
| D | 7.70 BSC. | | | BODY SIZE |
| E | 6.20 BSC. | | | BODY SIZE |
| D1 | 6.50 BSC. | | | MATRIX FOOTPRINT |
| E1 | 4.50 BSC. | | | MATRIX FOOTPRINT |
| MD | 14 | | | MATRIX SIZE D DIRECTION |
| ME | 10 | | | MATRIX SIZE E DIRECTION |
| n | 56 | | | BALL COUNT |
| ϕb | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| eE | 0.50 BSC. | | | BALL PITCH |
| eD | 0.50 BSC. | | | BALL PITCH |
| SE SD | 0.25 BSC. | | | SOLDER BALL PLACEMENT |
| | A2~A9, B1~B10, C1,C2, C9,C10,D1,D2,D9,D10 E1,E2,E3,E8,E9,E10,F1,F2, F3,F8,F9,F10,G1,G2,G9,G10 H1,H2,H9,H10,J1,J2,J3,J8,J9, J10,K1,K2,K3,K8,K9,K10 L1,L2,L9,L10,M1,M2,M9,M10, N1~N10, P2~P9 | | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP 95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X E
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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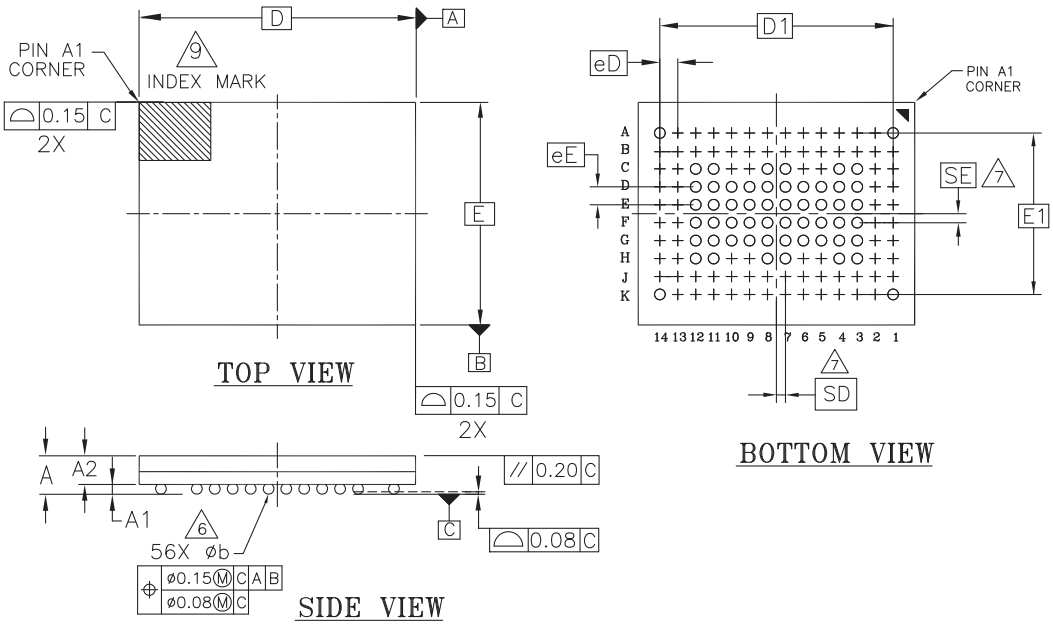
**Figure 4.5** RSD056—56-ball VFRBGA 7.7 x 6.2 mm




| PACKAGE | RSD 056 | | | NOTE |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D x E | 7.70 mm x 6.20 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | |
| A | 0.80 | 0.90 | 1.00 | PROFILE |
| A1 | 0.18 | --- | --- | BALL HEIGHT |
| A2 | 0.62 | --- | 0.74 | BODY THICKNESS |
| D | 7.70 BSC | | | BODY SIZE |
| E | 6.20 BSC | | | BODY SIZE |
| D1 | 6.50 BSC | | | MATRIX FOOTPRINT |
| E1 | 4.50 BSC | | | MATRIX FOOTPRINT |
| MD | 14 | | | MATRIX SIZE D DIRECTION |
| ME | 10 | | | MATRIX SIZE E DIRECTION |
| n | 56 | | | BALL COUNT |
| Øb | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| eE | 0.50 BSC | | | BALL PITCH |
| eD | 0.50 BSC | | | BALL PITCH |
| SE SD | 0.25 BSC | | | SOLDER BALL PLACEMENT |
| | A2~A9, B1~B10, C1,C2,C9,10,D1,D2,D9,D10 E1,E2,E3,E8,E9,E10,F1,F2,F3,F8,F9,F10,G1,G2,G9,G10 H1,H2,H9,H10,J1,J2,J3,J8,J9,J10,K1,K2,K3,K8,K9,K10 L1,L2,L9,L10,M1,M2,M9,M10, N1~N10, P2~P9 | | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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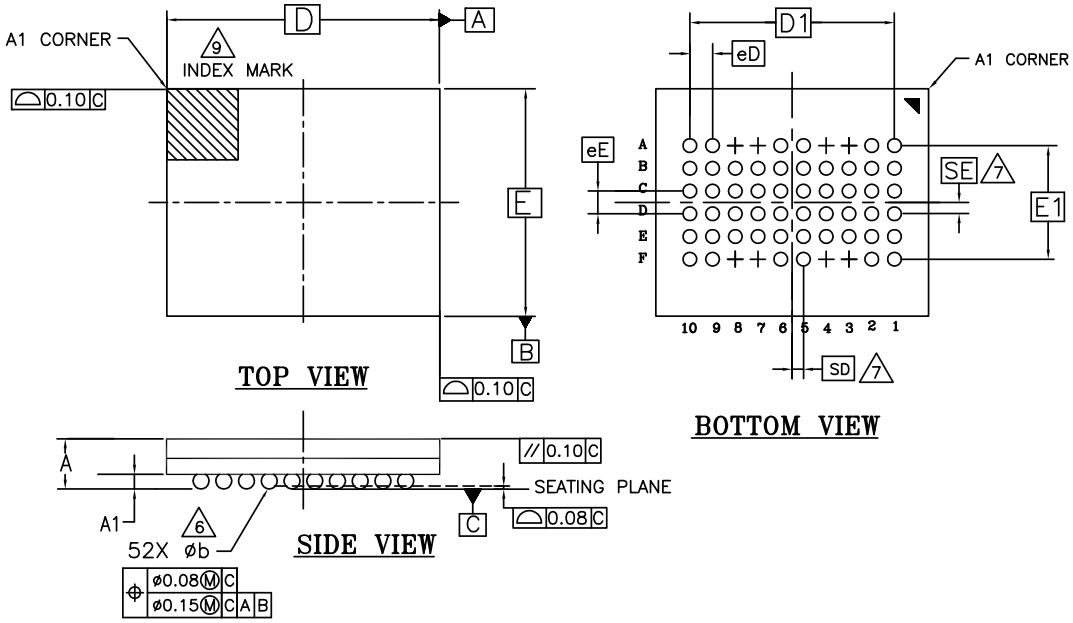
**Figure 4.6** RSE052—52-ball VFRBGA 6.0 x 5.0 mm




| PACKAGE | RSE 052 | | | |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D X E | 6.00 mm x 5.00 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | --- | --- | 1.00 | PROFILE |
| A1 | 0.18 | --- | --- | BALL HEIGHT |
| D | 6.00 BSC. | | | BODY SIZE |
| E | 5.00 BSC. | | | BODY SIZE |
| D1 | 4.50 BSC. | | | MATRIX FOOTPRINT |
| E1 | 2.50 BSC. | | | MATRIX FOOTPRINT |
| MD | 10 | | | MATRIX SIZE D DIRECTION |
| ME | 6 | | | MATRIX SIZE E DIRECTION |
| n | 52 | | | BALL COUNT |
| ϕb | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| e | 0.50 BSC. | | | BALL PITCH |
| SE / SD | 0.25 BSC. | | | SOLDER BALL PLACEMENT |
| | | | | |
| | 3A,3F,4A,4F,7A,7F,8A,8F | | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP 95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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# 5. Revision History

| Section | Description |
|---|---|
| **Revision 01 (August 25, 2008)** | |
| | Initial release |
| **Revision 02 (November 4, 2008)** | |
| Global | Added OPNs S71VS064RB0AHT00/04/80/84 |
| Connection Diagrams | Added S71VS-R 52-ball connection diagram |
| Physical Dimensions | Added RSB052 |
| General Description | Changed 128 Mb Mux pSRAM PID from TBD to pSRAM_39 |
| **Revision 03 (November 10, 2008)** | |
| General Description | Changed 64 Mb MUX pSRAM Type 3 PID from muxpsram_14 to muxpsram_15 |
| **Revision 04 (January 13, 2009)** | |
| Physical Dimensions | Replaced NLD056 with NSD056 |
| **Revision 05 (January 23, 2009)** | |
| Valid Combinations | Added OPN S71VS128RC0AHK20 |
| Physical Dimensions | Added RSD056 |
| **Revision 06 (March 11, 2009)** | |
| Valid Combinations | Added 108 MHz speed grade to S71VS128RC0 and S71VS256RC0 |
| **Revision 07 (September 29, 2009)** | |
| General Description | Added S71VS128RB0; added muxpsram_10 |
| Valid Combinations | Added OPN S71VS128RB0 |
| **Revision 08 (April 9, 2010)** | |
| General Description | Added SWM064D108M1R<br>Updated pSRAM documentation names |
| Valid Combinations | Added OPNs: S71VS128RC0AHK4L, S71VS256RC0AHK4L<br>Removed Bottom Boot options |
| Connection Diagrams | Updated $V_{SSQ}$ ball to $V_{SS}$ |
| **Revision 09 (May 4, 2010)** | |
| General Description | Added reference to S29VS064R data sheet<br>Removed CustComspec_01 for 32 Mb MUX pSRAM |
| Valid Combinations | Corrected pSRAM type for S71VS064RB0 from CustComspec_01 to SWM032D108M1R<br>Added OPNs: S71VS064RB0AHT0L, S71VS256RD0AHK40 |
| **Revision 10 (June 14, 2010)** | |
| General Description | Removed S71XS256RD0 from table<br>Unified data sheet reference for S29VS/XS-R<br>Removed MUX pSRAM Type 3<br>Added SWM128D108M1R |
| Valid Combinations | Restored necessary bottom boot options.<br>Added OPNs: S71VS256RD0AHK3L/BL/3C/BC<br>Removed OPNs: S71VS064RB0AHT00/04<br>Updated MUX pSRAM Type 3 entries to the Common RAM type specifications<br>Removed table after Figure 4.3 S71XS-R 56-ball Fine-Pitch Ball Grid Array |

| Section | Description |
|---|---|
| **Revision 11 (July 28, 2010)** | |
| Features | Corrected MCP BGA Packages information |
| Ordering Information | Corrected Package Modifier information<br>Removed 7 inch Tape and Reel option |
| Valid Combinations | Corrected package information for S71VS064RB0AHT0L<br>Added OPN S71VS064RB0AHT8L, S71VS128RC0AHKCL, S71VS256RC0AHKCL<br>Removed OPN S71VS256RD0AHK40 |
| MCP Block Diagram | Removed figure S71XS-R MCP Block Diagram |
| Connection Diagrams/ Physical Dimensions | Corrected figure S71VS-R 52-ball Fine-Pitch Ball Grid Array<br>Removed figure S71XS-R 56-ball Fine-Pitch Ball Grid Array<br>Replaced figure RSB052—52-ball VFBGA 5.0 x 7.5 mm with RSE052—52-ball VFRBGA 6.0 x 5.0 mm<br>Refreshed DNU/RFU/NC definitions |
| **Revision 12 (August 27, 2010)** | |
| Valid Combinations | Corrected package information for S71VS128RB0AHK0L/8L (RLA056)<br>Corrected speed for OPNs S71VS256RD0AHK3L/BL to 108 MHz |
| Connection Diagrams | Reverted DNU balls to RFU |
| Physical Dimensions | Added diagram for RLA056 |
| **Revision 13 (December 9, 2010)** | |
| Features | Added Industrial temperature |
| General Description | Added references to S29VS_XS-R_SP, S29VS064R_XS064R_SP, SWM032D108M3R, SWM128D108M3R |
| Valid Combinations | Added OPNs S71VS064RB0AHT3L/BL/0M/8M, S71VS128RB0AHK3L/BL, S71VS256RD0AHK3M, S71VS256RD0AHK40/C0<br>Added Temperature Range Column |
| **Revision 14 (April 13, 2011)** | |
| General Description | Removed SWM032D108M1N and SWM064D108M1N references |
| Valid Combinations | Removed OPNs S71VS064RB0AHT3M/BM, S71VS128RB0AHK2L/AL, S71VS128RC0AHK20, S71VS128RC0ZHKxx, S71VS256RC0ZHKxx, S71VS256RD0ZHExx<br>Physical Dimensions: Removed NLB056 and NSD056 diagrams. Added diagram for RLG052 |
| **Revision 15 (June 20, 2011)** | |
| Valid Combinations | Added OPNs S71VS128RB0AHK4L/CL, , S71VS064RB0AHT4L/CL |
| **Revision 16 (June 29, 2012)** | |
| Valid Combinations | Added OPNs S71VS064RB0AHT3M/BM |
| **Revision 17 (October 2, 2012)** | |
| Valid Combinations | Updated the S71VS256RC0AHK4L/CL package from RSD056 to RLA056 |
| **Revision 18 (January 31, 2014)** | |
| General Description | Removed 128 Mb MUX pSRAM Type 5 |
| Valid Combinations | Removed OPNs S71VS064RB0AHT0L/BL, S71VS256RD0AHK40/C0<br>Added OPN S71VS256RD0AHK4L/CL |

## Document History Page

| Document Title: S71VS/XS-R, MirrorBit® 1.8 V Simultaneous Read/Write Burst Mode Multiplexed Flash and Burst Mode pSRAM<br>Document Number: 002-00377 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | – | RYSU | 08/25/2008 | Initial release |
| *A | – | RYSU | 11/04/2008 | Global:<br>Added OPNs S71VS064RB0AHT00/04/80/84<br>Connection Diagrams:<br>Added S71VS-R 52-ball connection diagram<br>Physical Dimensions:<br>Added RSB052<br>General Description:<br>Changed 128 Mb Mux pSRAM PID from TBD to pSRAM_39 |
| *B | – | RYSU | 11/10/2008 | General Description:<br>Changed 64 Mb MUX pSRAM Type 3 PID from muxpsram_14 to muxpsram_15 |
| *C | – | RYSU | 01/13/2009 | Physical Dimensions:<br>Replaced NLD056 with NSD056 |
| *D | – | RYSU | 01/23/2009 | Valid Combinations:<br>Added OPN S71VS128RC0AHK20<br>Physical Dimensions:<br>Added RSD056 |
| *E | – | RYSU | 03/11/2009 | Valid Combinations:<br>Added 108 MHz speed grade to S71VS128RC0 and S71VS256RC0 |
| *F | – | RYSU | 09/29/2009 | General Description:<br>Added S71VS128RB0; added muxpsram_10<br>Valid Combinations:<br>Added OPN S71VS128RB0 |
| *G | – | RYSU | 04/09/2010 | General Description:<br>Added SWM064D108M1R<br>Updated pSRAM documentation names<br>Valid Combinations:<br>Added OPNs: S71VS128RC0AHK4L, S71VS256RC0AHK4L<br>Removed Bottom Boot options<br>Connection Diagrams:<br>Updated VSSQ ball to VSS |
| *H | – | RYSU | 05/04/2010 | General Description:<br>Added reference to S29VS064R data sheet<br>Removed CustComspec_01 for 32 Mb MUX pSRAM<br>Valid Combinations:<br>Corrected pSRAM type for S71VS064RB0 from CustComspec_01 to SWM032D108M1R<br>Added OPNs: S71VS064RB0AHT0L, S71VS256RD0AHK40 |

## Document History Page (Continued)

| Document Title: S71VS/XS-R, MirrorBit® 1.8 V Simultaneous Read/Write Burst Mode Multiplexed Flash and Burst Mode pSRAM<br>Document Number: 002-00377 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *I | – | RYSU | 06/14/2010 | General Description:<br>Removed S71XS256RD0 from table<br>Unified data sheet reference for S29VS/XS-R<br>Removed MUX pSRAM Type 3<br>Added SWM128D108M1R<br>Valid Combinations:<br>Restored necessary bottom boot options.<br>Added OPNs: S71VS256RD0AHK3L/BL/3C/BC<br>Removed OPNs: S71VS064RB0AHT00/04<br>Updated MUX pSRAM Type 3 entries to the Common RAM type specifications<br>Removed table after Figure 4.3 S71XS-R 56-ball Fine-Pitch Ball Grid Array |
| *J | – | RYSU | 07/28/2010 | Features:<br>Corrected MCP BGA Packages information<br>Ordering Information:<br>Corrected Package Modifier information<br>Removed 7 inch Tape and Reel option<br>Valid Combinations:<br>Corrected package information for S71VS064RB0AHT0L<br>Added OPN S71VS064RB0AHT8L, S71VS128RC0AHKCL, S71VS256RC0AHKCL<br>Removed OPN S71VS256RD0AHK40<br>MCP Block Diagram:<br>Removed figure S71XS-R MCP Block Diagram<br>Connection Diagrams/Physical Dimensions:<br>Corrected figure S71VS-R 52-ball Fine-Pitch Ball Grid Array<br>Removed figure S71XS-R 56-ball Fine-Pitch Ball Grid Array<br>Replaced figure RSB052—52-ball VFBGA 5.0 x 7.5 mm<br>with RSE052—52-ball VFRBGA 6.0 x 5.0 mm<br>Refreshed DNU/RFU/NC definitions |
| *K | – | RYSU | 08/27/2010 | Valid Combinations:<br>Corrected package information for S71VS128RB0AHK0L/8L (RLA056)<br>Corrected speed for OPNs S71VS256RD0AHK3L/BL to 108 MHz<br>Connection Diagrams:<br>Reverted DNU balls to RFU<br>Physical Dimensions:<br>Added diagram for RLA056 |
| *L | – | RYSU | 12/09/2010 | Features:<br>Added Industrial temperature<br>General Description:<br>Added references to S29VS_XS-R_SP, S29VS064R_XS064R_SP, SWM032D108M3R, SWM128D108M3R<br>Valid Combinations:<br>Added OPNs S71VS064RB0AHT3L/BL/0M/8M, S71VS128RB0AHK3L/BL, S71VS256RD0AHK3M, S71VS256RD0AHK40/C0<br>Added Temperature Range Column |

## Document History Page (Continued)

| Document Title: S71VS/XS-R, MirrorBit® 1.8 V Simultaneous Read/Write Burst Mode Multiplexed Flash and Burst Mode pSRAM<br>Document Number: 002-00377 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *M | – | RYSU | 04/13/2011 | General Description:<br>Removed SWM032D108M1N and SWM064D108M1N references<br>Valid Combinations:<br>Removed OPNs S71VS064RB0AHT3M/BM, S71VS128RB0AHK2L/AL, S71VS128RC0AHK20, S71VS128RC0ZHKxx, S71VS256RC0ZHKxx, S71VS256RD0ZHExx<br>Physical Dimensions: Removed NLB056 and NSD056 diagrams. Added diagram for RLG052 |
| *N | – | RYSU | 06/20/2011 | Valid Combinations:<br>Added OPNs S71VS128RB0AHK4L/CL, S71VS064RB0AHT4L/CL |
| *O | – | RYSU | 06/29/2012 | Valid Combinations:<br>Added OPNs S71VS064RB0AHT3M/BM |
| *P | – | RYSU | 10/02/2012 | Valid Combinations:<br>Updated the S71VS256RC0AHK4L/CL package from RSD056 to RLA056. |
| *Q | – | RYSU | 01/31/2014 | General Description:<br>Removed 128 Mb MUX pSRAM Type 5<br>Valid Combinations:<br>Removed OPNs S71VS064RB0AHT0L/BL, S71VS256RD0AHK40/C0<br>Added OPN S71VS256RD0AHK4L/CL |
| *R | 5175865 | RYSU | 03/23/2016 | Updated , *General Description* on page 2:<br>Updated table for detailed specifications:<br>Replaced “Publication Identification Number” with “Cypress Document Number” in column heading.<br>Replaced “S29VS/XS-R” with “S29VS256R, S29VS128R datasheet” in “Document” column.<br>Replaced “S29VS_XS-R_00” with “002-00833” in “Cypress Document Number” column.<br>Removed “S29VS/XS-R Supplement” document and its details.<br>Replaced “S29VS064R/XS064R” with “S29VS064R datasheet” in “Document” column.<br>Replaced “S29VS_XS064R_00” with “002-00949” in “Cypress Document Number” column.<br>Removed “S29VS064R/XS064R Supplement” document and its details.<br>Updated to Cypress template. |
| *S | 5965598 | AESATMP8 | 11/13/2017 | Updated logo and Copyright. |

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