Data Sheet
November 2016

MAX24287
1Gbps Parallel-to-Serial MII Converter

General Description

The MAX24287 is a flexible, low-cost Ethernet interface conversion IC. The parallel interface can be configured for GMII, RGMII, TBI, RTBI, or 10/100 MII, while the serial interface can be configured for 1.25Gbps SGMII or 1000BASE-X operation. In SGMII mode, the device interfaces directly to Ethernet switch ICs, ASIC MACs, and 1000BASE-T electrical SFP modules. In 1000BASE-X mode, the device interfaces directly to 1Gbps 1000BASE-X SFP optical modules. The MAX24287 performs automatic translation of link speed and duplex autonegotiation between parallel MII MDIO and the serial interface.

This device is ideal for interfacing single-channel GMII/MII devices such as microprocessors, FPGAs, network processors, Ethernet-over-SONET or -PDH mappers, and TDM-over-packet circuit emulation devices. The device also provides a convenient solution to interface such devices with electrical or optical Ethernet SFP modules.

Applications

Any System with a Need to Interface a Component with a Parallel MII Interface (GMII, RGMII, TBI RTBI, 10/100 MII) to a Component with an SGMII or 1000BASE-X Interface

Switches and Routers

Telecom Equipment

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX24287ETK+	-40°C to +85°C	68 TQFN-EP*
MAX24287ETK+T	-40°C to +85°C	68 TQFN-EP* Tape and Reel

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Block Diagram appears on page 7.

Register Map appears on page 42.

Highlighted Features

- **Bidirectional Wire-Speed Ethernet Interface Conversion**
- **Can Interface Directly to SFP Modules and SGMII PHY and Switch ICs**
- **Serial Interface Configurable as 1000BASE-X or SGMII Revision 1.8 (4-, 6-, or 8-Pin)**
- **Parallel Interface Configurable as GMII, RGMII, TBI, RTBI, or 10/100 MII**
- **Serial Interface Has Clock and Data Recovery Block (CDR) and Does Not Require a Clock Input**
- **Translates Link Speed and Duplex Mode Negotiation Between MDIO and SGMII PCS**
- **Supports 10/100 MII or RGMII Operation with SGMII Running at the Same Rate**
- **Configurable for 10/100 MII DTE or DCE Modes (i.e., Connects to PHY or MAC)**
- **Can Also Be Configured as General-Purpose 1:10 SerDes with Optional Comma Alignment**
- **Supports Synchronous Ethernet by Providing a 25MHz or 125MHz Recovered Clock and Accepting a Transmit Clock**
- **Can Provide a 125MHz Clock for the MAC to Use as GTXCLK**
- **Accepts 10MHz, 12.8MHz, 25MHz or 125MHz Reference Clock**
- **Software Control Through MDIO Interface**
- **GPIO Pins Can Be Configured as Clocks, Status Signals and Interrupt Outputs**
- **1.2V Operation with 3.3V I/O**
- **Small, 8mm x 8mm, 68-Pin TQFN Package**

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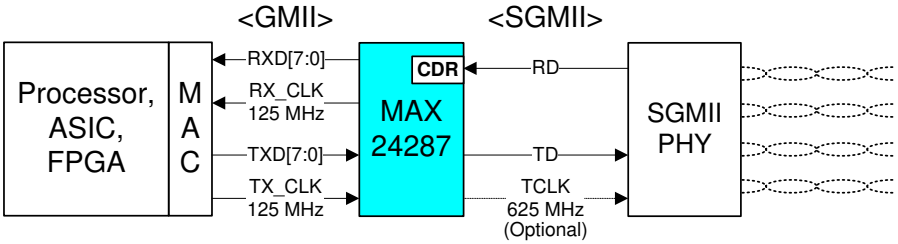
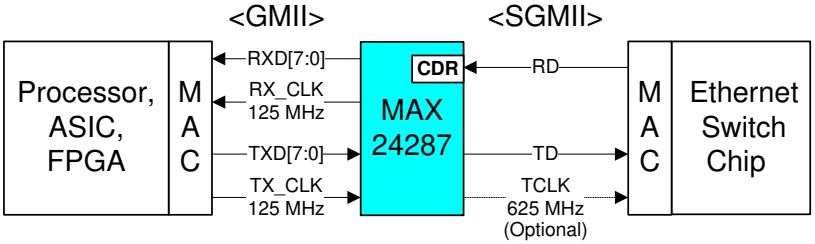
1. Application Examples

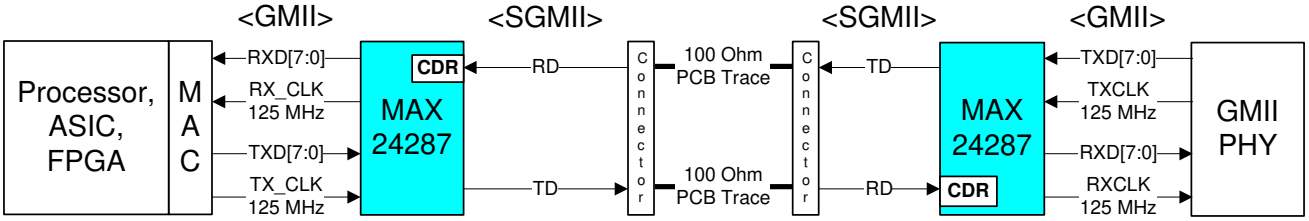
a) Copper Media



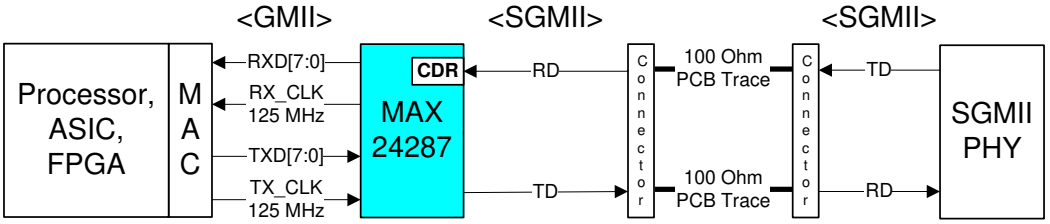
b) Connect Parallel MII Component to SGMII Component



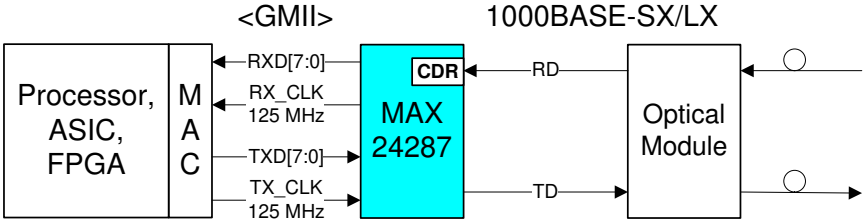
c1) Long PCB Trace Card-to-Card



c2)

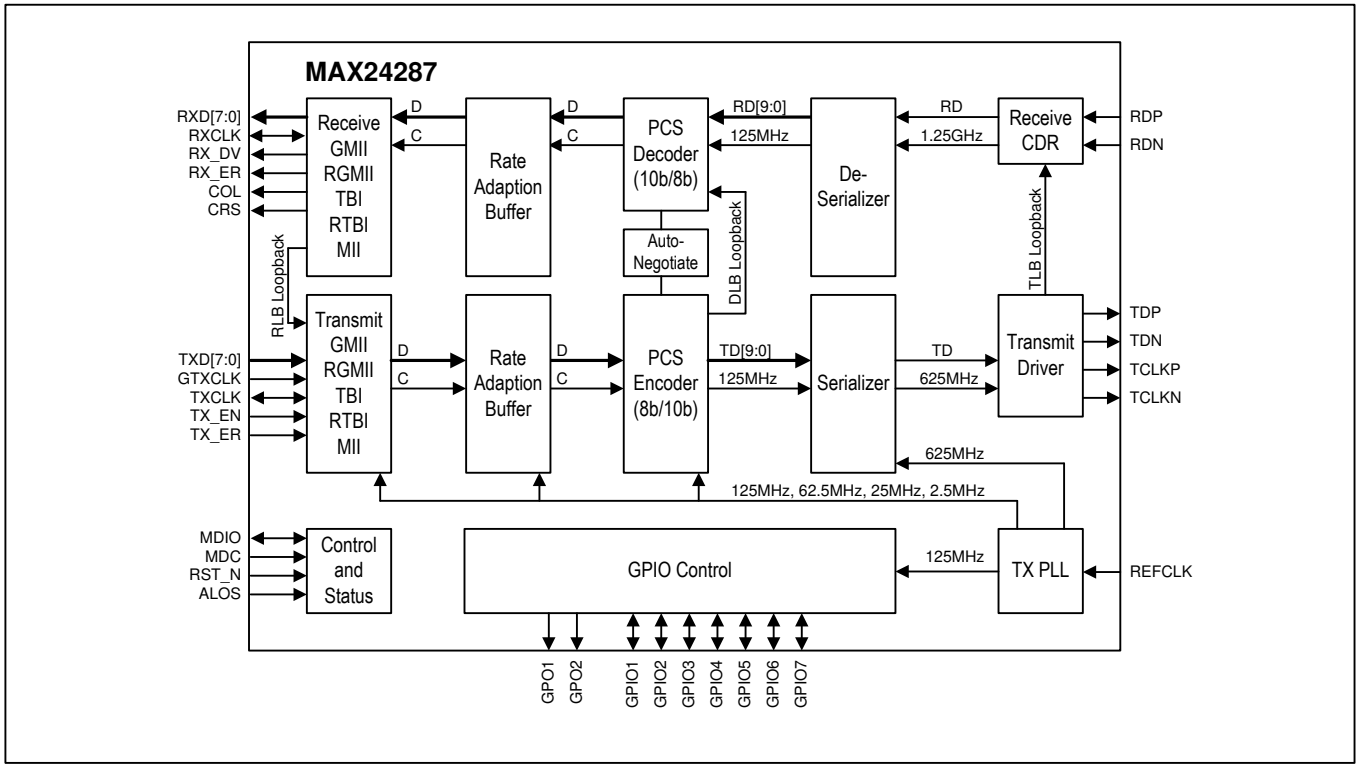


d) Fiber Module



2. Block Diagram

Figure 2-1. Block Diagram



3. Detailed Features

General Features

- High-speed MDIO interface (12.5MHz slave only) with optional preamble suppression
- Operates from a 10, 12.8, 20, 25, or 125MHz reference clock
- Optional 125MHz output clock for MAC to use as GTXCLK

Parallel-Serial MII Conversion Features

- Bidirectional wire-speed interface conversion
- Serial Interface: 1000BASE-X or SGMII revision 1.8 (4-, 6-, or 8-Pin)
- Parallel Interface: GMII, RGMII (10, 100 and 1000Mbps), TBI, RTBI or 10/100 MII (DTE or DCE)
- 8-pin source-clocked SGMII mode
- 4-pin 1000BASE-X SerDes mode to interface with optical modules
- Connects processors with parallel MII interfaces to 1000BASE-X SFP optical modules
- Connects processors with parallel MII interfaces to PHY or switch ICs with SGMII interfaces
- Interface conversion is transparent to MAC layer and higher layers
- Translates link speed and duplex mode between GMII/MII MDIO and SGMII PCS
- Configurable for 10/100 MII DTE or DCE Modes (i.e., connects to PHY or MAC)

Synchronous Ethernet Features

- Receive path bit clock can be output on a GPIO pin to line-time the system from the Ethernet port
- Transmit path can be frequency-locked to a system clock signal connected to the REFCLK pin

4. Acronyms, Abbreviations, and Glossary

- DCE Data Communication Equipment
- DDR Dual Data Rate (data driven and latched on both clock edges)
- DTE Data Terminating Equipment
- PCB Printed Circuit Board
- PHY Physical. Refers to either a transceiver device or a protocol layer

- Ingress The serial (SGMII) to parallel (GMII) direction
- Egress The parallel (GMII) to serial (SGMII) direction
- Receive The serial (SGMII) to parallel (GMII) direction
- Transmit The parallel (GMII) to serial (SGMII) direction

5. Pin Descriptions

Note that some pins have different pin names and functions under different configurations.

Table *5-1. Pin Type Definitions*

Type	Definition
I	Input
Idiff	Input, differential
Ipu	Input, with pullup
Ipd	Input, with pulldown
IO	Bidirectional
IOr	Bidirectional, sampled at reset
IOz	Bidirectional, can go high impedance
O	Output
Odiff	Output, differential (CML)
Oz	Output, can go high impedance

Table 5-2. Detailed Pin Descriptions – Global Pins (2 Pins)

Pin Name	PIN #	Type	Pin Description
RST_N	67	I	**Reset** (active low, asynchronous) This signal resets all logic, state machines and registers in the device. Pin states are sampled and used to set the default values of several register fields as described in 6.1. RST_N should be held low for at least 100µs. See section 6.3.1.
REFCLK	68	I	**Reference Clock** This signal is the reference clock for the device. The frequency can be 10MHz, 12.8MHz, 25MHz or 125MHz ± 100 ppm. At reset the frequency is specified using the RXD[3:2] pins (see section 6.1). The REFCLK signal is the input clock to the TX PLL. See section 6.9. Note: REFCLK frequency cannot be changed dynamically among the frequencies listed above. To change REFCLK frequency, (1) power down MAX24287, (2) change REFCLK frequency, then (3) power up MAX24287. REFCLK is an analog input that is internally biased with a 10kΩ resistor to 1.2V. This support AC-coupling if desired.

Pin Name	PIN #	Type	Pin Description
TEST0	45	I	**Factory Test.** Connect to DVDD33.
TEST1	64	I	**Factory Test.** Connect to DVDD33 or DVSS.
TEST2	63	I	**Factory Test.** Connect to DVDD33 or DVSS.
TEST3	62	I/O	**Factory Test.** Connect to DVDD33 or DVSS.

Table 5-3. Detailed Pin Descriptions – MDIO Interface (2 Pins)

Pin Name	PIN #	Type	Pin Description
MDC	41	I	**MDIO Clock.** MDC is the clock signal of the 2-wire MDIO interface. It can be any frequency up to 12.5MHz. See section 6.4.
MDIO	42	IOz	**MDIO Data.** This is the bidirectional, half-duplex data signal of the MDIO interface. It is sampled and updated on positive edges of MDC. IEEE 802.3 requires a 2kΩ±5% pulldown resistor on this signal at the MAC. See section 6.4.

Table 5-4. Detailed Pin Descriptions – JTAG Interface (5 pins)

Pin Name	PIN #	Type	Pin Description
JTRST_N	43	I	**JTAG Test Reset** (active low). Asynchronously resets the test access port (TAP) controller. JTRST_N should be held low during device power-up. If not used, JTRST_N can be held low or high after power-up. See section 7.2.18.
JTCLK	21	I	**JTAG Test Clock.** This clock signal can be any frequency up to 10MHz. JTDI and JTMS are sampled on the rising edge of JTCLK, and JTDO is updated on the falling edge of JTCLK. If not used, connect to DVDD33 or DVSS. See section 7.2.18.
JTMS	22	I	**JTAG Test Mode Select.** Sampled on the rising edge of JTCLK. Used to place the port into the various defined IEEE 1149.1 states. If not used, connect to DVDD33. See section 7.2.18.
JTDI	23	I	**JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, connect to DVDD33. See section 7.2.18.
JTDO	44	Oz	**JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used leave unconnected. See section 7.2.18.

Table 5-5. Detailed Pin Descriptions – GPIO signals (5 dedicated pins, 4 shared pins)

Pin Name	PIN #	Type	Pin Description
GPO1	24	IOr	**General Purpose Output 1.** After reset, this pin can either be high impedance (TBI or RTBI mode) or an output that indicates link status, 0=link down, 1=link up. The function can be changed after reset. See section 6.2.
GPO2	25	IOr	**General Purpose Output 2.** After reset, this pin can either be high impedance (TBI or RTBI mode) or an output that indicates CRS (carrier sense). The function can be changed after reset. See section 6.2.

Pin Name	PIN #	Type	Pin Description
GPIO1	61	IOz	**General Purpose Input or Output 1.** After reset this pin can be either high impedance or generating a 125MHz clock signal. GPO1=0 at reset: After reset, GPIO1 is high impedance. GPO1=1 at reset: After reset, GPIO1 is 125MHz clock out The function can be changed after reset. See section 6.2.
GPIO2	60	IOz	**General Purpose Input or Output 2.** After reset this pin is high impedance. The function can be changed after reset. See section 6.2.
GPIO3	59	IOz	**General Purpose Input or Output 3.** After reset this pin is high impedance. The function can be changed after reset. See section 6.2.
GPIO4/TXD[4]	52	IOz	**General Purpose Input or Output 4.** Available for use as a GPIO pin when the parallel interface is configured for MII, RGMII or RTBI modes. After reset this pin is high impedance. The function can be changed after reset. See section 6.2.
GPIO5/TXD[5]	53	IOz	**General Purpose Input or Output 5.** Available for use as a GPIO pin when the parallel interface is configured for MII, RGMII or RTBI modes. After reset this pin is high impedance. The function can be changed after reset. See section 6.2.
GPIO6/TXD[6]	54	IOz	**General Purpose Input or Output 6.** Available for use as a GPIO pin when the parallel interface is configured for MII, RGMII or RTBI modes. After reset this pin is high impedance. The function can be changed after reset. See section 6.2.
GPIO7/TXD[7]	55	IOz	**General Purpose Input or Output 7.** Available for use as a GPIO pin when the parallel interface is configured for MII, RGMII or RTBI modes. After reset this pin is high impedance. The function can be changed after reset. See section 6.2.

Table 5-6. Detailed Pin Descriptions – SGMII/1000BASE-X Serial Interface (7 pins)

Pin Name	PIN #	Type	Pin Description
TDP, TDN	9 8	Odiff	**Transmit Data Output** These pins form a differential CML output for the 1.25Gbaud SGMII transmit signal to a neighboring 1000BASE-X optical module (SFP, etc.) or PHY with SGMII interface. See section 6.5.
TCLKP, TCLKN	6 5	Odiff	**Transmit Clock Output** These pins form a differential CML output for an optional 625MHz clock for the SGMII transmit signal on TDP/TDN. This output is disabled at reset but is enabled by setting CR.TCLK_EN=1. See section 6.5.
RDP, RDN	13 14	Idiff	**Receive Data Input** These pins form a differential input for the 1.25Gbaud SGMII receive signal from a neighboring 1000BASE-X optical module (SFP, etc.) or PHY with SGMII interface. A receive clock signal is not necessary because the device uses a built-in CDR to recover the receive clock from the signal on RDP/RDN. See section 6.5.
ALOS	19	I	**Analog Loss of Signal** This pin receives analog loss-of-signal from a neighboring optical transceiver module. If the optical module does not have an ALOS output, this pin should be connected to DVSS for proper operation. See section 6.5. 0 = ALOS not detected or not required, normal operation 1 = ALOS detected, loss of signal

Table 5-7. Detailed Pin Descriptions – Parallel Interface (25 pins)

Pin Name	PIN #	Type	Pin Description
RXCLK	40	IO	**Receive Clock** In all modes the frequency tolerance is ± 100 ppm. GMII Mode: RXCLK is the 125MHz receive clock. RGMII Modes: RXCLK is the 125MHz (RGMII-1000), 25MHz (RGMII-100) or 2.5MHz (RGMII-10) receive clock (DDR). TBI Mode: In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), RXCLK is the 62.5MHz receive clock for odd code groups and TXCLK/RCXCLK1 is the 62.5MHz receive clock for even code groups. In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset), RXCLK is the 125MHz receive clock. RTBI Mode: RXCLK is the 125MHz receive clock (DDR). MII Mode: RXCLK is the 25MHz (100Mbps MII) or 2.5MHz (10Mbps MII) receive clock. In DTE mode (DCE_DTE)=1, RXCLK is an input. In DCE mode (DCE_DTE)=0, RXCLK is an output.

Pin Name	PIN #	Type	Pin Description
RXD[0] RXD[1] RXD[2] RXD[3] RXD[4] RXD[5] RXD[6] RXD[7]	38 37 36 35 34 33 32 31	IOr	**Receive Data Outputs** During reset these pins are configuration inputs. See section 6.1. After reset they are driven as outputs. GMII Mode: receive_data[7:0] is output on RXD[7:0] on the rising edge of RXCLK. MII, RGMII-10 and RGMII-100 Modes: receive_data[3:0] is output on RXD[3:0] on the rising edge of RXCLK. RXD[7:4] are high impedance. RGMII-1000 Mode: receive_data[3:0] is output on RXD[3:0] on the rising edge of RXCLK, and receive_data[7:4] is output on the falling edge of RXCLK. RXD[7:4] are high impedance. TBI Mode: In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), receive_data[7:0] is output on RXD[7:0], receive_data[8] is output on RX_DV, and receive_data[9] is output on RX_ER on the rising edge of RXCLK and the rising edge of RXCLK1 (both 62.5MHz, 180 degrees out of phase). In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset), these same signals are output on the rising edge of RXCLK (125MHz). RTBI Mode: Receive_data[3:0] is output on RXD[3:0] and Receive_data[4] is output on RX_DV on the rising edge of RXCLK. Receive_data[8:5] is output on RXD[3:0] and receive_data[9] is output on RX_DV on the falling edge of RXCLK. RXD[7:4] are high impedance.
RX_DV	29	IOr	**Receive Data Valid** During reset this pin is a configuration input. See section 6.1. After reset it is driven as an output. MII Mode and GMII Mode: RX_DV is output on the rising edge of RXCLK. RGMII Modes: The RX_CTL signal is output on RX_DV on both edges of RXCLK. TBI Mode: In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), receive_data[8] is output on RX_DV on the rising edge of RXCLK and the rising edge of RXCLK1 (both 62.5MHz, 180 degrees out of phase). In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset), receive_data[8] is output on RX_DV on the rising edge of RXCLK (125MHz). RTBI Mode: Receive_data[4} is output on RX_DV on the rising edge of RXCLK. Receive_data[9] is output on RX_DV on the falling edge of RXCLK.
RX_ER	28	IOr	**Receive Error** During reset this pin is a configuration input. See section 6.1. After reset it is driven as an output. MII Mode and GMII Mode: RX_ER is output on the rising edge of RXCLK. RGMII Mode and RTBI Mode: RX_ER pin is high impedance. TBI Mode: In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), receive_data[9] is output on RX_ER on the rising edge of RXCLK and the rising edge of RXCLK1 (both 62.5MHz, 180 degrees out of phase). In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset), receive_data[9] is output on the rising edge of RXCLK (125MHz).

Pin Name	PIN #	Type	Pin Description
COL	27	IOr	**Collision Detect** During reset this pin is a configuration input. See section 6.1. After reset it is driven as an output. MII Mode. GMII Mode and RGMII Modes: COL indicates that a Tx/Rx collision is occurring. It is meaningful only in half duplex operation. It is asynchronous to any of the clocks. COL is driven low at all times when BMCR.DLB=1 and BMCR.COL_TEST=0. When BMCR.DLB=1 and BMCR.COL_TEST=1, COL behaves as described in the COL_TEST bit description. 1 = Collision is occurring 0 = Collision is not occurring TBI Mode and RTBI Mode: This pin is high impedance.
CRS/COMMA	26	IOr	**Carrier Sense / Comma Detect** During reset this pin is a configuration input. See section 6.1. After reset it is driven as an output. MII Mode. GMII Mode and RGMII Modes: CRS is asserted by the device when either the transmit data path or the receive data path is active. This signal is asynchronous to any of the clocks. TBI Mode and RTBI Mode: COMMA is asserted by the device when a comma pattern is detected in the receive data stream. In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), COMMA is updated on the rising edge of RXCLK and the rising edge of RXCLK1 (both 62.5MHz, 180 degrees out of phase). In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset) and RTBI mode, COMMA is updated on the rising edge of RXCLK (125MHz).
TXCLK/ RXCLK1	46	IO	**MII Transmit Clock** When TXCLK is an input, frequency tolerance is ±100ppm. MII Mode: TXCLK is the 25MHz (100Mbps MII) or 2.5MHz 10Mbps MII) transmit clock. In DTE mode (DCE_DTE)=1, TXCLK is an input. In DCE mode (DCE_DTE)=0, TXCLK is an output. GMII Mode, RGMII Mode and RTBI Mode: TXCLK can output a 125MHz clock for use by neighboring components (e.g. a MAC) when GMIICR.TXCLK_EN=1 (or TXCLK=1 at reset). TBI Mode: In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), this pin becomes the 62.5MHz RXCLK1 output for even code groups. In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset), TXCLK can output a 125MHz clock for use by neighboring components (e.g. a MAC) when GMIICR.TXCLK_EN=1 (or TXCLK=1 at reset).

Pin Name	PIN #	Type	Pin Description
GTXCLK	66	I	**GMII/RGMII Transmit Clock** In all modes the frequency tolerance is ± 100ppm. GMII Mode: GTXCLK is the 125MHz transmit clock. RGMII Modes: GTXCLK is the 125MHz (RGMII-1000), 25MHz (RGMII-100) or 2.5MHz (RGMII-10) transmit clock (DDR). TBI Mode: GTXCLK is the 125MHz transmit clock. RTBI Mode: GTXCLK is the 125MHz transmit clock (DDR). MII Mode: This pin is not used and should be pulled low. See the TXCLK pin description.
TXD[0] TXD[1] TXD[2] TXD[3] TXD[4]/GPIO4 TXD[5]/GPIO5 TXD[6]/GPIO6 TXD[7]/GPIO7	48 49 50 51 52 53 54 55	I I I I IOz IOz IOz IOz	**Transmit Data Inputs** Depending on the parallel MII interface mode, four or eight of these pins are used to accept transmit data from a neighboring component. GMII Mode: The rising edge of GTXCLK latches transmit_data[7:0] from TXD[7:0]. MII, RGMII-10 and RGMII-100 Modes: The rising edge of TXCLK (MII) or GTXCLK (RGMII) latches transmit_data[3:0] from TXD[3:0]. TXD[7:4] become GPIO7 – GPIO4. RGMII-1000 Mode: The rising edge of GTXCLK latches transmit_data[3:0] from TXD[3:0]. The falling edge of GTXCLK latches transmit_data[7:4] from TXD[3:0]. TXD[7:4] become GPIO7 – GPIO4. TBI Mode: The rising edge of GTXCLK latches transmit_data[7:0] from TXD[7:0], transmit_data[8] from TX_EN and transmit_data[9] from TX_ER. RTBI Mode: The rising edge of GTXCLK latches transmit_data[3:0] from TXD[3:0] and transmit_data[4] from TX_EN. The falling edge of GTXCLK latches transmit_data[8:5] from TXD[3:0] and transmit data[9] from TX_EN. TXD[7:4] become GPIO7 – GPIO4.
TX_EN	57	I	**Transmit Enable** MII Mode and GMII Mode: The rising edge of TXCLK (MII) or GTXCLK (GMII) latches the TX_EN signal from this pin. RGMII Modes: Both edges of GTXCLK latch the TX_CTL signal from this pin. TBI Mode: The rising edge of GTXCLK latches transmit_data[7:0] from TXD[7:0], transmit_data[8] from TX_EN and transmit_data[9] from TX_ER. RTBI Mode: The rising edge of GTXCLK latches transmit_data[3:0] from TXD[3:0] and transmit_data[4] from TX_EN. The falling edge of GTXCLK latches transmit_data[8:5] from TXD[3:0] and transmit data[9] from TX_EN.

Pin Name	PIN #	Type	Pin Description
TX_ER	58	I	**Transmit Error** MII Mode and GMII Mode: The rising edge of TXCLK (MII) or GTXCLK (GMII) latches the TX_ER signal from this pin. RGMII Modes: This pin is not used. TBI Mode: The rising edge of GTXCLK latches transmit_data[7:0] from TXD[7:0], transmit_data[8] from TX_EN and transmit_data[9] from TX_ER. RTBI Mode: This pin is not used.

Table 5-8. Detailed Pin Descriptions – Power and Ground Pins (17 pins)

Pin Name	PIN #	Pin Description
DVDD12	30, 56	Digital Power Supply, 1.2V (2 pins)
DVDD33	20, 39, 65	Digital Power Supply, 3.3V
DVSS	47	Return for DVDD12 and DVDD33
RVDD12	16	1.25G Receiver Analog Power Supply, 1.2V
RVDD33	12	1.25G Receiver Analog Power Supply, 3.3V
RVSS	15	Return for RVDD12 and RVDD33
TVDD12	11	1.25G Transmitter Analog Power Supply, 1.2V
TVDD33	7	1.25G Transmitter Analog Power Supply, 3.3V
TVSS	10	Return for TVDD12 and TVDD33
CVDD12	3	TX PLL Analog Power Supply, 1.2V
CVDD33	2	TX PLL Analog Power Supply, 3.3V
CVSS	4	Return for CVDD12 and CVDD33
GVDD12	18	Analog Power Supply, 1.2V
GVSS	1	Return for GVDD12.
Exposed Pad	EP	Exposed pad (die paddle). Connect to ground plane. EP also functions as a heatsink. Solder to the circuit-board ground plane to maximize thermal dissipation.

6. Functional Description

6.1 Pin Configuration During Reset

The MAX24287 initial configuration is determined by pins that are sampled at reset. The values on these pins are used to set the reset values of several register bits. Note that the behavior described in this section cannot be used for “hardware-only” operation. Some register accesses through the MDIO interface are required for proper operation as described in section 6.14.

The pins that are sampled at reset to pin-configure the device are listed described in Table 6-1. During reset these pins are high-impedance inputs and require 10kΩ pullup or pulldown resistors to set pin-configuration values. After reset, the pins can become outputs if configured to do so and operate as configured. There are two pin configuration modes: 15-pin mode and 3-pin mode.

In 15-pin mode (COL=0 during reset, see Table 6-1) all major settings associated with the PCS block are configurable. In addition, the input reference clock frequency on the REFCLK pin is configured during reset using the RXD[3:2] pins.

Table 6-1. Reset Configuration Pins, 15-Pin Mode (COL=0)

Pin	Function	Register Bit Affected	Notes
CRS	Double Date Rate	GMIICR:DDR=CRS	See Table 6-2.
GPO2	10/100 MII: DTE or DCE	10/100 MII: GMIICR:DTE_DCE	0=DCE, 1=DTE (serial interface is configured for SGMII mode, PCSCR:BASEX=0)
	Other: Serial Interface	Other: PCSCR:BASEX	0=SGMII, 1=1000BASE=X
GPO1	GPIO1 Configuration	GPIOCR1.GPIO1_SEL[2]	0=high impedance 1=125MHz from TX PLL
RXD[1:0]	Parallel Interface Speed	GMIICR:SPD[1:0]	See Table 6-2.
RXD[3:2]	REFCLK Frequency	None	00=10MHz, 01=12.8MHz, 10=25MHz, 11=125MHz
RXD[7:4]	MDIO PHYAD[3:0].	Internal MDIO PHYAD register (device address on MDIO bus).	Note: PHYAD[4:0]=11111 enables factory test mode. Do not use.
RX_ER	MDIO PHYAD[4].		
RX_DV	TBI Mode	GMIICR:TBI_RATE	0=one-clock mode (125MHz) 1=normal mode (62.5MHz x 2)
	Other: Auto-negotiation	BMCR:AN_EN	0=Disable, 1=Enable
TXCLK	TXCLK Enable	GMIICR:TXCLK_EN	0=high impedance 1=125MHz from TX PLL Ignored in MII mode and TBI with two 62.5MHz Rx clocks

Table 6-2. Parallel Interface Configuration

SPD[1]	SPD[0]	Speed	DDR=0	DDR=1
0	0	10Mbps	MII	RGMII-10
0	1	100Mbps	MII	RGMII-100
1	0	1000Mbps	GMII	RGMII-1000
1	1	1000Mbps	TBI	RTBI

In 3-pin mode (COL=1 during reset, see Table 6-3) the device is configured for a 1000Mbps RGMII or GMII parallel interface. This mode is targeted to the application of connecting an ASIC, FPGA or processor with an RGMII or GMII interface to a switch device with an SGMII interface or to a 1000BASE-X optical interface. In 3-pin mode, the REFCLK pin is configured for 25MHz, the PHY address is set to 0x04, 1000BASE-X auto-negotiation (or automatic transmission of SGMII control information) is enabled, TXCLK is configured to output a 125MHz clock, and the

TCLKP/TCLKN differential pair is disabled. Note: if RX_ER and RXD[7:4] are all high when the device exits reset then the device enters factory test mode; for normal operation set these pins to any other combination of values.

Table 6-3. Reset Configuration Pins, 3-Pin Mode (COL=1)

Pin	Function	Register Bit Affected	Notes
CRS	Double Date Rate	GMIICR:DDR=CRS	0=GMII, 1=RGMII
GPO2	Serial Interface	PCSCR:BASEX	0=SGMII, 1=1000BASE=X

Note: In 3-pin mode register fields are automatically set as follows: REFCLK clock rate to 25MHz, GMIICR:SPD[1:0]=10, MDIO PHYAD is set to 0x04, BMCR:AN_EN=1, GMIICR:TXCLK_EN=1, GPIOCR1=0 and GPIOCR2=0. All other registers are reset to normal defaults listed in the register descriptions.

6.2 General-Purpose I/O

The MAX24287 has two general-purpose output pins, GPO1, GPO2, and seven general-purpose input/output pins, GPIO1 through GPIO7. Each pin can be configured to drive low or high or be in a high-impedance state. Other uses for the GPO and GPIO pins are listed in Table 6-4 through Table 6-6. The GPO and GPIO pins are each configured using a GPxx_SEL field in registers GPIOCR1 or GPIOCR2 with values as indicated in the tables below.

When a GPIO pin is configured as high impedance it can be used as an input. The real-time state of GPIOx can be read from GPIOSR.GPIOx. In addition, a latched status bit GPIOSR.GPIOxL is available for each GPIO pin. This latched status bit is set when the transition specified by GPIOCR2.GPIO13_LSC (for GPIO1 through GPIO3) or by GPIOCR2.GPIO47_LSC (for GPIO4 through GPIO7) occurs on the pin.

Note that GPIO4 through GPIO7 are alternate pin functions to TXD[7:4] and therefore are only available when the parallel MII is configured for MII, RGMII or RTBI.

Table 6-4. GPO1, GPIO1 and GPIO3 Configuration Options

GPxx_SEL	Description
000	High impedance, not driven, can be an used as an input
001	Drive logic 0
010	Drive logic 1
011	Interrupt output, active low. GPO1 drives low and high, GPIO1 and GPIO3 are open-drain.
100	Output 125MHz from the TX PLL
101	Output 25MHz or 125MHz from receive clock recovery PLL. Not squelched. Frequency specified by CR.RCFREQ.
110	Output real-time link status, 0=link down, 1=link up
111	reserved value, do not use

Table 6-5. GPO2 and GPIO2 Configuration Options

GPxx_SEL	Description
000	High impedance, not driven, can be an used as an input
001	Drive logic 0
010	Drive logic 1
011	reserved value, do not use
100	Output 125MHz from TX PLL
101	Output 25MHz or 125MHz from receive clock recovery PLL. The frequency is specified by CR.RCFREQ. Signal is automatically squelched (driven low) when CR.RCSQL=1 and any of several conditions occur. See section 6.2.1.
110	Output CRS (carrier sense) status
111	reserved value, do not use

Table 6-6. GPIO4, GPIO5, GPIO6 and GPIO7 Configuration Options

GPxx_SEL	Description
000	High impedance, not driven, can be an used as an input
001	Drive logic 0
010	Drive logic 1
011	reserved value, do not use
100	Output 125MHz from TX PLL
101	Output 25MHz or 125MHz from receive clock recovery PLL. The frequency is specified by CR.RCFREQ. Signal is automatically squelched (driven low) when CR.RCSQL=1 and any of several conditions occur. See section 6.2.1.
110	reserved value, do not use
111	reserved value, do not use

6.2.1 Receive Recovered Clock Squelch Criteria

A 25MHz or 125MHz clock from the receive clock recovery PLL can be output on any of GPO2, GPIO2 and GPIO4-7. When CR.RCSQL=1, this clock is squelched (driven low) when any of the following conditions occur:

- IR.ALOS=1 (analog loss-of-signal occurred)
- IR.RLOS=1 (CDR loss-of-signal occurred))
- IR.RLOL=1 (CDR PLL loss-of-lock occurred)
- IR.LINK_ST=0 (auto-negotiation link down occurred, latched low)

Since each of these criteria is a latched status bit, the output clock signal remains squelched until all of these latched status bits go inactive (as described in section 7.2).

6.3 Reset and Processor Interrupt

6.3.1 Reset

The following reset functions are available in the device:

1. Hardware reset pin (RST_N): This pin asynchronously resets all logic, state machines and registers in the device except the JTAG logic. When the RST_N pin is low, all internal registers are reset to their default values. Pin states are sampled and used to set the default values of several register fields as described in section 6.1. RST_N should be asserted for at least 100µs.

2. Global reset bit, GPIOCR1.RST: Setting this bit is equivalent to asserting the RST_N pin. This bit is self-clearing.

3. Datapath reset bit, BMCR.DP_RST. This bit resets the entire datapath from parallel MII interface through PCS encoder and decoder. It also resets the deserializer. It does not reset any registers, GPIO logic, or the TX PLL. The DP_RST bit is self-clearing.

4. JTAG reset pin JTRST_N. This pin resets the JTAG logic. See section 7.2.18 for details about JTAG operation.

6.3.2 Processor Interrupts

Any of pins GPO1, GPIO1 and GPIO3 can be configured as an active low interrupt output by setting the appropriate field in GPIOCR1 to 011. GPO1 drives high and low while GPIO1 and GPIO3 are open-drain and require pullup resistors.

Status bits than can cause an interrupt are located in the IR register. The corresponding interrupt enable bits are also located in the IR register. The PAGESEL register has a top-level IR status bit to indicate the presence of

active interrupt sources. The PAGESEL register is available on all pages through the MDIO interface, allowing the interrupt routine to read the register without changing the MDIO page.

6.4 MDIO Interface

6.4.1 MDIO Overview

The MAX24287's MDIO interface is compliant to IEEE 802.3 clause 22. MAX24287 always behaves as a PHY on the MDIO bus. Because MAX24287 is not a complete PHY but rather a device that sits between a MAC and a PHY, it implements only a subset of the registers and register fields specified in 802.3 clause 22 as shown in the table below.

MDIO Address	802.3 Name	MAX24287 Name
0	Control	BMCR
1	Status	BMSR
2, 3	PHY Identifier	ID1, ID2
4	Auto-Negotiation Advertisement	AN_ADV
5	Auto-Negotiation Link Partner Base Page Ability	AN_RX
6	Auto-Negotiation Expansion	AN_EXP
15	Extended Status	EXT_STAT

The MDIO consists of a bidirectional, half-duplex serial data signal (MDIO) and a ≤12.5MHz clock signal (MDC) driven by a bus master, usually a MAC. The format of management frames transmitted over the MDIO interface is shown below (see IEEE 802.3 clause 22.2.4.5 for more information). MDIO DC electrical characteristics are listed in section 9.2.1. AC electrical characteristics are listed in section 9.3.6. The MAX24287's MDIO slave state machine is shown in Figure 6-1.

	Management Frame Fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ Command	32 ‘1’s	01	10	AAAAA	RRRRR	Z0	16-bit	Z
WRITE Command	32 ‘1’s	01	01	AAAAA	RRRRR	10	16-bit	Z

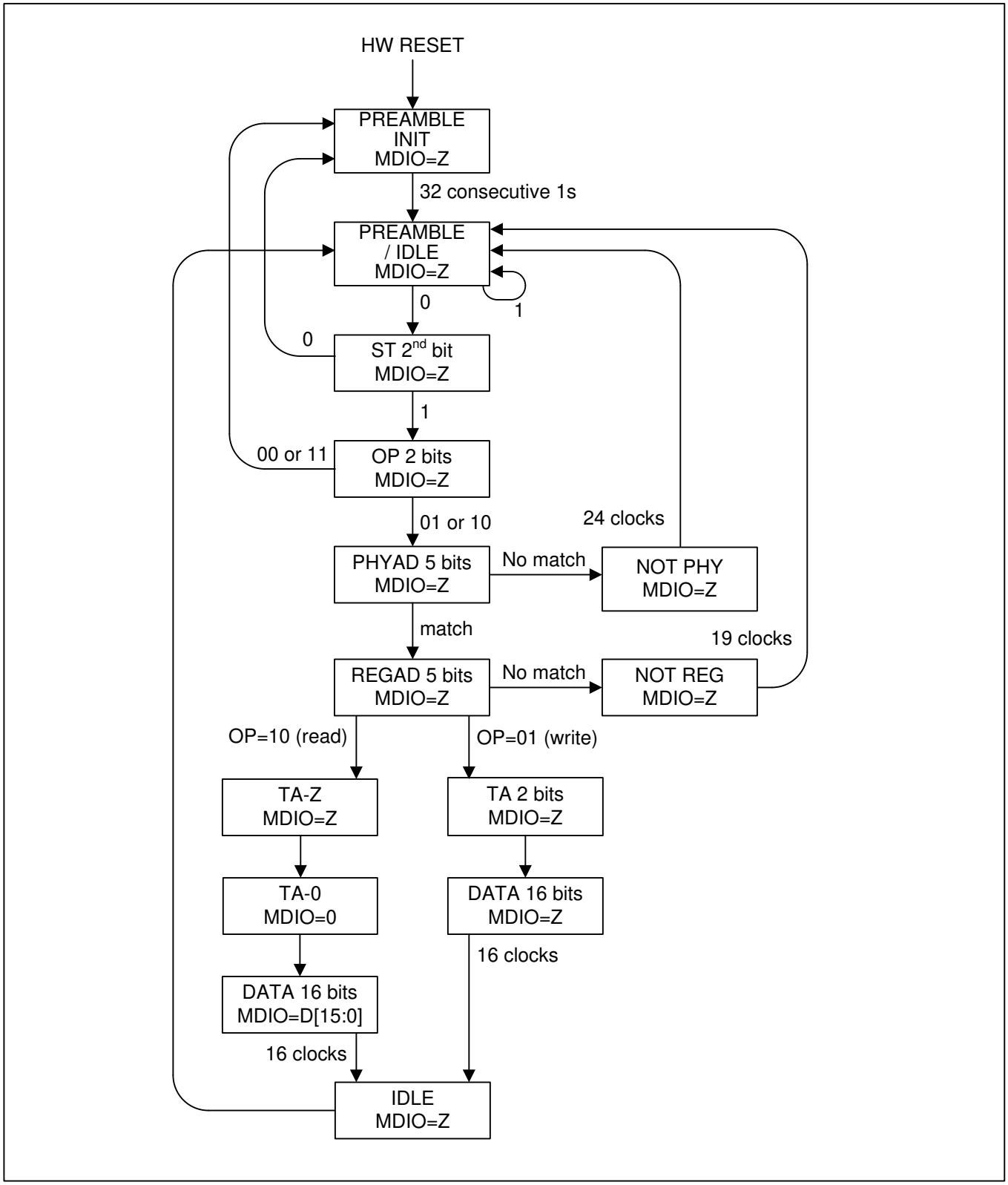
The transmission and reception bit order is MSB first for the PHYAD, REGAD and DATA fields

MAX24287 supports preamble suppression. This allows quicker bursts of read and write transfers to occur by shortening the minimum transfer cycle time from 65 clock periods to 33 clock periods. There must be at least a 32-bit preamble on the first transfer after reset, but on subsequent transfers the preamble can be suppressed or shortened. When the preamble is completely suppressed the 0 in the ST symbol follows the single IDLE Z, which is one clock period duration.

Like any MDIO slave, MAX24287 only performs the read or write operation specified if the PHYAD bits of the MDIO command match the device PHY address. The device PHY address is latched during device reset from the RXD[7:4] and RX_ER pins. See section 6.1.

The MAX24287 does not support the 802.3 clause 45 MDIO extensions. Management frames with ST bits other than 01 or OP bits other than 01 or 10 are ignored and put the device in a state where it ignores the MDIO traffic until it sees a full preamble (32 ones). If Clause 45 ICs and the MAX24287 are connected to the same MDIO management interface, the station management entity must put a full preamble on the bus after communicating with clause 45 ICs before communicating with the MAX24287.

Figure 6-1. MDIO Slave State Machine

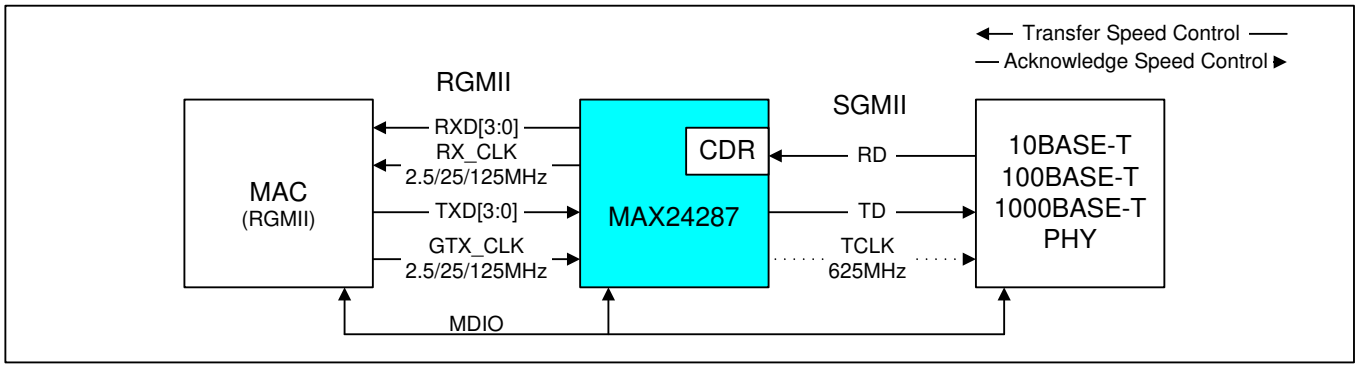


6.4.2 Examples of MAX24287 and PHY Management Using MDIO

The MDIO interface is typically provided by the MAC function within a neighboring processor, ASIC or FPGA component. It can be used to configure the registers in the MAX24287 and/or the registers in a PHY or switch chip connected to the MAX24287 via the SGMII interface.

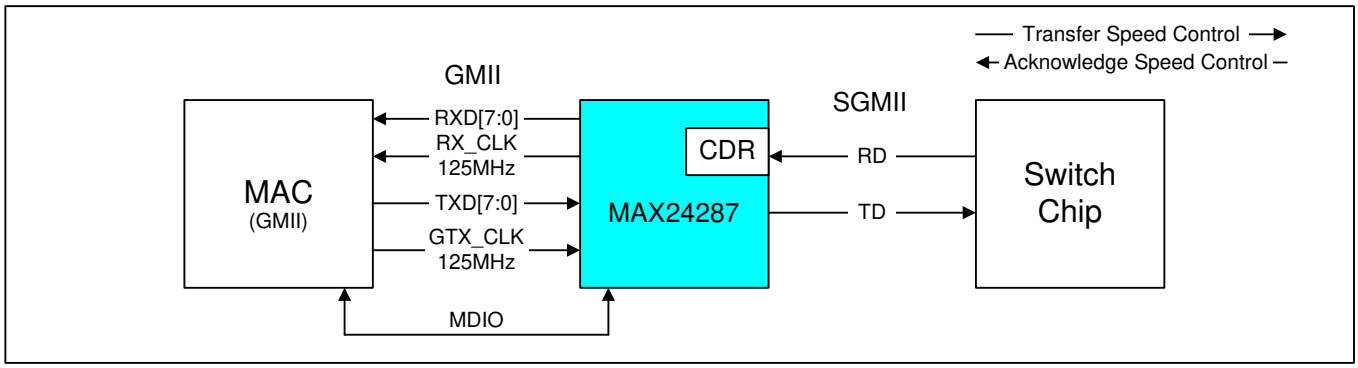
Case 1 in Figure 6-2 shows a typical application where the MAX24287 connects a MAC with a 3-speed RGMII interface to a 3-speed PHY with an SGMII interface. Through the MDIO interface, system software configures the MAX24287 and optionally the PHY. (The PHY may not need to be configured if it is operating in a hardware-only auto-negotiation 1000BASE-T mode). After initial configuration and after the PHY auto-negotiates link details with its 1000BASE-T link partner, the speed and mode are transferred to the MAX24287 over the SGMII interface as specified in the SGMII specification and are available in the MAX24287 AN_RX register. The processor reads this information and configures the MAC and the MAX24287 to match the mode the PHY is in.

Figure 6-2. Management Information Flow Options, Case 1,Tri-Mode PHY



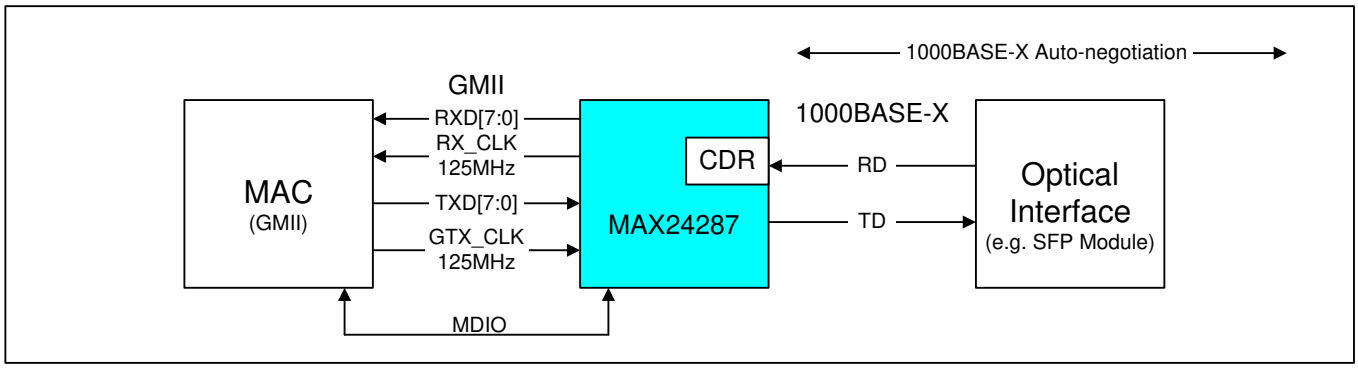
Case 2 in Figure 6-3 shows a typical application where the MAX24287 connects a MAC with a GMII interface to an SGMII switch chip. Through the MDIO interface, system software configures the MAX24287 to match the MAC mode and writes the MAX24287's AN_ADV register to also match the MAC mode. The MAX24287 then transfers the speed and mode over the SGMII interface as specified in the SGMII specification. The switch chip receives this information and configures its port to match.

Figure 6-3. Management Information Flow Options, Case 2, SGMII Switch Chip



Case 3 in Figure 6-4 shows a typical application where the MAX24287 connects a MAC with a GMII interface to an optical interface. In this case the MAX24287 provides the 1000BASE-X PCS and PMA functions for the optical interface. Through the MDIO interface, system software configures the MAX24287 to match the MAC mode, both of which need to be 1000 Mbps speed. The MAX24287 then auto-negotiates with its link partner. This 1000BASE-X auto-negotiation is primarily to establish the pause functionality of the link. The MAX24287's auto-negotiation support is described in section 6.7.

Figure 6-4. Management Information Flow Options, Case 3, 1000BASE-X Interface



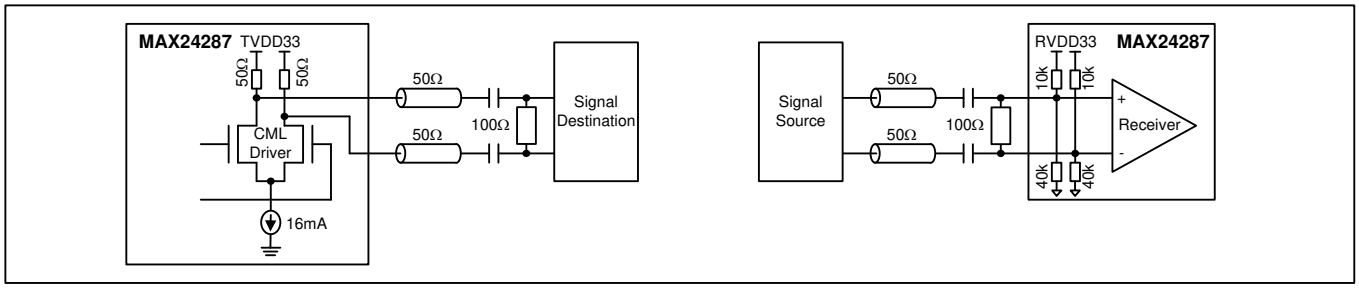
6.5 Serial Interface – 1000BASE-X or SGMII

The high-speed serial interface is compatible with the specification of the 1000BASE-CX PMD service interface TP1 as defined in 802.3 clause 39. It is also compatible with the specification of the SGMII interface and can connect to optical PMD modules in 1000BASE-SX/LX interfaces.

On this interface the MAX24287 transmits a 1250Mbaud differential signal on the TDP/TDN output pins. DDR clocking is used, and the transmit interface outputs a 625MHz differential clock signal on the TCLKP/TCLKN output pins. In the receive direction the clock and data recovery (CDR) block recovers both clock and data from the incoming 1250Mbaud signal on RDP/RDN. A separate receive clock signal is not needed.

Signal Format, Coupling, Termination. The serial interface passes data at 1.25 Gbaud using a CML differential output and an any-format differential input. The CML TDP/TDN outputs have internal 50Ω pullup resistors to TVDD33. The differential input RDP/RDN does not have internal termination, and an external 100Ω termination resistor between RDP and RDN is recommended. The high-speed serial interface pins are typically connected with neighboring components using AC coupling as shown in Figure 6-5.

Figure 6-5. Recommended External Components for High-Speed Serial Interface



Receive Loss-of-Signal. The device's receiver logic has an ALOS input pin through which analog loss-of-signal (ALOS) can be received from a neighboring optical transceiver module, if the high-speed serial signal is transmitted/received optically. The IR.ALOS bit is set when the ALOS pin goes high. ALOS can cause an interrupt if enabled by IR.ALOS_IE.

In addition, the clock-and-data recovery block (CDR) indicates loss-of-signal when it does not detect any transitions in 24 bit times. The IR.RLOS latched status bit is set when the CDR indicates loss-of-signal. RLOS can cause an interrupt if enabled by IR.RLOS_IE.

Receive Loss-of-Lock. The receive clock PLL in the CDR locks to the recovered clock from the RDP/RDN pins and produces several receive-side clock signals. If the receive clock PLL loses lock, it sets IR.RLOL, which can cause an interrupt if enabled by IR.RLOL_IE.

Transmit Clock. The TCLKP/TCLKN differential output can be enabled and disabled using CR.TCLK_EN. Disabled means the output drivers for TCLKP and TCLKN are disabled (high impedance) and the internal 50Ω termination resistors pull both TCLKP and TCLKN up to 3.3V.

DC Electrical Characteristics. See section 9.2.2.

AC Electrical Characteristics. See section 9.3.3.

6.6 Parallel Interface – GMII, RGMII, TBI, RTBI, MII

The parallel interface can be configured as GMII, MII or TBI compliant to IEEE 802.3 clauses 35, 22 and 36, respectively. It can also be configured as reduced pin count RGMII or RTBI compliant to the HP document RGMII Version 1.3 12/10/2000. A summary of the parallel interface modes is show in Table 6-7 below.

Table 6-7. Parallel Interface Modes

Mode	Baud Rate, Mbps	Data Transfer Per Cycle, # of Wires Per Direction	Transmit Clock	Receive Clock	Full Duplex	Half Duplex
TBI, normal	1250	10-bit codes, 10 wires	Input, 125MHz	Output, 2 62.5MHz	Yes	No
TBI, 1 Rx clock	1250	10-bit codes, 10 wires	Input, 125MHz	Output, 1 125MHz	Yes	No
RTBI	1250	10-bit codes, 5 wires, DDR	Input, 125MHz	Output, 125MHz	Yes	No
GMII	1000	8-bit data, 8 wires	Input, 125MHz	Output, 125MHz	Yes	No
RGMII-1000	1000	8-bit data, 4 wires, DDR	Input, 125MHz	Output, 125MHz	Yes	No
RGMII-100	100	4-bit data, 4 wires	Input, 25MHz	Output 25MHz	Yes	Yes
RGMII-10	10	4-bit data, 4 wires	Input, 2.5MHz	Output, 2.5MHz	Yes	Yes
MII-100 DCE	100	4-bit data, 4 wires	Output, 25MHz	Output, 25MHz	Yes	Yes
MII-10 DCE	10	4-bit data, 4 wires	Output, 2.5MHz	Output, 2.5MHz	Yes	Yes
MII-100 DTE	100	4-bit data, 4 wires	Input, 25MHz	Input, 25MHz	Yes	Yes
MII-10 DTE	10	4-bit data, 4 wires	Input ,2.5MHz	Input, 2.5MHz	Yes	Yes

The parallel interface mode is controlled by GMIICR.SPD[1:0]. TBI and MII options are specified by GMIICR.TBI_RATE and GMIICR.DTE_DCE, respectively.

6.6.1 GMII Mode

The MAX24287's GMII interface is compliant to IEEE 802.3 clause 35 but only operates full duplex. Half duplex operation is not supported, and the TX_ER pin is ignored. The PHY therefore does not receive the following from the MAC: carrier extend, carrier extend error, and transmit error propagation as described in 802.3 section 35.2.1.6, section 35.2.2.5 and Table 35-1. These features are not needed for full duplex operation.

The parallel interface can be configured for GMII mode using software configuration or pin configuration at reset. For pin configuration (see section 6.1) one of the following combinations of pin states must be present during device reset:

- COL=0, RXD[1:0]=10, CRS=0
- COL=1, CRS=0

For software configuration, the following register fields must be set: GMIICR.SPD[1:0]=10 and GMIICR.DDR=0.

See IEEE 802.3 clause 35 for functional timing diagrams. GMII DC electrical characteristics are listed in section 9.2.1. AC electrical characteristics are listed in section 9.3.4 and 9.3.5.

Table 6-8. GMII Parallel Bus Pin Naming

Pin Name	802.3 Pin Name	Function
RXCLK	RX_CLK	Receive 125MHz clock output
RXD[7:0]	RXD[7:0]	Receive data output
RX_DV	RX_DV	Receive data valid output
RX_ER	RX_ER	Receive data error output
CRS	CRS	Receive carrier sense
COL	COL	Receive collision (held low in GMII mode)
TXCLK	---	Outputs 125MHz from the TX PLL for MAC when GMIICR.TXCLK_EN=1.
GTXCLK	GTX_CLK	Transmit 125MHz clock input
TXD[7:0]	TXD[7:0]	Transmit data input
TX_EN	TX_EN	Transmit data enable input
TX_ER	TX_ER	Transmit data error input (not used - ignored)

6.6.2 TBI Mode

6.6.2.1 Configuration

The TBI and RTBI interfaces are used when a neighboring component implements the 802.3 PCS layer and therefore transmits and receives 10-bit 8B/10B-encoded data. The parallel interface can be configured for TBI mode using software configuration or pin configuration at reset. For pin configuration (see section 6.1) device pins must be set as follows during device reset: COL=0, RXD[1:0]=11, CRS=0. For software configuration, the following register fields must be set: GMIICR.SPD[1:0]=11 and GMIICR.DDR=0. When the parallel interface is in TBI mode, the MAX24287 does not perform 8B/10B encoding or decoding or any auto-negotiation functions.

6.6.2.2 Normal TBI with Two 62.5MHz Receive Clocks

The normal TBI interface specified in IEEE 802.3 section 36.3.3 has a 10-bit data bus in each direction, a 125MHz transmit clock (GTXCLK), two 62.5MHz receive clocks (RXCLK and RXCLK1) and a receive COMMA signal. See Table 6-9. In the transmit path the MAX24287 samples tx_code_group[9:0] on rising edges of GTXCLK. In the receive path, RXCLK and RXCLK1 are 180 degrees out of phase from each other (i.e. inverted) and together provide rising edges every 8 ns. The MAX24287 updates the rx_code_group[9:0] and COMMA signals before every RXCLK rising edge and every RXCLK1 rising edge. The neighboring component then samples rx_code_group[9:0] and COMMA every RXCLK rising edge and every RXCLK1 rising edge. The normal TBI interface is selected with pin configuration by setting RX_DV=1 during device reset or in software by setting GMIICR:TBI_RATE=1. See IEEE 802.3 section 36.3.3 for functional timing diagrams. TBI DC electrical characteristics are listed in section 9.2.1. AC electrical characteristics are listed in section 9.3.4 and 9.3.5.

Table 6-9. TBI Parallel Bus Pin Naming (Normal Mode}

Pin Name	802.3 Pin Name	Function
RXCLK	PMA_RX_CLK0	Receive 62.5MHz clock output phase 0, odd numbered code-groups
RXD[7:0]	rx_code_group[7:0]	Receive data bits 7 to 0 output
RX_DV	rx_code_group[8]	Receive data bit 8 output
RX_ER	rx_code_group[9]	Receive data bit 9 output
CRS	COM_DET	Comma detection output
COL	---	Not used
TXCLK/RXCLK1	PMA_RX_CLK1	Receive 62.5MHz clock output phase 1, even numbered code-groups
GTXCLK	PMA_TX_CLK	Transmit 125MHz clock input
TXD[7:0]	tx_code_group[7:0]	Transmit data bits 7 to 0 input
TX_EN	tx_code_group[8]	Transmit data bit 8 input
TX_ER	tx_code_group[9]	Transmit data bit 9 input

6.6.2.3 One-Clock TBI Mode

An alternate TBI receive clocking scheme is also available in which the two 62.5MHz receive clocks are replaced by a single 125MHz receive clock on the RXCLK pin. See Table 6-10. In this mode a neighboring component uses rising edges of the RXCLK signal to sample rx_code_group[9:0]. The alternate TBI receive clocking scheme is selected with pin configuration by setting RX_DV=0 during device reset or in software by setting GMIICR:TBI_RATE=0.

Table 6-10. TBI Parallel Bus Pin Naming (One-Clock Mode)

Pin Name	802.3 Pin Name	Function
RXCLK	---	Receive 125MHz clock output
RXD[7:0]	rx_code_group[7:0]	Receive data bits 7 to 0 output
RX_DV	rx_code_group[8]	Receive data bit 8 output
RX_ER	rx_code_group[9]	Receive data bit 9 output
CRS	COM_DET	Comma detection output
COL	---	Not used
TXCLK	---	Outputs 125MHz from the TX PLL for use by the MAC when GMIICR.TXCLK_EN=1.

Pin Name	802.3 Pin Name	Function
GTXCLK	PMA_TX_CLK	Transmit 125MHz clock input
TXD[7:0]	tx_code_group[7:0]	Transmit data bits 7 to 0 input
TX_EN	tx_code_group[8]	Transmit data bit 8 input
TX_ER	tx_code_group[9]	Transmit data bit 9 input

6.6.2.4 Frequency-Locked Through Clocking, No Buffers

The REFCLK signal is internally multiplied to produce the 1250MHz clock used to transmit data on the serial interface TDP/TDN pins. This 1250MHz clock is also used to create the 625MHz clock on the serial interface TCLKP/TCLKN pins. The REFCLK signal must therefore be ±100ppm and low jitter (<5ps rms measured using a 12kHz to 2MHz bandpass filter). The RXCLK and RXCLK1 signals (normal TBI mode) or only the RXCLK signal (one-clock TBI mode) are divided down from the 1250MHz clock recovered from the serial data stream on the RDP/RDN pins.

For proper operation in TBI mode, the signal on the GTXCLK pin must be frequency locked to the signal on the REFCLK pin. One easy way to achieve this is to configure the MAX24287 to output on a GPIO pin a 125MHz signal from the TX PLL (which is locked to the signal on the REFCLK pin). See section 6.2. This 125MHz signal is then wired to a clock input on the neighboring MAC/PCS component. The neighboring component then uses that signal as GTXCLK.

6.6.2.5 Comma Detection and Code-Group Alignment

In the receive path, if PCSCR.EN_CDET=1 then code-group alignment is performed based on comma detection. When a comma+ pattern (0011111xxx) or a comma– (1100000xxx) occurs in the serial bit stream in a K28.1 or K28.5 code-group, three things happen: (1) the code-group containing the comma is output on rx_code_group[9:0] with the alignment shown in 802.3 Figure 36-3, (2) the COMMA pin is driven high, and (3) the PMA_RX clocks are stretched as needed so that both rx_code_group[9:0] and COMMA are setup to be sampled by the neighboring component on the rising edge of RXCLK1 (normal TBI mode) or RXCLK (one-clock TBI mode). Commas in K28.7 code-groups are ignored.

When PCSCR.EN_CDET=0, the receive path does not perform any comma detection or code-group alignment, and the COMMA signal is held low.

6.6.2.6 TBI Control Pins

The MAX24287 TBI interface does not have the TBI EN_CDET pin mentioned in 802.3 section 36.3.3. Comma detection is enabled/disabled by the PCSCR.EN_CDET register bit instead.

The MAX24287 TBI interface does not have the EWRAP pin mentioned in 802.3 section 36.3.3. Control for this loopback is handled by the PCSCR.TLB register bit. See section 6.10.

The MAX24287 TBI interface also does not have the –LCK_REF pin because such a control is not needed by the receive clock and data recovery block.

6.6.3 RGMII Mode

The RGMII interface has three modes of operation to support three Ethernet speeds: 10, 100 and 1000Mbps. This document refers to these three modes as RGMII-1000 for 1000Mbps operation, RGMII-100 for 100Mbps operation and RGMII-10 for 10Mbps operation. RGMII is specified to support speed changes among the three rates as needed. The RGMII specification document can be downloaded from http://www.hp.com/rnd/pdfs/RGMIIv1_3.pdf or can be found by a web search for "RGMII 1.3". This document also specifies the RTBI interface discussed in section 6.6.4.

The parallel interface can be configured for RGMII modes using software configuration or pin configuration at reset. For pin configuration (see section 6.1) one of the following combinations of pin states must be present during device reset:

- COL=0, RXD[1:0]=xx, CRS=1 (xx=00 for RGMII-10, xx=01 for RGMII-100, xx=10 for RGMII-1000)
- COL=1, CRS=1 (RGMII-1000 only)

For software configuration, the following register fields must be set: GMIICR.SPD[1:0]=xx and GMIICR.DDR=1 (where xx values are the same as shown above for RXD[1:0]).

On the receive RGMII interface the MAX24287 does not report in-band status for link state, clock speed and duplex during normal inter-frame. This status indication is defined as optional in the RGMII specification.

Table 6-11. RGMII Parallel Bus Pin Naming

Pin Name	RGMII Pin Name	Function
RXCLK	RXC	Receive 125MHz clock output
RXD[3:0]	RD[3:0]	Receive data bits 3 to 0 and 7 to 4 output
RX_DV	RX_CTL	Receive data valid output
RX_ER	---	Not used
CRS	---	Outputs carrier sense signal
COL	---	Outputs collision signal
TXCLK	---	Outputs 125MHz from the TX PLL for use by the MAC when GMIICR.TXCLK_EN=1.
GTXCLK	TXC	Transmit 125MHz clock input
TXD[3:0]	TD[3:0]	Transmit data bits 3 to 0 and 7 to 4 input
TX_EN	TX_CTL	Transmit data enable input
TX_ER	---	Not used

6.6.3.1 RGMII-1000 Mode

RGMII-1000 is a reduced pin count alternative to the GMII interface. Pin count is reduced by sampling and updating data and control signals on both clock edges. For data, only four data lines are used, as shown in Table 6-11. Data bits 3:0 are latched on the rising edge of the clock, and data bits 7:4 are latched on the falling edge. The transmit control signals TX_EN and TX_ER are multiplexed onto a single TX_CTL signal. TX_EN is latched on the rising edge of the transmit clock TXC while a modified TX_ER signal is latched on the falling edge of TXC. The receive control signals RX_DV and RX_ER are multiplexed onto a single RX_CTL signal. RX_DV is latched on the rising edge of the receive clock RXC while a modified RX_ER signal is latched on the falling edge of RXC.

The modified TX_ER signal = (GMII TX_ER) XOR (GMII TX_EN). The modified RX_ER signal = (GMII_RX_ER) XOR (GMII_RX_DV). These modifications are done to reduce power by eliminating control signal toggling at 125MHz during normal data transmission and during idle.

On the transmit side of the parallel interface the MAX24287 ignores the TX_ER component of the TX_CTL signal, as it does in all 1000Mbps interface modes, since it only operates full-duplex at 1000Mbps. Therefore the 0,1 TX_CTL encoding is interpreted as 0,0 (idle, normal interframe). Similarly, the 1,0 TX_CTL encoding is interpreted as 1,1 (normal data transmission).

See the RGMII v1.3 specification document for functional timing diagrams. DC electrical characteristics are listed in section 9.2.1. AC electrical characteristics are listed in section 9.3.4 and 9.3.5.

6.6.3.2 RGMII-10 and RGMII-100 Modes

The RGMII interface can be used to convey 10 and 100Mbps Ethernet data. The theory of operation at these lower speeds is similar to RGMII-1000 mode as described above but with a 2.5MHz clock for 10Mbps operation, a 25MHz clock for 100Mbps operation, and data latched and updated only on the rising edge of the clock. The RXD[3:0] pins maintain their values during the negative edge of RXCLK. The control signals are conveyed on both clock edges exactly as described for RGMII-1000. See the RGMII v1.3 specification document for functional timing

diagrams. DC electrical characteristics are listed in section 9.2.1. AC characteristics are listed in section 9.3.4 and 9.3.5.

6.6.3.3 Clocks

The RXCLK clock output is 125MHz, 25MHz or 2.5MHz, depending on RGMII mode. It is derived from the recovered clock from the receive serial data.

The GTXCLK clock input must be 125MHz, 25MHz or 2.5MHz ±100 ppm. The GTXCLK clock is not used as the source of the serial data transmit clock.

6.6.4 RTBI Mode

The RGMII v1.3 specification document also specifies a reduced pin-count TBI interface called RTBI. This interface behaves similarly to the RGMII-1000 interface specified in section 6.6.3.1, but conveys 10-bit data and no control information. (TBI control signals such as EWRAP and EN_CDET are handled by control register settings.) The TX_EN (TX_CTL) and RX_DV (RX_CTL) pins behave as additional data pins in this mode, as shown in Table 6-12. Data is sampled and updated on both clock edges as is done in RGMII-1000 mode. On the positive clock edge RXD[3:0] = rx_code_group[3:0], RX_DV = rx_code_group[4], TXD[3:0] = tx_code_group[3:0] and TX_EN = tx_code_group[4]. On the negative clock edge RXD[3:0] = rx_code_group[5:8], RX_DV = rx_code_group[9], TXD[3:0] = tx_code_group[5:8] and TX_EN = tx_code_group[9].

Unlike the normal TBI interface, which has two 62.5MHz receive clocks, RTBI has a single 125MHz clock signal in each direction.

The parallel interface can be configured for RTBI mode using software configuration or pin configuration at reset. For pin configuration (see section 6.1) device pins must be set as follows during device reset: COL=0, RXD[1:0]=11, CRS=1. For software configuration, the following register fields must be set: GMIICR.SPD[1:0]=11 and GMIICR.DDR=1. When the parallel interface is in RTBI mode, the MAX24287 does not perform 8B/10B encoding or decoding or any auto-negotiation functions.

For proper operation in RTBI mode, the signal on the GTXCLK pin must be frequency locked to the signal on the REFCLK pin. One easy way to achieve this is to configure the MAX24287 to output on a GPIO pin a 125MHz signal from the TX PLL (which is locked to the signal on the REFCLK pin). See section 6.2. This 125MHz signal is then wired to a clock input on the neighboring MAC/PCS component. The neighboring component then uses that signal as GTXCLK.

See the RGMII v1.3 specification document for functional timing diagrams. RGMII DC electrical characteristics are listed in section 9.2.1. AC electrical characteristics are listed in section 9.3.4 and 9.3.5.

Table 6-12. RTBI Parallel Bus Pin Naming

Pin Name	Spec Pin Name	Function
RXCLK	RXC	Receive 125MHz clock output
RXD[3:0]	RD[3:0]	Receive data bits 3 to 0 and 8 to 5 output
RX_DV	RX_CTL	Receive data bits 4 and 9 output
RX_ER	---	Not used
CRS	COM_DET	Comma detection output
COL	---	Not used
TXCLK	---	Outputs 125MHz from the TX PLL for use by the MAC when GMIICR.TXCLK_EN=1.
GTXCLK	TXC	Transmit 125MHz clock input
TXD[3:0]	TD[3:0]	Transmit data bits 3 to 0 and 8 to 5 input
TX_EN	TX_CTL	Transmit data bits 4 and 9 input
TX_ER	---	Not used

6.6.5 MII Mode

The MAX24287's MII interface is compliant to IEEE 802.3 clause 22 except that TX_ER is ignored (and therefore the MAX24287 does not receive transmit error propagation from the MAC).

The parallel interface can be configured for MII mode using software configuration or pin configuration at reset. For pin configuration (see section 6.1) device pins must be set as follows during device reset: COL=0, RXD[1:0]=0x, CRS=0 (x=0 for 10Mbps, x=1 for 100Mbps). For software configuration, the following register fields must be set: GMIICR.SPD[1:0]=0x and GMIICR.DDR=0.

Since the MAX24287 can be used in a variety of applications, it can be configured to source the TXCLK and RXCLK as a PHY normally does or to accept TXCLK and RXCLK from a neighboring component. The former case is called DCE mode; the latter is called DTE mode. DTE/DCE selection is controlled by the GMIICR.DTE_DCE register bit.

In DTE mode the MAX24287 is configured for operation on the MAC side of the MII. Both TXCLK and RXCLK are inputs at 2.5MHz (10Mbps MII) or 25MHz (100Mbps MII) ±100 ppm. TXCLK is not used as the serial data transmit clock (which is derived from the REFCLK input instead).

In DCE mode the MAX24287 is configured for operation on the PHY side of the MII. Both TXCLK and RXCLK are outputs at 2.5MHz or 25MHz. The TXCLK output clock is derived from the REFCLK input. The RXCLK output clock is derived from the recovered clock from the receive serial data when a receive signal is present or from REFCLK when no receive signal is present.

See 802.3 clause 22 for functional timing diagrams. MII DC electrical characteristics are listed in section 9.2.1. AC electrical characteristics are listed in section 9.3.4 and 9.3.5.

On the transmit MII interface the MAX24287 requires that the preamble including the SFD must be an even number of nibbles (i.e. number of nibbles divided by 2 is an integer). On the receive MII interface the MAX24287 always outputs an even number of nibbles of preamble.

Table 6-13. MII Parallel Bus Pin Naming

Pin Name	802.3 Pin Name	Function
RXCLK	RX_CLK	Receive 2.5 or 25MHz clock, can be input or output
RXD[3:0]	RXD[3L0]	Receive data nibble output
RX_DV	RX_DV	Receive data valid output
RX_ER	RX_ER	Receive data error output
CRS	CRS	Receive carrier sense
COL	COL	Receive collision
TXCLK	TX_CLK	Transmit 2.5 or 25MHz clock, can be input or output
GTXCLK	---	Not used
TXD[3:0]	TXD[3:0]	Transmit data nibble input
TX_EN	TX_EN	Transmit data enable input
TX_ER	TX_ER	Transmit data error input (not used - ignored)

6.7 Auto-Negotiation (AN)

In the MAX24287 the auto-negotiation mechanism described in IEEE 802.3 Clause 37 is used for auto-negotiation between IEEE 802.3 1000BASE-X link partners as well as the transfer of SGMII PHY status to a neighboring MAC as described in the Cisco Serial-SGMII document ENG-46158. The 802.3 1000BASE-X next page functionality is not supported. The PCSCR.BASEX register bit controls the link timer time-out mode of the auto-negotiation protocol.

The auto-negotiation mechanism between link partners uses a special code set that passes a 16-bit value called tx_Config_Reg[15:0] as defined in IEEE 802.3. The auto-negotiation transfer starts when BMCR.AN_START is set (self clearing) and BMCR.AN_EN is set. The tx_Config_Reg value is continuously sent with the ACK bit (bit 14) clear and the other bits sourced from the AN_ADV register. When the device receives a non-zero rx_Config_Reg value it sets the ACK bit in the tx_Config_Reg, saves the rx_Config_Reg bits to the AN_RX register, and sets the AN_EXP.PAGE and IR.PAGE bits to tell system software that a new page has arrived. The tx_Config_Reg transmission stops when the link timer times out after 10ms in 1000BASE-X mode or after 1.6ms in SGMII mode.

System software must complete the auto-negotiation function by processing the AN_RX register and configuring the hardware appropriately.

The fields of the auto-negotiation registers AN_ADV and AN_RX have different meanings when used in 1000BASE-X or SGMII mode. See section 6.7.1 for 1000BASE-X and section 6.7.2. for SGMII.

By default, an internal watchdog timer monitors the auto-negotiation process. If the link is not up within 5 seconds after auto-negotiation was started, the watchdog timer restarts the auto-negotiation. This watchdog timer can be disabled by setting PCSCR.WD_DIS=1.

6.7.1 1000BASE-X Auto-Negotiation

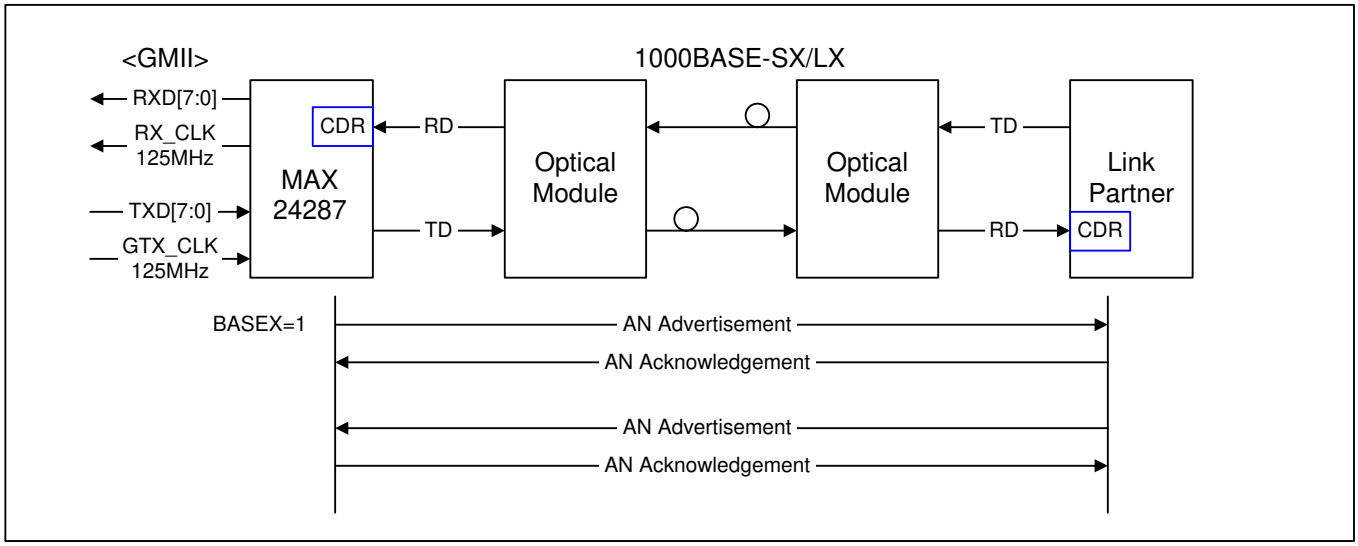
In 1000BASE-X auto-negotiation, two link partners send their specific capabilities to each other. Each link partner compares the capabilities that it advertises in its AN_ADV register against its link partner's advertised abilities, which are stored in the AN_RX register when received. Each link partner uses the same arbitration algorithm specified in IEEE 802.3 clause 37.2 to determine how it should configure its hardware, and, therefore, the two link partners' configurations should match. However, if there is no overlap of capabilities between the link partners, the RF bits (Remote Fault, see Table 6-14) are set to 11, and the auto-negotiation process is started again. An external processor configures the advertised abilities, reads the link partner’s abilities, performs the arbitration algorithm, and sets the RF bits as needed.

The MAX24287 AN block implements the auto-negotiation state machine shown in IEEE 802.3 Figure 37-6. It also generates an internal link-down status signal whenever the AN state machine is in any state other than AN_DISABLE_LINK_OK or LINK_OK. This link-down signal is used to clear the active-low BMSR.LINK_ST bit and is used to squelch output clock signals on GPIO pins when CR.RCSQL=1.

System software can configure the MAX24287 for 1000BASE-X auto-negotiation by setting PCSCR.BASEX=1 and BMCR.AN_EN=1.

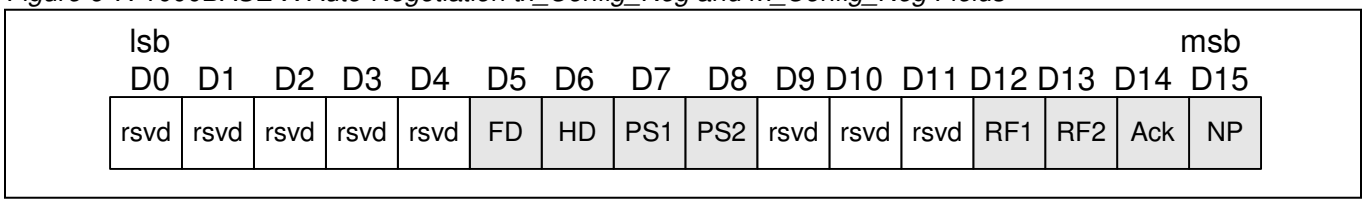
The MAX24287 can also be configured for 1000BASE-X auto-negotiation by pin settings at reset. In 15-pin configuration mode (COL=0 at reset), if RXD[1:0]=10 and GPO2=1 and RX_DV=1 at reset then PCSCR:BASEX is set to 1 to indicate 1000BASE-X mode and BMCR.AN_EN is set to 1 to enable auto-negotiation. In 3-pin configuration (COL=1 at reset), if GPO2=1 then PCSCR:BASEX is set to 1 to indicate 1000BASE-X mode and auto-negotiation is automatically enabled. In both pin configuration modes the AN_ADV register's reset-default value causes device capabilities to be advertised as follows: full-duplex only, no pause support, no remote fault. See section 6.1 for details about pin configuration at reset.

Figure 6-6. Auto-Negotiation with a Link Partner over 1000BASE-X



The tx_Config_Reg and rx_Config_Reg format for 1000BASE-X auto-negotiation is shown in Figure 6-7. All reserved bits are set to 0. The ACK bit is set and detected by the PCS auto-negotiation hardware.

Figure 6-7. 1000BASE-X Auto-Negotiation tx_Config_Reg and rx_Config_Reg Fields



The AN_ADV register is the source of tx_Config_Reg. The received rx_Config_Reg is written to the AN_RX register. The auto-negotiation fields for AN_ADV and AN_RX are described in Table 6-14 and Table 6-15.

Table 6-14. AN_ADV 1000BASE-X Auto-Negotiation Ability Advertisement Register (MDIO 4)

Bit(s)	Name	Description	R/W	Reset
15	NP	Next Page capability is not supported. This bit should always be set to 0.	RW	0
14	Reserved	Ignore on Read	RO	0
13:12	RF	Remote Fault. Used to indicate to the link partner that a remote fault condition has been detected: 00 = No Error, Link OK 01 = Link Failure 10 = Off Line 11 = Auto-Negotiation Error	RW	00
11:9	ZERO1	Always write 000	RW	0
8:7	PS	Pause. Used to indicate pause capabilities to the link partner. 00 = No Pause 01 = Symmetric Pause 10 = Asymmetric Pause 11 = Both Symmetric and Asymmetric Pause	RW	00
6	HD	Used to indicate ability to support half duplex to link partner. Since half duplex is not supported always write 0.	RW	0
5	FD	Used to indicate ability to support full duplex to link partner. 0 = Do not advertise full duplex capability 1 = Advertise full duplex capability	RW	1

Bit(s)	Name	Description	R/W	Reset
4:0	ZERO2	Always write 00000	RW	00000

Table 6-15. AN_RX 1000BASE-X Auto-negotiation Ability Receive Register (MDIO 5)

Bit(s)	Name	Description	R/W	Reset
15	NP	Next Page. Used by link partner to indicate its PCS has a Next Page to exchange. 0 = No Next Page exchange request 1 = Next Page exchange request	RO	0
14	Acknowledge	Indicates link partner successfully received the previously transmitted base page.	RO	0
13:12	RF	Remote Fault. Link partner uses this field to indicate a remote fault condition has been detected. 00 = No Error, Link OK 01 = Link Failure 10 = Off Line 11 = Auto-Negotiation Error	RO	0
11:9	Reserved	Ignore on Read	RO	0
8:7	PS	Pause. Used by link partner to indicate its pause capabilities. 00 = No Pause 01 = Symmetric Pause 10 = Asymmetric Pause 11 = Both Symmetric and Asymmetric Pause	RO	0
6	HD	Used by link partner to indicate ability to support half duplex. 0 = Not able to support half duplex 1 = Able to support half duplex	RO	0
5	FD	Used by link partner to indicate ability to support full duplex. 0 = Not able to support full duplex 1 = Able to support full duplex	RO	0
4:0	Reserved	Ignore on Read	RO	0

6.7.2 SGMII Control Information Transfer

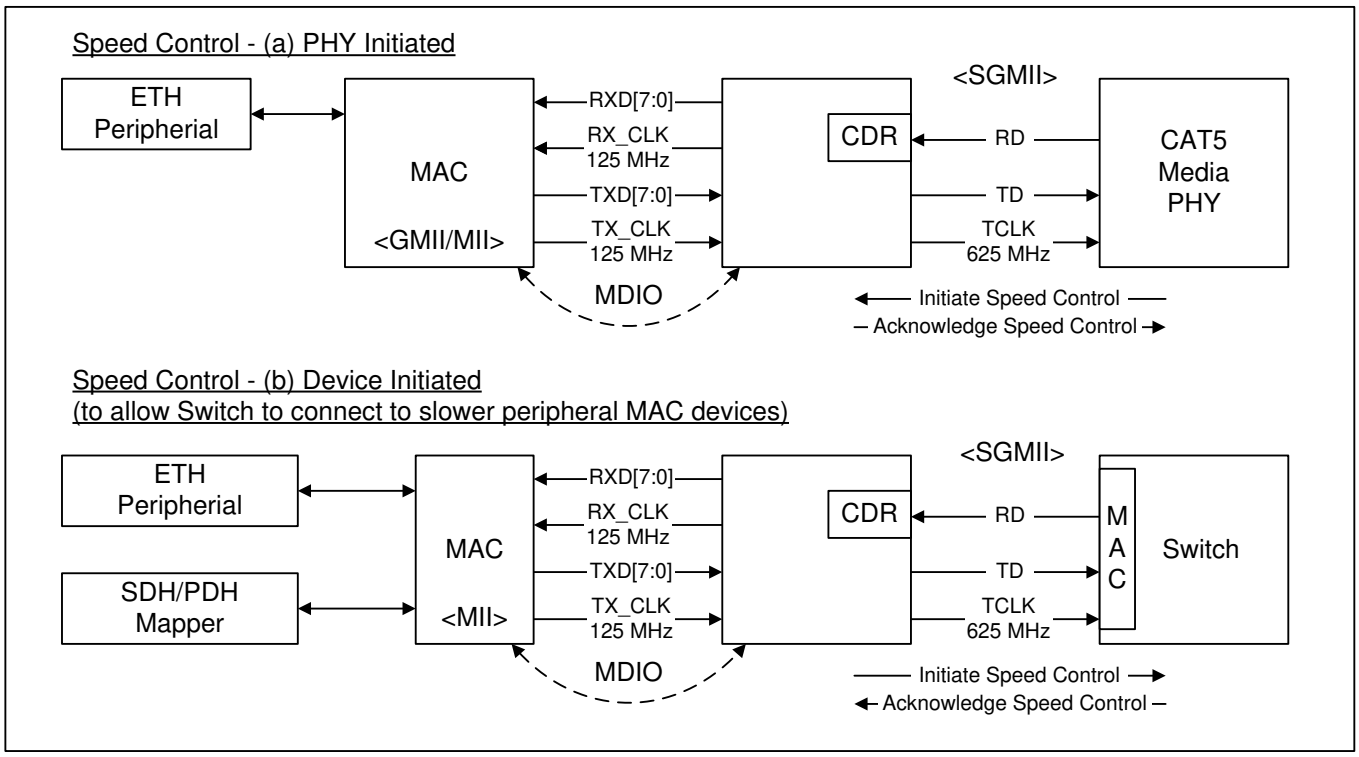
SGMII control information transfer mode is enabled by setting PCSCR.BASEX=0. According the SGMII specification, a PHY sends control information to the neighboring MAC using the same facilities used for 1000BASE-X auto-negotiation (AN_ADV, AN_RX, tx_Config_Reg, rx_Config_Reg, see section 6.7.1). Since the MAX24287 sits between a PHY and a MAC it can behave as the transmitter or receiver in the control information transfer process depending on how it is connected to neighboring components.

When the MAX24287 is connected to a 1000BASE-T PHY, for example, the PHY transfers control information to the MAX24287, which then acknowledges the information transfer. System software then reads the control information from the MAX24287 and configures the MAX24287 to match the PHY. This situation is shown in case (a) of Figure 6-8.

In other scenarios, such as when the MAX24287 is connected by SGMII to a switch IC, shown in case (b) of Figure 6-8, the MAX24287 transfers control information to the neighboring component, which then acknowledges the information transfer. System software then reads the control information from the neighboring component and configures that component to match the MAX24287.

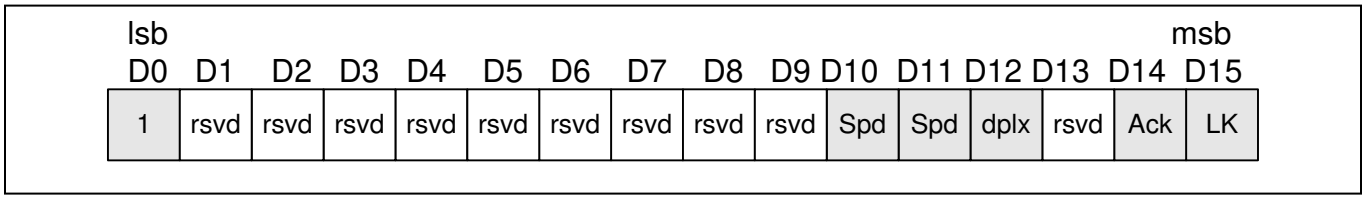
The MAX24287 AN block implements the auto-negotiation state machine shown in IEEE 802.3 Figure 37-6. It also generates an internal link-down status signal whenever the AN state machine is in any state other than AN_DISABLE_LINK_OK or LINK_OK. This link-down signal is used to clear the active-low BMSR.LINK_ST bit and is used to squelch output clock signals on GPIO pins when CR.RCSQL=1.

Figure 6-8. SGMII Control Information Generation, Reception and Acknowledgement



The control information fields carried on the SGMII are: link status (up/down), link speed (1000/100/10Mbps) and duplex mode (full/half). The tx_Config_Reg and rx_Config_Reg format for SGMII control information transfer is shown in Figure 6-9. All reserved bits are set to 0. The ACK bit is set and detected by the PCS hardware.

Figure 6-9. SGMII tx_Config_Reg and rx_Config_Reg Fields



When the MAX24287 is the control information receiver, its AN_ADV register must be set to 0x0001. The received control information is automatically stored in the AN_RX register.

When the MAX24287 is the control information transmitter, the information is sourced from its AN_ADV register.

The MAX24287 can be configured to automatically send SGMII control information by pin settings at reset. In 15-pin configuration mode (COL=0 at reset), if RXD[1:0]=10 and GPO2=0 and RX_DV=1 at reset then PCSCR:BASEX is set to 0 to indicate SGMII mode, BMCR.AN_EN is set to 1 to enable auto-negotiation, and the AN_ADV SPD[1:0] bits are set by the reset values of the RXD[1:0] pins. In 3-pin configuration (COL=1 at reset), if GPO2=0 then PCSCR:BASEX is set to 0 to indicate SGMII mode, auto-negotiation is automatically enabled, and the AN_ADV SPD[1:0] bits are set to 10 (1000Mbps). In both pin configuration modes the AN_ADV register's reset-default value causes device capabilities to be advertised as follows: full-duplex only, link up. See section 6.1 for details about pin configuration at reset.

The AN_ADV register is the source of tx_Config_Reg value. The received rx_Config_Reg value is written to the AN_RX register. These meanings are described in Table 6-16 and Table 6-17.

Table 6-16. AN_ADV SGMII Configuration Information Register (MDIO 4)

Bit(s)	Name	Description	R/W	Reset
15	LK	Link Status. 0 = Link down 1 = Link up	RW	Note 1
14	Reserved	Ignore on Read	RO	0
13	ZERO1	Always write 0	RW	0
12	DPLX	Duplex mode 0 = Half duplex 1 = Full duplex	RW	1
11:10	SPD[1:0]	Link speed 00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved	RW	Note 1
9:1	ZERO2	Always write 000000000	RW	0
0	ONE	Always write 1	RW	1

Note 1: See the AN_ADV register description.

Table 6-17. AN_RX SGMII Configuration Information Receive Register (MDIO 5)

Bit(s)	Name	Description	R/W	Reset
15	LK	Link partner link status. 0 = Link down 1 = Link up	RO	0
14:13	Reserved	Ignore on read	RO	0
12	DPLX	Link partner duplex mode 0 = Half duplex 1 = Full duplex	RO	0
11:10	SPD	Link partner link speed 00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved	RO	0
9:0	Reserved	Ignore on read	RO	0

6.8 Data Paths

The MAX24287 data paths perform bidirectional conversion between a parallel interface (GMII, RGMII, TBI, RTBI or MII) and a 1.25Gbps serial interface (1000BASE-X or SGMII).

In GMII, RGMII and MII modes, the data paths implement the 802.3 PCS and PMA sublayers including auto-negotiation. The parallel interface data is 8 bits wide. The PCS logic performs 8B/10B encoding and decoding. The PMA logic performs 10:1 serialization and deserialization.

In TBI and RTBI modes, the MAX24287's PCS and auto-negotiation blocks are not used, and the data paths implements only the PMA sublayer. The parallel interface data is 10 bits wide, and the PMA logic performs 10:1 serialization and deserialization.

6.8.1 GMII, RGMII and MII Serial to Parallel Conversion and Decoding

Refer to the block diagram in Figure 2-1. Clock and data are recovered from the incoming 1.25Gbps serial signal on RDP/RDN. The serial data is then converted to 10-bit parallel data with 10-bit alignment determined by detecting commas. The 10-bit code groups are then 8B/10B decoded by the PCS decoder as specified in 802.3 clause 36. After passing through a rate adaption buffer that accounts for phase and/or frequency differences between recovered clock and MII clock, the 8-bit data is clocked out of the device to a neighboring MAC either 4 bits or 8 bits at a time. Half duplex is supported in 10 and 100Mbps modes but not in 1000Mbps modes. Carrier extend is not supported in 1000Mbps modes.

6.8.2 GMII, RGMII and MII Parallel to Serial Conversion and Encoding

Refer to the block diagram in Figure 2-1. Parallel data is received from the MAC clocked by a 125MHz, 25MHz or 2.5MHz clock, either 4 bits or 8 bits at a time. The data then passes through a rate adaption buffer that accounts for phase and/or frequency differences between MII clock and transmit clock. The 8-bit data is then 8B/10B encoded by the PCS encoder as specified in 802.3 clause 36. The 10-bit code-groups are then serialized. The resulting 1.25Gbps serial data is transmitted to a neighboring 1000BASE-X optical module or SGMII-interface copper PHY. Half duplex is supported in 10 and 100 Mbps modes but not in 1000 Mbps modes. Carrier extend is not supported in 1000 Mbps modes.

6.8.3 TBI, RTBI Serial to Parallel Conversion and Decoding

In the block diagram in Figure 2-1, the PCS decoder is disabled because 8B/10B decoding is not done by the MAX24287 in these modes. Clock and data are recovered from the incoming 1.25Gbps serial signal. The serial data is then converted to 10-bit parallel data with 10-bit alignment set by detecting commas (PCSCR.EN_CDET=1) or with no 10-bit alignment (EN_CDET=0, simple 10-bit SERDES mode). Data is clocked out of the device to a neighboring component either 5 bits or 10 bits at a time.

6.8.4 TBI Parallel to Serial Conversion and Encoding

In the block diagram in Figure 2-1, the PCS encoder is disabled because 8B/10B encoding is not done by the MAX24287 in these modes. Parallel data is received from the MAC clocked by a 125MHz clock, either 5 bits or 10 bits at a time. The 10-bit code-groups are then serialized. The resulting 1.25Gbps serial data is transmitted to a neighboring 1000BASE-X optical module or SGMII-interface copper PHY.

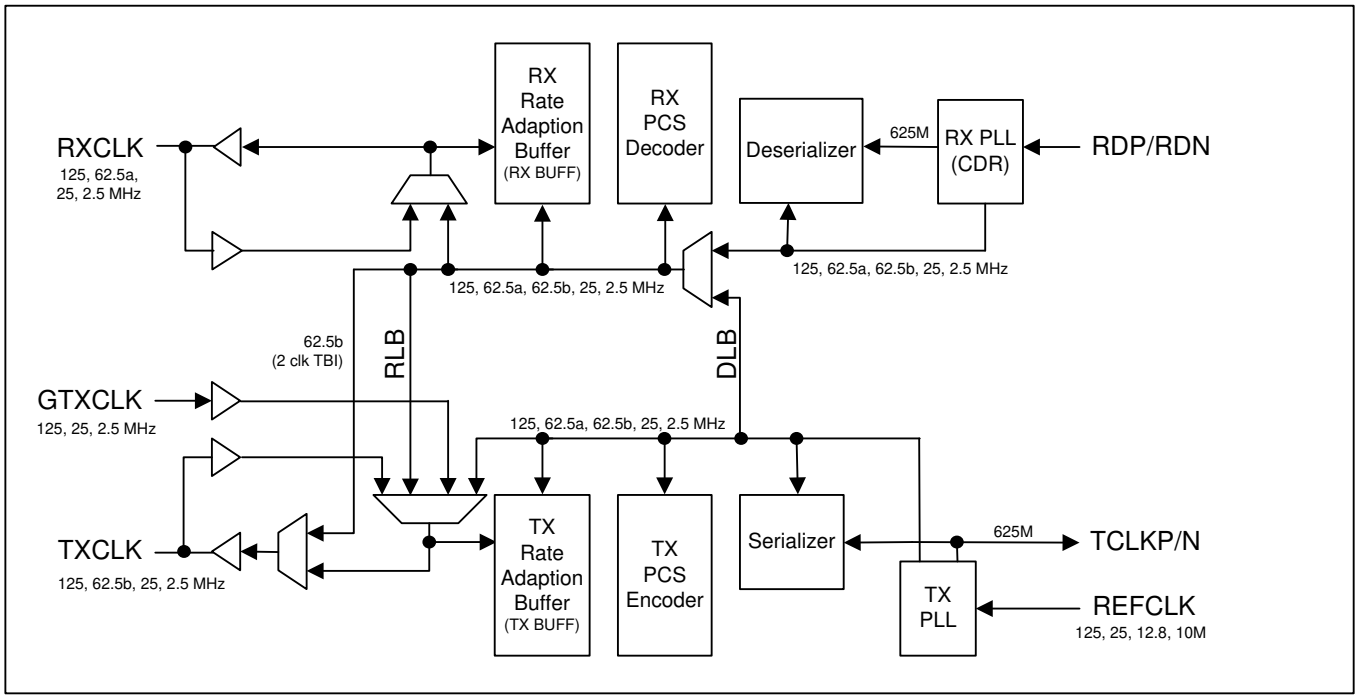
6.8.5 Rate Adaption Buffers, Jumbo Packets and Clock Frequency Differences

The MAX24287 can handle jumbo packets up to 9001 bytes long as long as the clock frequencies of each rate adaption buffer’s write clock and the read clock are both within ±100ppm of nominal.

For example, in GMII mode the transmit rate adaption buffer is written by GTXCLK and read by a 125MHz clock frequency locked to the REFCLK signal. If GTXCLK and REFCLK are both maintained within ±100ppm of nominal frequency then jumbo packets up to 9001 bytes long can be accommodated by the transmit rate adaption buffer.

6.9 Timing Paths

Figure 6-10. Timing Path Diagram



Numbers in the tables below are clock frequencies in MHz.

Table 6-18. Timing Path Muxes – No Loopback

Mode	TX Rate Buffer Mux	TXCLK Mux/Driver	RX PCS Mux	RX Rate Buffer Mux	RXCLK Driver
GMII	GTXCLK 125	--	RX PLL 62.5	RX PLL 125	RX PLL 125
RGMII 1000	GTXCLK 125	--	RX PLL 62.5	RX PLL 125	RX PLL 125
RGMII 100	GTXCLK 25	--	RX PLL 62.5	RX PLL 25	RX PLL 25
RGMII 10	GTXCLK 2.5	--	RX PLL 62.5	RX PLL 2.5	RX PLL 2.5
MII 100 - DCE	TX PLL 25	TX PLL 25	RX PLL 62.5	RX PLL 25	RX PLL 25
MII 100 - DTE	TXCLK 25	---	RX PLL 62.5	RXCLK 25	---
MII 10 - DCE	TX PLL 2.5	TX PLL 2.5	RX PLL 62.5	RX PLL 2.5	RX PLL 2.5
MII 10 - DTE	TXCLK 2.5	--	RX PLL 62.5	RXCLK 2.5	---
TBI half rate	GTXCLK 125	RX PLL 62.5b	RX PLL 62.5	RX PLL 62.5a	RX PLL 62.5a
TBI full rate	GTXCLK 125	--	RX PLL 62.5	RX PLL 125	RX PLL 125
RTBI	GTXCLK 125	--	RX PLL 62.5	RX PLL 125	RX PLL 125

Table 6-19. Timing Path Muxes – DLB Loopback

Mode	TX Rate Buffer Mux	TXCLK Mux/Driver	RX PCS Mux	RX Rate Buffer Mux	RXCLK Driver
GMII	GTXCLK 125	--	TX PLL 62.5	TX PLL 125	TX PLL 125
RGMII 1000	GTXCLK 125	--	TX PLL 62.5	TX PLL 125	TX PLL 125
RGMII 100	GTXCLK 25	--	TX PLL 62.5	TX PLL 25	TX PLL 25
RGMII 10	GTXCLK 2.5	--	TX PLL 62.5	TX PLL 2.5	TX PLL 2.5
MII 100 - DCE	TX PLL 25	TX PLL 25	TX PLL 62.5	TX PLL 25	TX PLL 25
MII 100 - DTE	TXCLK 25	---	TX PLL 62.5	TXCLK 25	---

Mode	TX Rate Buffer Mux	TXCLK Mux/Driver	RX PCS Mux	RX Rate Buffer Mux	RXCLK Driver
MII 10 - DCE	TX PLL 2.5	TX PLL 2.5	TX PLL 62.5	TX PLL 2.5	TX PLL 2.5
MII 10 - DTE	TXCLK 2.5	---	TX PLL 62.5	TXCLK 2.5	---
TBI half rate	GTXCLK 125	TX PLL 62.5b	TX PLL 62.5	TX PLL 62.5a	TX PLL 62.5a
TBI full rate	GTXCLK 125	--	TX PLL 62.5	TX PLL 125	TX PLL 125
RTBI	GTXCLK 125	--	TX PLL 62.5	TX PLL 125	TX PLL 125

Table 6-20. Timing Path Muxes – RLB Loopback

Mode	TX Rate Buffer Mux	TXCLK Mux/Driver	RX PCS Mux	RX Rate Buffer Mux	RXCLK Driver
GMII	RX PLL 125	--	RX PLL 62.5	RX PLL 125	RX PLL 125
RGMII 1000	RX PLL 125	--	RX PLL 62.5	RX PLL 125	RX PLL 125
RGMII 100	RX PLL 25	--	RX PLL 62.5	RX PLL 25	RX PLL 25
RGMII 10	RX PLL 2.5	--	RX PLL 62.5	RX PLL 2.5	RX PLL 2.5
MII 100 - DCE	RX PLL 25	TX PLL 25	RX PLL 62.5	RX PLL 25	RX PLL 25
MII 100 - DTE	RXCLK 25	---	RX PLL 62.5	RXCLK 25	---
MII 10 - DCE	RX PLL 2.5	TX PLL 2.5	RX PLL 62.5	RX PLL 2.5	RX PLL 2.5
MII 10 - DTE	RXCLK 2.5	--	RX PLL 62.5	RXCLK 2.5	--

6.9.1 RX PLL

The RX PLL is used to recover the clock from the RDP/RDN high-speed serial input signal. It generates 625MHz for the de-serializer and 125MHz, 62.5MHz, 25MHz and 2.5MHz for the receive-side PCS decoder, rate adaption buffer and parallel port logic. It also generates a loss of lock (RLOL) signal for the IR.RLOL latched status bit.

6.9.2 TX PLL

The TX PLL generates a low-jitter 625MHz clock signal for the serializer and the TCLKP/TCLKN differential output. This clock signal meets the jitter requirements of IEEE802.3. It also generates 125MHz, 62.5MHz, 25MHz and 2.5MHz for the transmit-side PCS decoder, rate adaption buffer and parallel port logic.

The TX PLL locks to the REFCLK signal, which can be 125MHz, 25MHz, 12.8MHz or 10MHz as specified by the RXD[3:2] pins during device reset. The 12.8MHz and 10MHz frequencies enable the device to share an oscillator with any clock synchronization ICs that may be on the same board.

6.9.3 Input Jitter Tolerance

The input jitter tolerance is specified at the receive serial input RDP/RDN. The MAX24287 CDR block accepts data with maximum total jitter up to 0.75 UI (or 600 ps) peak-to-peak as required by 802.3 Table 38-10 and as shown in Table 9-8. Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at RDP/RDN.

6.9.4 Output Jitter Generation

The output jitter generation limit is specified at the transmit serial output (TDP/TDN) of the serializer. According to Table 38-10 of IEEE 802.3, the maximum total jitter generated must be less than 0.24 UI (192 ps) peak-to-peak and the deterministic jitter should be less than 0.10 UI (80 ps) peak-to-peak. MAX24287 typical and maximum jitter generation specifications are shown in Table 9-10. Actual output jitter performance is a function of REFCLK signal jitter. Contact the factory for a tool to calculate output jitter from REFCLK phase noise.

6.9.5 TX PLL Jitter Transfer

The TX PLL has a bandwidth of approximately 200kHz and jitter transfer peaking of 0.1dB or less.

6.9.6 GPIO Pins as Clock Outputs

Reference Clock. A 125MHz clock from the TX PLL (locked to the REFCLK signal) can be output on one or more GPIO pins. See section 6.2 for configuration details. One use for this 125MHz output is to provide a 125MHz transmit clock to a MAC block on a neighboring component. The MAC then uses this signal to clock its transmit parallel MII pins.

Recovered Clock. A 25MHz or 125MHz clock signal from the receive clock and data recovery PLL can be output on one or more GPIO pins. This clock signal is typically used in synchronous Ethernet applications to send recovered Ethernet line timing to the system's central timing function. See section 6.2 for configuration details.

These output clock signals do not glitch during internal switching between frequencies or sources or when being squelched and unsquelched.

6.10 Loopbacks

Three loopbacks are available in the MAX24287. The loopback data paths are shown in the block diagram in Figure 2-1. The clocking paths are shown in section 6.9.

6.10.1 Diagnostic Loopback

Diagnostic loopback is enabled by setting BMCR.DLB=1. When the parallel interface is GMII, RGMII or MII, the PCS decoder in the receive path takes 10-bit codes from the PCS encoder in the transmit path rather than from the deserializer. In these modes the rate adaption buffers are in the path, and therefore the receive clock can be different than the transmit clock.

When the parallel interface is TBI or RTBI, 10-bit codes from the transmit side of the parallel interface are looped back to the receive side of the parallel interface. In these modes the PCS encoder and decoder blocks perform a simple pass-through function of 10-bit codes. The single 125MHz receive clock or dual 62.5MHz receive clocks are derived from the signal on the GTXCLK pin.

During diagnostic loopback, if CR.DLBDO=0 the TDP/TDN output driver is placed in a high-impedance state and the TDP/TDN pins are both pulled up to 3.3V by their internal 50Ω termination resistors. The TCLKP/TCLKN output continues to toggle if enabled. If CR.DLBDO=1 then data is transmitted on TDP/TDN during diagnostic loopback while also being looped back to the receiver.

During diagnostic loopback, the COL signal remains deasserted at all times, unless BMCR.COL_TEST is set, in which case the COL signal behaves as described in 802.3 section 22.2.4.1.9.

6.10.2 Terminal Loopback

Terminal loopback is enabled by setting PCSCR.TLB=1. When this loopback is enabled, the receive CDR takes serial data from the transmit driver rather than from the RDP/RDN pins. This loopback implements the EWRAP function specified in 802.3 section 36.3.3 for the TBI interface.

During terminal loopback, if CR.TLBDO=0 the TDP/TDN output driver is placed in a high-impedance state, and the TDP/TDN pins are both pulled up to 3.3V by their internal 50Ω termination resistors. The TCLKP/TCLKN output continues to toggle if enabled. If CR.TLBDO=1 then data is transmitted on TDP/TDN during terminal loopback while also being looped back to the receiver.

6.10.3 Remote Loopback

Remote loopback is enable by setting GMIICR.RLB=1. When this loopback is enabled, the transmit parallel interface logic takes data from the receive parallel interface logic rather than from the transmit parallel interface

pins. During remote loopback the rate adaption buffers, PCS encoder and decoder, and PCS auto-negotiation function all operate normally.

Loopback control bits BMCR.DLB and PCSCR.TLB must be set to zero for correct remote loopback operation. RLB cannot be used in TBI or RTBI mode unless the receive signal on RDP/RDN is frequency locked to the REFCLK signal. If the two signals are not frequency locked the rate adaption buffers will repeatedly overflow and reset causing data errors.

During remote loopback, if CR.RLBDO=0 the receive parallel interface pins RXD, RX_DV, RX_ER, CRS and COL are all driven low. If CR.RLBDO=1 then receive data and control information are output on these pins while also being looped back to the transmitter.

6.11 Diagnostic and Test Functions

Transmit PCS Pattern Generator. The PCS encoder has a built-in pattern generator block. These patterns provide different types of jitter in order to test the performance of a downstream PHY receiver. When JIT_DIAG.JIT_EN=1, the PCS encoder outputs 10-bit codes from the jitter pattern generator rather than from the 8B/10B encoding logic. The pattern to be generated is specified by JIT_DIAG.JIT_PAT. Patterns include low-, mixed- and high-frequency test patterns from 802.3 Annex 36A as well as a custom 10-bit pattern from the JIT_DIAG.CUST_PAT register field.

When JIT_EN is set to 1, pattern generation starts and packet transmission stops immediately. This can cut off the tail end of the packet currently being transmitted and can also cause a running disparity error. When JIT_EN is set to 0, pattern generation stops and packet transmission starts immediately. This can result in the transmission of only the tail end of a packet and can also cause a running disparity error.

6.12 Data Path Latencies

The MAX24287 data path latencies are shown in Table 6-21 below. These latencies exceed the full-duplex delay constraints in 802.3 Table 36-9b. Therefore MAX24287 may not be compatible with PAUSE operation as specified in 802.3 Clause 31.

Table 6-21. GMII Data Path Latencies

Event	Min, ns	Max, ns	802.3 Max, ns (#bit times)
TX_EN=1 sampled to 1st bit of /S/ on TDP/TDN	119	121	108.8 (136)
1st bit of /T/ on RDP/RDN to RX_DV deassert	211	216	153.6 (192)

6.13 Power Supply Considerations

Due to the multi-power-supply nature of the device, some I/Os have parasitic diodes between a 1.2V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the 1.2V supply and the 3.3V supply to force the 3.3V supply to be within one parasitic diode drop of the 1.2V supply. The second method is to ramp up the 3.3V supply first and then ramp up the 1.2V supply.

6.14 Startup Procedure

MAX24287 revision B requires the following start-up procedure after power-up for proper operation:

1. Assert RST_N (low) for at least 100µs after the power supplies have ramped up and are stable then deassert RST_N.
2. Write 0x0012 to the PAGESEL register. This sets bit 4 as required and selects MDIO page 2.
3. Write 0x4004 to PTPCR1 to power-down the receive CDR.
4. Wait 1ms.
5. Write 0x4000 to PTPCR1 to power-up the receive CDR.
6. Set the BMCR.DP_RST bit to reset the datapath. This bit is self-clearing.

The device can then be further configured as needed.

This procedure only applies for MAX24287 revision B.

7. Register Descriptions

The device registers can be accessed through the MDIO interface, which is part of the parallel MII interface. Registers at addresses 16 to 30 are paged using the PAGESEL.PAGE register field. Register addresses 0 to 15 and 31 are not paged and remain the same regardless of the value of PAGESEL.PAGE. Nonexistent registers are not writable and read back as high impedance.

7.1 Register Map

Table 7-1. Register Map

MDIO Register Address	Register Name	R/W
0	BMCR	RW
1	BMSR	RO
2	ID1	RO
3	ID2	RO
4	AN_ADV	RW
5	AN_RX	RO
6	AN_EXP	RO
15	EXT_STAT	RO
P0.16	JIT_DIAG	RW
P0.17	PCSCR	RW
P0.18	GMIICR	RW
P0.19	CR	RW
P0.20	IR	RW
P1.16	ID	RO
P1.17	GPIOCR1	RW
P1.18	GPIOCR2	RW
P1.19	GPIOSR	RO
P2.16	PTPCR1	RW
31	PAGESEL	RW

7.2 Register Descriptions

The register operating type is described in the “R/W” column using the following codes:

Type	Description
RW	**Read-Write.** Register field can be written and read back.
RO	**Read Only**. Register field can only be read; writing it has no effect. Write 0 for future compatibility.
SC	**Self Clearing.** Register bit self clears to 0 after being written as 1
LH-E	**Latch High—Event.** Bit latches high when the internal event occurs and returns low when it is read.
LL-E	**Latch Low—Event.** Bit latches low when the internal event occurs and returns high when it is read.
LH-C	**Latch High—Condition.** Bit latches high when the internal condition is present. If the condition is still present when the bit is read then the bit stays high. If the condition is not present when the bit is read then the bit returns low.
LL-C	**Latch Low—Condition.** Bit latches low when the internal condition is present. If the condition is still present when the bit is read then the bit stays low. If the condition is not present when the bit is read then the bit returns high.

In the register definitions below, the register addresses are provided at the end of the table title, e.g. "(MDIO 0)" for the BMCR register. Addresses 16 to 30 are bank-switched by the PAGESEL.PAGE field as shown in Table 7-1. Addresses 0 to 15 and 31 are not bank-switched.

7.2.1 BMCR

Basic Mode Control Register (MDIO 0)

Bit(s)	Name	Description	R/W	Reset
15	DP_RST	Datapath Reset. This bit resets the entire datapath from parallel MII through PCS. Self-clearing. See section 6.3.1. 0 = normal operation 1 = reset	RW, SC	0
14	DLB	Diagnostic Loopback. Transmit data is looped back to the receive path. See block diagram in Figure 2-1 for the location of this loopback and see section 6.10 for additional details. 0 = Disable diagnostic loopback (normal operation) 1 = Enable diagnostic loopback	RW	0
13	Reserved	Ignore on Read	RO	0
12	AN_EN	Auto-negotiation enable. See section 6.7. 0 = Disable 1 = Enable	RW	Note 1
11:10	Reserved	Ignore on Read	RO	0
9	AN_START	Setting this bit causes a restart of the Auto-negotiation process. Self clears. See section 6.7.	RW, SC	0
8	Reserved	Ignore on Read	RO	0
7	COL_TEST	Collision test. When this bit is set, MAX24287 asserts the COL signal within 64 parallel interface transmit clock cycles after TX_EN is asserted and deasserts the COL signal within one parallel interface transmit clock cycle after TX_EN is deasserted. See 802.3 section 22.2.4.1.9. See section 6.10.1.	RW	0
6:0	Reserved	Ignore on Read	RO	0

Note 1: At reset when COL=1 or (RXD[1:0]!=11 and RX_DV=1) AN_EN is set to 1 else it is set to 0.

7.2.2 BMSR

Basic Mode Status Register (MDIO 1)

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Ignore on read	RO	0
14	SPD100FD	100BASE-X Full Duplex capability. Always indicates 1 = able to do 100BASE-X full duplex	RO	1
13	SPD100HD	100BASE-X Half Duplex capability Always indicates 1 = able to do 100BASE-X half duplex	RO	1
12	SPD10FD	10Mb/s Full Duplex capability Always indicates 1 = able to do 10Mb/s full duplex	RO	1
11	SPD10HD	10Mb/s Half Duplex capability Always indicates 1 = able to do 10Mb/s half duplex	RO	1
10:9	Reserved	Ignore on read	RO	0
8	EXT_STAT	Extended Status information available Always indicates 1 = extended status information in EXT_STAT register	RO	1
7	Reserved	Ignore on Read	RO	0
6	MF_PRE	Management preamble suppression supported Always indicates 1 = MDIO preamble suppression is supported.	RO	1
5	AN_COMP	Auto-negotiation Complete 0 = Auto-negotiation not completed or not in progress 1 = Auto-negotiation has completed	RO	0
4	RFAULT	Remote Fault – Indicates presence of remote fault on link partner. For SGMII, remote fault is latched high when the ALOS input pin goes high or when the CDR indicates receive loss-of-lock. For 1000BASE-X, remote fault is RF≠00 in AN_RX. RFAULT is latched high when a remote fault is detected. If no remote fault is detected when RFAULT is read then RFAULT goes low. Otherwise RFAULT remains unchanged. IR.RFAULT is a read-only copy of this bit that can cause an interrupt when enabled. 0 = no remote fault has been detected since this bit was last read 1 = remote fault has occurred since this bit was last read	RO, LH-C	0
3	AN_ABIL	Auto-negotiation Ability Always indicates 1 = able to perform Auto-negotiation	RO	1
2	LINK_ST	Link Status – Indicates the status of the physical connection to the link partner. LINK_ST is latched low when the link goes down. If the PCS state machine is in the link-up state when LINK_ST is read then LINK_ST goes high. Otherwise LINK_ST remains unchanged. IR.LINK_ST is a read-only copy of this bit that can cause an interrupt when enabled. 0 = link down has occurred since this bit was last read 1 = link has been up continuously since this bit was last read	RO, LL-C	0
1	Reserved	Ignore on Read	RO	0
0	EXT_CAP	Extended Register Capability Always indicates 1 = the extended registers exist	RO	1

7.2.3 ID1 and ID2

Registers ID1 and ID2 are set to all zeroes as allowed by clause 22.2.4.3.1 of IEEE 802.3. The actual device ID can be read from the ID register.

Device ID 1 Register (MDIO 2)

Bit(s)	Name	Description	R/W	Reset
15:0	OUI_HI	OUI[3:18]	RO	0

Device ID 2 Register (MDIO 3)

Bit(s)	Name	Description	R/W	Reset
15:10	OUI_LI	OUI[19:24]	RO	0
9:4	MODEL	MODEL[5:0] Model Number	RO	0
3:0	REV	REV[3:0] Revision Number	RO	0

7.2.4 AN_ADV

The register contents are transmitted to the link partner's AN_RX register.

The fields of this register have different functions depending on whether the device is in 1000BASE-X auto-negotiation mode or in SGMII control information transfer mode. See section 6.7 for details.

Auto-Negotiation Advertisement Register (MDIO 4)

Bit(s)	Name	Description	R/W	Reset
15	AN_ADV[15] (NP_LK)	See section 6.7 for details.	RW	Note 1
14	AN_ADV[14]	Ignore on read	RO	0
13:0	AN_ADV[13:0]	See section 6.7 for details.	RW	Note 1

Note 1: The reset value of the bits of this register depend on the values of configuration pins at reset, as shown below. See section 6.1.

Configuration Pin Settings at Reset	Configuration Description	AN_ADV[15:0] Reset Value
COL=0, RX_DV=0	No auto-negotiation	0000 0000 0000 0000
COL=0, RX_DV=1, RXD[1]=0	15-pin config mode, SGMII 10 or 100Mbps	1001 0R00 0000 0001 (R = RXD[0] pin value)
COL=0, RX_DV=1, RXD[1]=1, GPO2=0	15-pin config mode, SGMII 1000Mbps	1001 1000 0000 0001
COL=0, RX_DV=1, RXD[1]=1, GPO2=1	15-pin config mode, 1000BASE-X	0000 0000 0010 0000
COL=1, GPO2=0	3-pin config mode, SGMII 1000Mbps	1001 1000 0000 0001
COL=1, GPO2=1	3-pin config mode, 1000BASE-X	0000 0000 0010 0000

7.2.5 AN_RX

The rx_Config_Reg[15:0] value received from the link partner is stored in this register.

This fields of this register have different functions depending on whether the device is in 1000BASE-X auto-negotiation mode or in SGMII control information transfer mode. See section 6.7 for details.

Auto-Negotiation Link Partner Ability Receive Register (MDIO 5)

Bit(s)	Name	Description	R/W	Reset
15	NP	See section 6.7 for details	RO	0
14	Acknowledge	1= link partner successfully received the transmitted base page.	RO	0
13:0	ABILITY	See section 6.7 for details	RO	0

7.2.6 AN_EXP

This register is used to indicate that a new link partner abilities page has been received.

Auto-negotiation Extended Status Register (MDIO 6)

Bit(s)	Name	Description	R/W	Reset
15:3	Reserved	Ignore on Read	RO	0
2	NP	Next Page capability - This device does not support next pages, it always reads as 0.	RO	0
1	PAGE	Page received, clears when read. See section 6.7. 0 = No new AN_RX page from link partner 1 = New AN_RX page from Link partner is ready	RO, LH-E	0
0	Reserved	Ignore on Read	RO	0

7.2.7 EXT_STAT

Extended Status Register (MDIO 15)

Bit(s)	Name	Description	R/W	Reset
15	1000X_FDX	1000BASE-X Full Duplex capability. Always indicates 1 = able to do 100BASE-X full duplex	RO	1
14	1000X_HDX	1000BASE-X Half Duplex capability. Always indicates 0 = not able to do 100BASE-X half duplex	RO	0
13:0	Reserved	Ignore on Read	RO	0

7.2.8 JIT_DIAG

Jitter Diagnostics Register (MDIO 0.16)

Bit(s)	Name	Description	R/W	Reset
15	JIT_EN	Jitter Pattern Enable. Enables jitter pattern to be transmitted instead of normal data on TDP/TDN. 0 = Transmit normal data patterns from PCS encoder 1 = Transmit jitter test pattern specified by JIT_PAT	RW	0
14:12	JIT_PAT	Jitter Pattern. Specifies the pattern to transmit. Includes standard patterns specified in IEEE 802.3 Annex 36A. **JIT_PAT** / **Pattern** 000 / Custom pattern defined in CUST_PAT[9:0] 001 / 802.3 Annex 36A.1 high frequency test pattern 1010101010… 010 / 802.3 Annex 36A.3 mixed frequency test pattern 1111101011 0000010100… 011 / Low frequency pattern 1111100000… 100 / "Random" jitter pattern 0011111010 1001001100 1010011100 1100010101… 101 / 802.3 Annex 36A.2 low frequency test pattern 1111100000… 110 / Reserved 111 / Reserved .	RW	0
11:10	Reserved	Write as 0, Ignore on Read	RO	0
9:0	CUST_PAT	CUST_PAT[9:0] Custom 10-bit repeating pattern used when JIT_PAT=000. The transmission order is LSB(0) to MSB(9).	RW	0

7.2.9 PCSCR

PCS Control Register (MDIO 0.17)

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Ignore on read	RO	0
14	TIM_SHRT	When PCSCR.BASEX=1 (1000BASE-X mode), this bit can be used to shorten the link timer timeout from 10ms to 1.6ms. The normal 10ms setting is called for in the 802.3 standard. When BASEX=0 this bit is ignored. 0 = PCS link timer has normal timeout 1 = PCS link timer has 1.6ms timeout	RW	0
13	DYRX_DIS	Disable Receive PCS Running Disparity. 0 = Enable PCS receive running disparity (normal) 1 = Disable PCS receive running disparity	RW	0
12	DYTX_DIS	Disable Transmit PCS Running Disparity. 0 = Enable PCS transmit running disparity (normal) 1 = Disable PCS transmit running disparity	RW	0
11:7	Reserved	Write as 0, Ignore on Read	RO	0
6	WD_DIS	Disable auto-negotiation watchdog timer. See section 6.7. 0 = Restart auto-negotiation after 5 seconds if link not up after previous start or restart 1 = Disable auto-negotiation watchdog restart	RW	0
5	Reserved	Ignore on Read	RO	0
4	BASEX	Specifies 1000BASE-X PCS mode or SGMII PCS mode. See section 6.7. 0 = SGMII PCS mode selected, link timer = 1.6 ms 1 = 1000BASE-X PCS mode selected, link timer = 10 ms (or 1.6ms when PCSCR.TIM_SHRT=1)	RW	Note 1
3:2	Reserved	Write as 0, Ignore on Read	RO	0
1	TLB	Terminal Loopback. Transmit data is looped back to the receive path at the high-speed serial interface (TDP/TDN to RDP/RDN). See block diagram in Figure 2-1 for the location of this loopback and see section 6.10 for additional details. 0 = Disable terminal loopback (normal operation) 1 = Enable terminal loopback	RW	0
0	EN_CDET	Enable comma detection and code group alignment in the ingress path. See section 6.6.2.5. 0 = Disable comma alignment 1 = Enable comma alignment (normal operation)	RW	1

Note 1: At reset, if COL=1 or RXD[1] = 1 then BASEX is set to the value of the GPO2 pin, else BASEX is set to 0. In other words, in 3-pin configuration mode OR (15-pin configuration mode AND parallel interface is set to 1000Mbps) BASEX is set to the value of the GPO2 pin. Otherwise BASEX is set to 0.

7.2.10 GMIICR

GMII Interface Control Register (MDIO 0.18)

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th><th>R/W</th><th>Reset</th></tr>
<tr><td>15:14</td><td>SPD[1:0]</td><td>Selects parallel MII interface mode. See section 6.6.
<table>
<tr><th rowspan="2">SPD</th><th rowspan="2">Speed</th><th colspan="2">Bus mode</th></tr>
<tr><th>DDR=0</th><th>DDR=1</th></tr>
<tr><td>00</td><td>10 Mbps</td><td>MII</td><td>RGMII-10</td></tr>
<tr><td>01</td><td>100 Mbps</td><td>MII</td><td>RGMII-100</td></tr>
<tr><td>10</td><td>1000 Mbps</td><td>GMII</td><td>RGMII-1000</td></tr>
<tr><td>11</td><td>1000 Mbps</td><td>TBI</td><td>RTBI</td></tr>
</table></td><td>RW</td><td>Note 1</td></tr>
<tr><td>13</td><td>TBI_RATE</td><td>Select TBI bus receive clock mode. Used when SPD[1:0]=11; ignored otherwise. See section 6.6.2.
0 = TBI with one 125MHz receive clock (RXCLK pin)
1 = Normal TBI interface: dual 62.5MHz clocks on RXCLK and TXCLK/RXCLK1 pins, 180 degrees out of phase</td><td>RW</td><td>Note 2</td></tr>
<tr><td>12</td><td>DTE_DCE</td><td>DTE-DCE mode selection for MII bus mode. Used when SPD[1:0]=0x and DDR=0; ignored otherwise. See section 6.6.5.
1 = MII-DTE (MAX24287 on MAC side of MII, both RXCLK and TXCLK are inputs)
0 = MII-DCE (MAX24287 on PHY side of MII, both RXCLK and TXCLK are outputs)</td><td>RW</td><td>Note 3</td></tr>
<tr><td>11</td><td>DDR</td><td>Reduced pin count (RGMII or RTBI) using double data rate, i.e. data sampling/updating on both edges of the clock. See the SPD[1:0] description above and section 6.6.
0 = MII, GMII or TBI bus mode
1 = RGMII or RTBI bus mode</td><td>RW</td><td>Note 4</td></tr>
<tr><td>10</td><td>TXCLK_EN</td><td>In GMII, RGMII and RTBI modes and in TBI mode with one 125MHz receive clock, the TXCLK pin is not used for parallel interface operation. The TXCLK_EN bit enables TXCLK to output a 125MHz clock from the TX PLL in those modes. TXCLK_EN is ignored in MII mode and normal TBI mode. See section 6.6.
0 = TXCLK pin is high impedance
1 = TXCLK pin outputs 125MHz clock</td><td>RW</td><td>Note 5</td></tr>
<tr><td>9:8</td><td>Reserved</td><td>Write as 0, ignore on Read</td><td>RO</td><td>0</td></tr>
<tr><td>7</td><td>Reserved</td><td>Write as 1, ignore on Read</td><td>RW</td><td>1</td></tr>
<tr><td>6:4</td><td>Reserved</td><td>Write as 0, ignore on Read</td><td>RO</td><td>0</td></tr>
<tr><td>3</td><td>REF_INV</td><td>REFCLK Invert control.
0 = Noninverted
1 = Inverted</td><td>RW</td><td>0</td></tr>
<tr><td>2:1</td><td>Reserved</td><td>Write as 0, ignore on Read</td><td>RO</td><td>0</td></tr>
<tr><td>0</td><td>RLB</td><td>Remote Loopback. Receive data is looped back to the transmit path. See block diagram in Figure 2-1 for the location of this loopback and see section 6.10 for additional details.
0 = Disable remote loopback (normal operation)
1 = Enable remote loopback</td><td>RW</td><td>0</td></tr>
</table>

Note 1: At reset if COL=0 then SPD[1:0] is set to the value on the RXD[1:0] pins, else SPD[1:0] is set to 10. In other words, in 15-pin configuration mode SPD[1:0] is set to the value on the RXD[1:0] pins. In 3-pin configuration mode SPD[1:0] is set to 10 (1000Mbps).

Note 2: At reset if COL=0 the TBI_RATE bit is set to the value on the RX_DV pin, else TBI_RATE is set to 0. In other words, in 15-pin configuration mode the TBI_RATE bit is set to the value on the RX_DV pin. In 3-pin configuration mode TBI_RATE is set to 0.

Note 3: At reset if COL=0 and RXD[1] = 0 the DTE_DCE bit is set to the value on the GPO2 pin, else DTE_DCE is set to 0. In other words, in 15-pin configuration mode when the parallel interface is configured for 10Mbps or 100Mbps the DTE_DCE bit is set to the value on the GPO2 pin. Otherwise the DTE_DCE bit is set to 0.

Note 4: At reset the DDR bit is set to the value on the CRS pin.
Note 5: At reset if COL=0 the TXCLK_EN bit is set to the value on the TXCLK pin, else TXCLK_EN is set to 1. In other words, in 15-pin configuration mode the TXCLK_EN bit is set to the value on the TXCLK pin. In 3-pin configuration mode TXCLK_EN is set to 1.

7.2.11 CR

Control Register (MDIO 0.19)

Bit(s)	Name	Description	R/W	Reset
15:13	Reserved	Write as 0, Ignore on Read	RO	0
12	DLBDO	Diagnostic Loopback Data Out. Set this bit to enable transmit data to be output on the serial interface during diagnostic loopback (i.e. when BMCR.DLB=1). See section 6.10.	RW	0
11	RLBDO	Remote Loopback Data Out. Set this bit to enable receive data to be output on the parallel interface during remote loopback (i.e. when GMIICR.RLB=1). See section 6.10.	RW	0
10	TLBDO	Terminal Loopback Data Out. Set this bit to enable transmit data (rather than zeros) to be output on the serial interface during terminal loopback (i.e. when PCSCR.TLB=1). See section 6.10.	RW	0
9	RCFREQ	Specifies which recovered clock frequency to output on a GPIO pin. See section 6.2. 0 = 25MHz 1 = 125MHz	RW	0
8	RCSQL	Set this bit to squelch the recovered clock on GPO2, GPIO2 and GPIO4-7 when any of several squelch conditions occur. See sections 6.2.1. 0 = Recovered clock output not squelched 1 = Recovered clock squelched when a squelch condition occurs	RW	0
7:6	Reserved	Write as 0, Ignore on Read	RO	0
5	TCLK_EN	Serial interface transmit clock output enable. See section 6.5. 0 = Disable TCLKP/TCLKN 1 = Enable TCLKP/TCLKN	RW	0
4:0	Reserved	Write as 0, Ignore on Read	RO	0

7.2.12 IR

This register contains both latched status bits and interrupt enable bits. When the latched status bit is active and the associated interrupt enable bit is set an interrupt signal can be driven onto one of the GPIO pins by configuring the GPIOCR1 register.

Interrupt Register 1 (MDIO 0.20)

Bit(s)	Name	Description	R/W	Reset
15:14	Reserved	Write as 0, Ignore on Read	RO	0
13	RFAULT_IE	Interrupt Enable for RFAULT. 0 = interrupt disabled 1 = interrupt enabled	RO	0
12	LINK_ST_IE	Interrupt Enable for LINK_ST. 0 = interrupt disabled 1 = interrupt enabled	RO	0
11	ALOS_IE	Interrupt Enable for ALOS. See section 6.5. 0 = interrupt disabled 1 = interrupt enabled	RW	0
10	PAGE _IE	Interrupt Enable for PAGE. See section 6.7. 0 = interrupt disabled 1 = interrupt enabled	RW	0
9	RLOL_IE	Interrupt Enable for RLOL. See section 6.5. 0 = interrupt disabled 1 = interrupt enabled	RW	0
8	RLOS_IE	Interrupt Enable for RLOS. See section 6.5. 0 = interrupt disabled 1 = interrupt enabled	RW	0
7:6	Reserved	Write as 0, Ignore on Read	RO	0
5	RFAULT	Remote Fault. This is a read-only copy of BMSR.RFAULT. An interrupt is generated when RFAULT=1 and RFAULT_IE=1.	RO	0
4	LINK_ST	Link Status. This is a read-only copy of BMSR.LINK_ST (active low). An interrupt is generated when LINK_ST=0 and LINK_ST_IE=1.	RO	0
3	ALOS	Analog Loss-of-Signal latched status bit. Set when ALOS input pin goes high. An interrupt is generated when ALOS=1 and ALOS_IE=1. See section 6.5. 0 = Defect not detected since last read 1 = Defect detected since last read	RO, LH-C	0
2	PAGE	This is a read-only copy of AN_EXP.PAGE. An interrupt is generated when PAGE=1 and PAGE_IE=1. See section 6.7. 0 = Defect not detected since last read 1 = Defect detected since last read	RO	0
1	RLOL	Receive CDR Loss-of-Lock latched status bit. Set when the CDR PLL loses lock. An interrupt is generated when RLOL=1 and RLOL_IE=1. See section 6.9.1. 0 = Defect not detected since last read 1 = Defect detected since last read	RO, LH-C	0
0	RLOS	Receive CDR Loss-of-Signal latched status bit. Set when the CDR block sees no transitions in the incoming signal for 24 consecutive bit times. See section 6.5. 0 = Defect not detected since last read 1 = Defect detected since last read	RO, LH-C	0

7.2.13 PAGESEL

This page select register is used to extend the MDIO register space by mapping any of several pages of 15 registers into MDIO register addresses 16 to 30. PAGESEL also has a global interrupt status bit. This register is available on all pages at MDIO register address 31.

Page Register (MDIO 31, on all pages)

Bit(s)	Name	Description	R/W	Reset
15	TEST	Factory Test. Always write 0.	RW	0
14	Reserved	Ignore on Read	RO	0
13	IR	Interrupt from IR register. This bit is set if any latched status bit and its associated interrupt enable bit are both active in the IR register. See section 6.3.2. 0 = interrupt source not active 1 = interrupt source is active	RO	0
12:5	Reserved	Ignore on Read	RO	0
4	Reserved	This bit must be set to 1 for proper operation. Ignore on Read.	RW	0
3:2	Reserved	Ignore on Read	RO	0
1:0	PAGE[1:0]	Page selection for MDIO register addresses 16 to 30. See section 7. 00 = PHY extended register page 0 01 = PHY extended register page 1 10 = PHY extended register page 2 11 = PHY extended register page 3	RW	00

7.2.14 ID

The ID register matches the JTAG device ID (lower 12 bits) and revision (all 4 bits).

Device ID Register (MDIO 1.16)

Bit(s)	Name	Description	R/W	Reset
15:12	REV	REV[3:0] Device revision number. Contact factory for value.	RO	Note 1
11:0	DEVICE	DEVICE[11:0] Device ID	RO	Note 1

Note 1: See Device Code in Table 8-2.

7.2.15 GPIOCR1

GPIO Control Register 1 (MDIO 1.17)

Bit(s)	Name	Description	R/W	Reset
15	RST	Global device reset. Pin states are sampled and used to set the default values of several register fields. See section 6.3.1. 0 = normal operation 1 = reset	RW, SC	0
14:12	GPO1_SEL[2:0]	GPO1 output pin mode selection. See Table 6-4.	RW	Note 2
11:9	GPO2_SEL[2:0]	GPO2 output pin mode selection. See Table 6-5.	RW	Note 2
8:6	GPIO1_SEL[2:0]	GPIO1 output pin mode selection. See Table 6-4.	RW	Note 1
5:3	GPIO2_SEL[2:0]	GPIO2 output pin mode selection. See Table 6-5.	RW	000
2:0	GPIO3_SEL[2:0]	GPIO3 output pin mode selection. See Table 6-4.	RW	000

Note 1: At reset if COL=0 and GPO1=1 the GPIO1_SEL bits are set to 100 (125MHz), else the bits are set to 000 (high impedance).
Note 2: At reset if COL=0 and RXD[1:0]=11 (TBI or RTBI) the bits are set to 000, else the bits are set to 110.

7.2.16 GPIOCR2

GPIO Control Register 2 (MDIO 1.18)

Bit(s)	Name	Description	R/W	Reset
15:14	Reserved	Ignore on Read	RO	0
13	GPIO47_LSC	GPIO4-7 Latched Status Control. This bit controls the behavior of latched status bits GPIO4L through GPIO7L in GPIOSR. See section 6.2. 0 = Set latched status bit when input goes low 1 = Set latched status bit when input goes high	RW	0
12	GPIO13_LSC	GPIO1-3 Latched Status Control. This bit controls the behavior of latched status bits GPIO1L through GPIO3L in GPIOSR. See section 6.2. 0 = Set latched status bit when input goes low 1 = Set latched status bit when input goes high	RW	0
11:9	GPIO7_SEL[2:0]	GPIO7 output pin mode selection. See Table 6-6.	RW	000
8:6	GPIO6_SEL[2:0]	GPIO6 output pin mode selection. See Table 6-6.	RW	000
5:3	GPIO5_SEL[2:0]	GPIO5 output pin mode selection. See Table 6-6.	RW	000
2:0	GPIO4_SEL[2:0]	GPIO4 output pin mode selection. See Table 6-6.	RW	000

7.2.17 GPIOSR

GPIO Status Register (MDIO 1.19)

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Ignore on Read	RO	0
14	GPIO7L	GPIO7 latched status. Set when the transition specified by GPIOCR2.GPIO47_LSC occurs on the GPIO7 pin. 0 = Transition did not occur since this bit was last read 1 = Transition did occur since this bit was last read	RO, LH-E	0
13	GPIO6L	GPIO6 latched status. Set when the transition specified by GPIOCR2.GPIO47_LSC occurs on the GPIO6 pin. 0 = Transition did not occur since this bit was last read 1 = Transition did occur since this bit was last read	RO, LH-E	0
12	GPIO5L	GPIO5 latched status. Set when the transition specified by GPIOCR2.GPIO47_LSC occurs on the GPIO5 pin. 0 = Transition did not occur since this bit was last read 1 = Transition did occur since this bit was last read	RO, LH-E	0
11	GPIO4L	GPIO4 latched status. Set when the transition specified by GPIOCR2.GPIO47_LSC occurs on the GPIO4 pin. 0 = Transition did not occur since this bit was last read 1 = Transition did occur since this bit was last read	RO, LH-E	0
10	GPIO3L	GPIO3 latched status. Set when the transition specified by GPIOCR2.GPIO13_LSC occurs on the GPIO3 pin. 0 = Transition did not occur since this bit was last read 1 = Transition did occur since this bit was last read	RO, LH-E	0
9	GPIO2L	GPIO2 latched status. Set when the transition specified by GPIOCR2.GPIO13_LSC occurs on the GPIO2 pin. 0 = Transition did not occur since this bit was last read 1 = Transition did occur since this bit was last read	RO, LH-E	0
8	GPIO1L	GPIO1 latched status. Set when the transition specified by GPIOCR2.GPIO13_LSC occurs on the GPIO1 pin. 0 = Transition did not occur since this bit was last read 1 = Transition did occur since this bit was last read	RO, LH-E	0
7	Reserved	Ignore on Read	RO	0
6	GPIO7	GPIO7 pin real time status. See section 6.2. 0 = Pin low 1 = Pin high	RO	0
5	GPIO6	GPIO6 pin real time status. 0 = Pin low 1 = Pin high	RO	0
4	GPIO5	GPIO5 pin real time status. 0 = Pin low 1 = Pin high	RO	0
3	GPIO4	GPIO4 pin real time status. 0 = Pin low 1 = Pin high	RO	0
2	GPIO3	GPIO3 pin real time status. 0 = Pin low 1 = Pin high	RO	0
1	GPIO2	GPIO2 pin real time status. 0 = Pin low 1 = Pin high	RO	0
0	GPIO1	GPIO1 pin real time status. 0 = Pin low 1 = Pin high	RO	0

7.2.18 PTPCR1

PTP Control Register 1 (MDIO 2.16)

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Write 0; Ignore on read	RW	0
14	Reserved	Write 1; ignore on read	RW	1
13:12	Reserved	Write 0; Ignore on read	RW	0
11:7	Reserved	Write 0; Ignore on read	RO	0
6	Reserved	Write 0; Ignore on read	RW	0
5	PLL_PWDN	TX PLL Power Down. Setting this bit powers down and bypasses the TX PLL. 0 = Power-down disabled 1 = Power-down enabled	RW	0
4	Reserved	Write 0; Ignore on read	RW	0
3	TX_PWDN	Serial Interface Transmit Power Down. Setting this bit powers down the transmit serializer and the TDP/TDN and TCLKP/TCLN output drivers. See section 6.5. 0 = Power-down disabled 1 = Power-down enabled	RW	0
2	RX_PWDN	Serial Interface Receive Power Down. Setting this bit powers down the RDP/RDN inputs, the clock and data recovery PLL, and the de-serializer. See section 6.5. 0 = Power Down Disabled 1 = Power Down Enabled	RW	0
1:0	Reserved	Write 0; Ignore on read	RW	0

8. JTAG and Boundary Scan

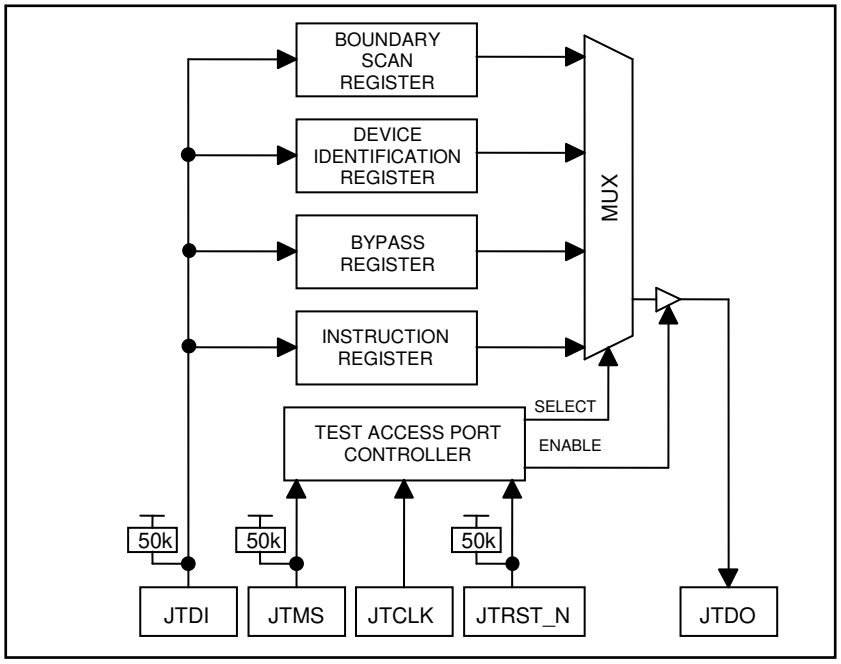
8.1 JTAG Description

The MAX24287 supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. Figure 8-1 shows a block diagram. The MAX24287 contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

Test Access Port (TAP)	Bypass Register
TAP Controller	Boundary Scan Register
Instruction Register	Device Identification Register

The TAP has the necessary interface pins, namely JTCLK, JTRST_N, JTDI, JTDO, and JTMS. Details on these pins can be found in Table 5-4. Details about the boundary scan architecture and the TAP can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

Figure 8-1. JTAG Block Diagram



8.2 JTAG TAP Controller State Machine Description

This section discusses the operation of the TAP controller state machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. Each of the states denoted in Figure 8-2 are described in the following paragraphs.

Test-Logic-Reset. Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the device operates normally.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The instruction register and all test registers remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR. Data can be parallel-loaded into the test register selected by the current instruction. If the instruction does not call for a parallel load or the selected test register does not allow parallel loads, the register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

Shift-DR. The test register selected by the current instruction is connected between JTDI and JTDO and data is shifted one stage toward the serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output because of changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the instruction register's shift register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and the test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state, while moving data one stage through the instruction shift register.

Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

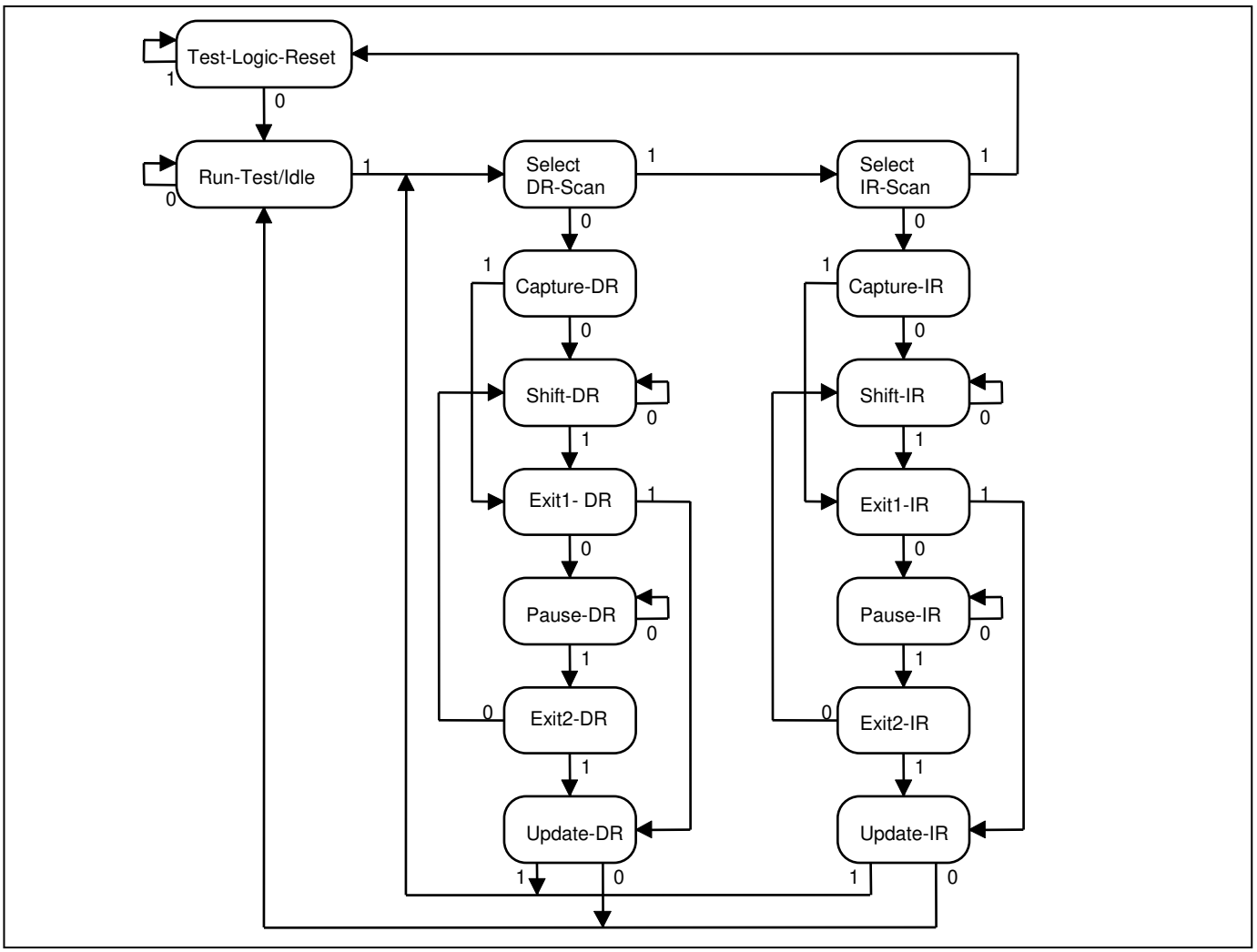
Pause-IR. Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A

rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Figure 8-2. JTAG TAP Controller State Machine



8.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Table 8-1 shows the instructions supported by the MAX24287 and their respective operational binary codes.

Table 8-1. JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD. SAMPLE/RELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. First, the digital I/Os of the device can be sampled at the boundary scan register, using the Capture-DR state, without interfering with the device's normal operation. Second, data can be shifted into the boundary scan register through JTDI using the Shift-DR state.

EXTEST. EXTEST allows testing of the interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur: (1) Once the EXTEST instruction is enabled through the Update-IR state, the parallel outputs of the digital output pins are driven. (2) The boundary scan register is connected between JTDI and JTDO. (3) The Capture-DR state samples all digital inputs into the boundary scan register.

BYPASS. When the BYPASS instruction is latched into the parallel instruction register, JTDI is connected to JTDO through the 1-bit bypass register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

IDCODE. When the IDCODE instruction is latched into the parallel instruction register, the device identification register is selected. The device ID code is loaded into the device identification register on the rising edge of JTCLK, following entry into the Capture-DR state. Shift-DR can be used to shift the ID code out serially through JTDO. During Test-Logic-Reset, the ID code is forced into the instruction register's parallel output.

HIGHZ. All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

CLAMP. All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

8.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included in the device design. It is used with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Bypass Register. This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions to provide a short path between JTDI and JTDO.

Boundary Scan Register. This register contains a shift register path and a latched parallel output for control cells and digital I/O cells. BSDL files are available on the MAX24287 page of Microsemi's website..

Identification Register. This register contains a 32-bit shift register and a 32-bit latched parallel output. It is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. The device identification code for the MAX24287 is shown in Table 8-2.

Table 8-2. JTAG ID Code

DEVICE	REVISION	DEVICE CODE	MANUFACTURER CODE	REQUIRED
MAX24287A	0001	0101 1110 1101 1111	00010100001	1
MAX24287B	0001	0101 1110 1110 0000	00010100001	1

9. Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Signal IO Lead with Respect to VSS ..... -0.3V to +5.5V
Supply Voltage (VDD12) Range with Respect to VSS ..... -0.3V to +1.32V
Supply Voltage (VDD33) Range with Respect to VSS ..... -0.3V to +3.63V
Operating Temperature Range: Industrial ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device. Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.

Note 1: The typical values listed in the tables of section 9 are not production tested.
Note 2: Specifications to T_A = -40°C are guaranteed by design and not production tested.

9.1 Recommended Operating Conditions

Table 9-1. Recommended DC Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, Nominal 1.2V	VDD12		1.14	1.2	1.26	V
Supply Voltage, Nominal 3.3V	VDD33		3.135	3.3	3.465	V
Ambient Temperature Range	T_A		-40		+85	°C
Junction Temperature Range	T_J		-40		+125	°C

9.2 DC Electrical Characteristics

Unless otherwise stated, all specifications in this section are valid for VDD12 = 1.2V ±5%, VDD33 = 3.3V ±5% and T_A = -40°C to +85°C.

Table 9-2. DC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, VDD12 Pins	I_{DD12}	10, 25 or 125MHz REFCLK		135		mA
Supply Current, VDD33 Pin	I_{DD33}	10, 25 or 125MHz REFCLK		100		mA
Supply Current, VDD12 Pins	I_{DD12}	12.8MHz REFCLK (Note 1)		160	205	mA
Supply Current, VDD33 Pin	I_{DD33}	12.8MHz REFCLK		140	175	mA
Input Capacitance	C_{IN}			4		pF
Output Capacitance	C_{OUT}			7		pF

Note 1: When a 12.8MHz oscillator is used the TX PLL uses a two-stage process to perform the frequency conversion and therefore consumes additional power.

9.2.1 CMOS/TTL DC Characteristics

Table 9-3. DC Characteristics for Parallel and MDIO Interfaces

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	I_{OH} = -1mA, V_{DD}=3.135V	2.4		5.5	V
Output Low Voltage	V_{OL}	I_{OL} = 1mA, V_{DD}=3.135V	0		0.4	V
Output High Voltage	V_{OH}	MDC, MDIO. Notes 1, 3, 4	2.4		V_{DD}	V
Output Low Voltage	V_{OL}	MDC, MDIO. Notes 2, 3, 4	0		0.4	V
Input High Voltage	V_{IH}		2.0		V_{DD}+0.2V	V
Input Low Voltage	V_{IL}		-0.2		0.8	V
Input High Current	I_{IH}	VIN=3.3V			10	µA
Input Low Current, all other Input Pins	I_{IL}	VIN=0V	-10			µA
Output and I/O Leakage (when High Impedance)	I_{LO}		-10		+10	µA

Note 1: I_{OH}=-4mA
Note 2: I_{OL}=4mA
Note 3: MDC load: 340pF max.
Note 4: MDIO load: 340pF max plus 2kΩ±5% pulldown resistor.

9.2.2 SGMII/1000BASE-X DC Characteristics

Table 9-4. SGMII/1000BASE-X Transmit DC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage High, TDP or TDN (Single-Ended)	$V_{OH,DC}$	DC-coupled. Load: 50Ω pullup resistors to TVDD33 on TDP pin and on TDN pin. (Note 1)		V_{TVDD33}		V
Output Voltage Low, TDP or TDN (Single-Ended)	$V_{OL,DC}$			V_{TVDD33} – 0.4		V
Output Common Mode Voltage	$V_{OCM,DC}$			V_{TVDD33}– 0.2		V
Differential Output Voltage $\|V_{TDP} – V_{TDN}\|$	$V_{OD,DC}$		320	400	500	mV
Differential Output Voltage $\|V_{TDP} – V_{TDN}\|$ Peak-to-Peak	$V_{OD,DC,PP}$		640	800	1000	mV_{P-P}
Output Common Mode Voltage	$V_{OCM,AC}$	AC-coupled to100Ω load. See Figure 6-5.		V_{TVDD33}– 0.4		V
Differential Output Voltage, $\|V_{TDP} – V_{TDN}\|$	$V_{OD,AC}$			400		mV
Differential Output Voltage, $\|V_{TDP} – V_{TDN}\|$ Peak-to-Peak	$V_{OD,AC,PP}$			800		mV_{P-P}
Output Impedance	R_{OUT}	Single Ended, to TVDD33	35	50	65	Ω
Mismatch in a pair	ΔR_{OUT}				10	%

Table 9-5. SGMII/1000BASE-X Receive DC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage, RDP pin	V_{RDP}		1.4		V_{RVDD33}	V
Input Voltage, RDN pin	V_{RDN}		1.4		V_{RVDD33}	V
Input Common Mode Voltage	V_{ICM}	External components as shown in Figure 6-5.		2.64		V
Input Differential Voltage	V_{ID}	$\|V_{RDP} – V_{RDN}\|$	200		1600	mV

9.3 AC Electrical Characteristics

Unless otherwise stated, all specifications in this section are valid for VDD12 = 1.2V ±5%, VDD33 = 3.3V ±5% and T_A = -40°C to +85°C.

9.3.1 REFCLK AC Characteristics

Table 9-6. REFCLK AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Accuracy	Δf/f		-100		+100	ppm
Duty Cycle			40		60	%
Rise Time (20–80%)	t_R				1	ns
Fall Time (20–80%)	t_F				1	ns

REFCLK Jitter: See Table 9-10 below.

9.3.2 SGMII/1000BASE-X Interface Receive AC Characteristics

Table 9-7. 1000BASE-X and SGMII Receive AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Data Rate, Nominal	f_{IN}			1250		Mbps
Input Frequency Accuracy	Δf/f		-100		+100	ppm
Skew, RDP vs. RDN	|tskew|	Note 1			20	ps

Note 1: Measured at 50% of the transition

Table 9-8. 1000BASE-X and SGMII Receive Jitter Tolerance

PARAMETER	SYMBOL	CONDITIONS	UI p-p	ps p-p
Rx Jitter Tolerance, Deterministic Jitter, max	DJ_{RD}	Note 1, 2	0.46	370
Rx Jitter Tolerance, Total Jitter, max	TJ_{RD}	Note 1, 2	0.75	600

Note 1: Jitter requirements represent high-frequency jitter (above 637kHz) and do not represent low-frequency jitter or wander. Random jitter = Total Jitter minus Deterministic Jitter.

Note 2: The bandwidth of the CDR PLL is approximately 4MHz.

9.3.3 SGMII/1000BASE-X Interface Transmit AC Characteristics

Table 9-9. SGMII and 1000BASE-X Transmit AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TCLKP/TCLKN Duty Cycle		at 625MHz	48		52	%
Rise Time (20–80%)	t_R		100		200	ps
Fall Time (20–80%)	t_F		100		200	ps
TCLK edge to TD valid data	$t_{clock2q}$	Note 1	250		550	ps

Note 1: Measured at 0V differential. Does not include effects of jitter.

Table 9-10. 1000BASE-X Transmit Jitter Characteristics

PARAMETER	SYMBOL	CONDITIONS	Typical		Max	
			UI p-p	ps p-p	UI p-p	ps p-p
Tx Output Jitter, Deterministic	DJ_{TD}	Note 1, 2	0.025	20	0.10	80
Tx Output Jitter, Total	TJ_{TD}	Note 1, 2	0.0875	70	0.24	192

Note 1: Jitter requirements represent high-frequency jitter (above 637kHz) and do not represent low-frequency jitter or wander. Random jitter = Total Jitter minus Deterministic Jitter.

Note 2: Typical values are room-temperature measurements with a Connor-Winfield MX010 crystal oscillator connected to the REFCLK pin. Note that the bandwidth of the TX PLL is in the 300-400kHz range.

9.3.4 Parallel Interface Receive AC Characteristics

Figure 9-1. MII/GMII/RGMII/TBI/RTBI Receive Timing Waveforms

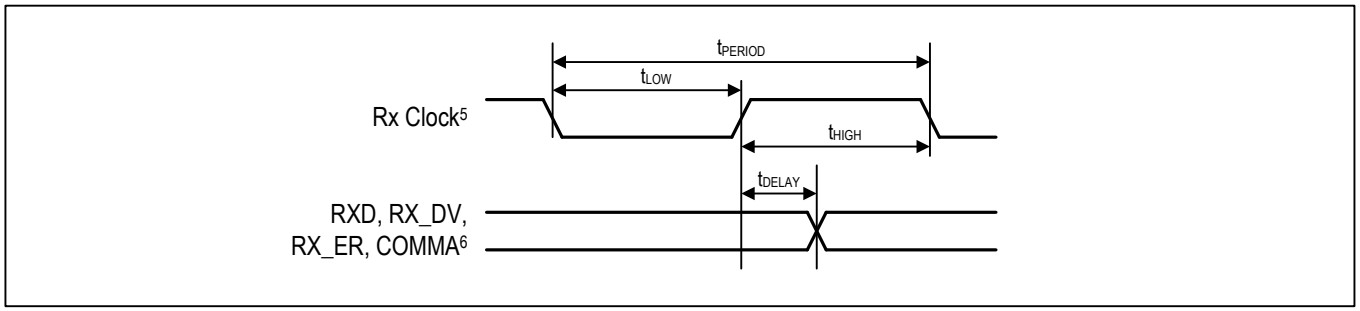


Table 9-11. GMII and TBI Receive AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RXCLK Period	t_{PERIOD}	GMII or TBI with one 125MHz Rx clock, Note 5	7.5	8	8.5	ns
RXCLK, RXCLK1 Period	t_{PERIOD}	Normal TBI	15	16	17	ns
Rx Clock[5] Duty Cycle			40		60	%
Rx Clock[5] Rising Edge to RXD, RX_DV, RX_ER, COMMA Valid	t_{DELAY}	Notes 1, 6	1		5.5	ns
RXCLK Rise Time	t_R	GMII mode, 0.7V to 1.9V			1	ns
RXCLK Fall Time	t_F	GMII mode, 1.9V to 0.7V			1	ns
Rx Clock[5] Rise Time	t_R	TBI mode, 0.8V to 2.0V			2	ns
Rx Clock[5] Fall Time	t_F	TBI mode, 2.0V to 0.8V			2	ns
Rx Clock[5] Slew Rate Rising		0.7V to 1.9V, Note 2	0.6			V/ns
Rx Clock[5] Slew Rate Falling		1.9V to 0.7V, Note 2	0.6			V/ns
RXCLK vs. RXCLK1 Skew	t_{RCSKEW}	Normal TBI mode	7.5	8	8.5	ns
RXCLK, RXCLK1 Drift Rate	t_{DRIFT}	Normal TBI mode, Note 3	0.2			µs/MHz

Note 1: 802.3 specifies setup and hold times for the receiver of the signals. This output delay specification has values that ensure 802.3 setup and hold specifications are met.

Note 2: Clock Slew rate is the instantaneous rate of change of the clock potential with respect to time (dV/dt), not an average value over the entire rise or fall time interval. Conformance with this specification guarantees that the clock signals will rise and fall monotonically through the switching region.

Note 3: t_{DRIFT} is the (minimum) time for RXCLK/RXCLK1 to drift from 63.5MHz to 64.5MHz or 60MHz to 59MHz from the RXCLK lock value. It is applicable under all input signal conditions (except during the code group alignment process), including invalid or absent input signals, provided that the receiver clock recovery unit was previously locked to REFCLK or to a valid input signal.

Note 4: All specifications in this table are guaranteed by design with output load of 5pF for GMII mode and 10pF for TBI.

Note 5: The term "Rx Clock" above stands for RXCLK in GMII mode, both RXCLK and RXCLK1 in normal TBI mode, and RXCLK for TBI with one 125MHz receive clock.

Note 6: COMMA signal only applicable in TBI and RTBI modes.

Table 9-12. RGMII-1000 and RTBI Receive AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RXCLK Period	t_{PERIOD}		7.5	8	8.5	ns
RXCLK Duty Cycle		t_{LOW} % of t_{PERIOD} , Note 1	45		55	%
RXCLK to RXD, RX_CTL Delay	t_{DELAY}	Notes 2, 3	-0.2		0.8	ns
Rise Time, All RX Signals	t_R	20% to 80%			0.75	ns
Fall Time, All RX Signals	t_F	20% to 80%			0.75	ns

Note 1: Per the RGMII spec, duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three clock cycles of the lowest speed transitioned between.
Note 2: RXCLK timing is from both edges in RGMII 1000 Mbps mode.
Note 3: the RGMII specification requires clocks to be routed such that a trace delay is added to the RXCLK signal to provide sufficient setup time for RXD and RX_CTL vs. RXCLK at the receiving component.
Note 4: All specifications in this table are guaranteed by design with output load of 5pF.

Table 9-13. RGMII-10/100 Receive AC Characteristics

PARAMETER	SYMBOL	10 Mbps			100 Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RXCLK Period	t_{PERIOD}		400			40		ns
RXCLK Duty Cycle (Note 4)		45		55	45		55	%
RXCLK to RXD, RX_CTL Delay (Notes 1, 2)	t_{DELAY}	-0.2		0.8	-0.2		0.8	ns
Rise Time, All RX Signals, 20% to 80%	t_R			0.75			0.75	ns
Fall Time, All RX Signals, 20% to 80%	t_F			0.75			0.75	ns

Note 1: RXCLK to RXD is timed from rising edge.
Note 2: RXCLK to RX_CTL is timed from both RXCLK edges.
Note 3: Per the RGMII spec, duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three clock cycles of the lowest speed transitioned between.
Note 4: All specifications in this table are guaranteed by design with output load of 5pF.

Table 9-14. MII–DCE Receive AC Characteristics

PARAMETER	SYMBOL	10 Mbps			100 Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RXCLK Period	t_{PERIOD}		400			40		ns
RXCLK Duty Cycle		45		55	45		55	%
RXCLK to RXD, RX_DV, RX_ER Delay	t_{DELAY}	180		230	18		30	ns

Note 1: RXCLK is an output in this mode.
Note 2: 802.3 specifies setup and hold times, but setup and hold specifications are typically for inputs to an IC rather than outputs. This output delay specification has values that ensure 802.3 setup and hold specifications are met.
Note 3: All specifications in this table are guaranteed by design with output load of 5pF.

Table 9-15. MII–DTE Receive AC Characteristics

PARAMETER	SYMBOL	10 Mbps			100 Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RXCLK Period	t_{PERIOD}		400			40		ns
RXCLK Duty Cycle		45		55	45		55	%
RXCLK to RXD, RX_DV, RX_ER Delay	t_{DELAY}	0		10	0		10	ns

Note 1: RXCLK is an input in this mode.
Note 2: 802.3 specifies setup and hold times, but setup and hold specifications are typically for inputs to an IC rather than outputs. This output delay specification has values that ensure 802.3 setup and hold specifications are met.
Note 3: All specifications in this table are guaranteed by design with output load of 5pF.

9.3.5 Parallel Interface Transmit AC Characteristics

Figure 9-2. MII/GMII/RGMII/TBI/RTBI Transmit Timing Waveforms

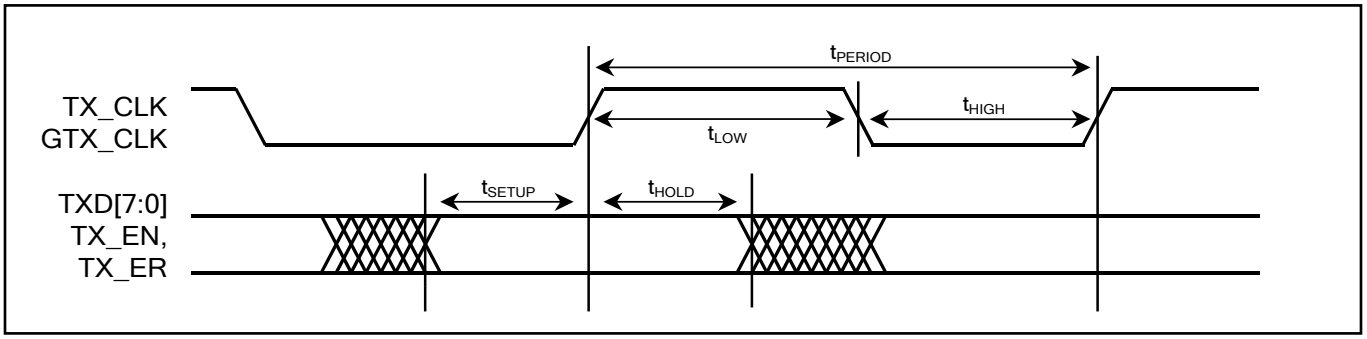


Table 9-16. GMII, TBI, RGMII-1000 and RTBI Transmit AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Low, AC	V_{IL_AC}				0.9	V
Input Voltage High, AC	V_{IH_AC}		1.7			V
GTXCLK Period	t_{PERIOD}		7.2	8	8.8	ns
GTXCLK Low Time	t_{LOW}		2.5			ns
GTXCLK High Time	t_{HIGH}		2.5			ns
GTXCLK Duty Cycle		GMII mode or TBI mode, t_{LOW} % of t_{PERIOD}	40		60	%
GTXCLK Duty Cycle		RGMII-1000 mode, t_{LOW} % of t_{PERIOD}	45		55	%
GTXCLK, TXD, TX_DV, TX_ER Rise Time	t_R	30% to 70% of VDD33, Note 1	0.5		2	ns
GTXCLK, TXD, TX_DV, TX_ER Fall Time	t_F	70% to 30% of VDD33, Note 1	0.5		2	ns
TXD, TX_DV, TX_ER to GTXCLK Setup Time	t_{SETUP}	Note 1	1			ns
GTXCLK to TXD, TX_DV, TX_ER Hold Time	t_{HOLD}	Note 1	0			ns

Note 1: GTXCLK timing is from both edges in RGMII 1000 Mbps mode.
Note 2: All specifications in this table are guaranteed by design.

Table 9-17. RGMII-10/100 Transmit AC Characteristics

PARAMETER	SYMBOL	10 Mbps			100 Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
GTXCLK Period	t_{PERIOD}		400			40		ns
GTXCLK Duty Cycle (Note 3)		40		60	40		60	%
TXD, TX_CTL to GTXCLK Setup Time	t_{SETUP}	1			1			ns
GTXCLK to TXD, TX_CTL Hold Time	t_{HOLD}	0			0			ns
Rise Time, All TX Signals, 0.5V to 2.0V	t_R			0.75			0.75	ns
Fall Time, All TX Signals, 0.5V to 2.0V	t_F			0.75			0.75	ns

Note 1: TXCLK to TXD is timed from rising edge.
Note 2: TXCLK to TX_CTL is timed from both TXCLK edges.
Note 3: Per the RGMII spec, duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three clock cycles of the lowest speed transitioned between.
Note 4: All specifications in this table are guaranteed by design.

Table 9-18. MII–DCE Transmit AC Characteristics

PARAMETER	SYMBOL	10 Mbps			100 Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TXCLK Period	t_{PERIOD}		400			40		ns
TXCLK Duty Cycle		45		55	45		55	%
TXD, TX_DV, TX_ER to TXCLK Setup Time	t_{SETUP}	6.5			6.5			ns
TXCLK to TXD, TX_DV, TX_ER Hold Time	t_{HOLD}	0			0			ns

Note 1: TXCLK is an output in this mode.
Note 2: All specifications in this table are guaranteed by design.

Table 9-19. MII–DTE Transmit AC Characteristics

PARAMETER	SYMBOL	10 Mbps			100 Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TXCLK Period	t_{PERIOD}		400			40		ns
TXCLK Duty Cycle		40		60	40		60	%
TXD, TX_DV, TX_ER to TXCLK Setup Time	t_{SETUP}	6.5			6.5			ns
TXCLK to TXD, TX_DV, TX_ER Hold Time	t_{HOLD}	0			0			ns

Note 1: TXCLK is an input in this mode.
Note 2: All specifications in this table are guaranteed by design.

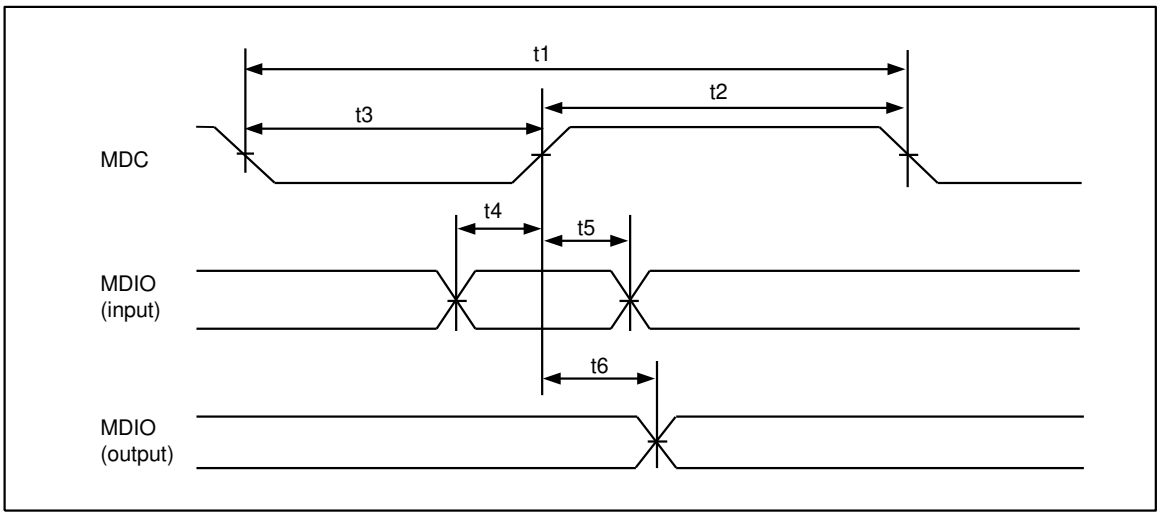
9.3.6 MDIO Interface AC Characteristics

Table 9-20. MDIO Interface AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
MDC Input Period (12.5MHz)	t1	Note 1	80			ns
MDC Input High	t2	Notes 1, 2	30			ns
MDC Input Low	t3	Notes 1, 2	30			ns
MDIO Input Setup Time to MDC	t4	Note 1	10			ns
MDIO Input Hold Time from MDC	t5	Note 1	10			ns
MDC to MDIO Output Delay	t6	Note 1,3	0		40	ns
MDC to MDIO High Impedance	t6	Note 1,4	0		40	ns

Note 1: The input/output timing reference level for all signals is VDD33/2. All parameters are with 340pF load on MDC and 340pF load and 2kΩ pulldown on MDIO.
Note 2: All specifications in this table are guaranteed by design.
Note 3: Data is valid on MDIO until min delay time.
Note 4: When going to high impedance, data is valid until min and signal is high impedance after max.

Figure 9-3. MDIO Interface Timing



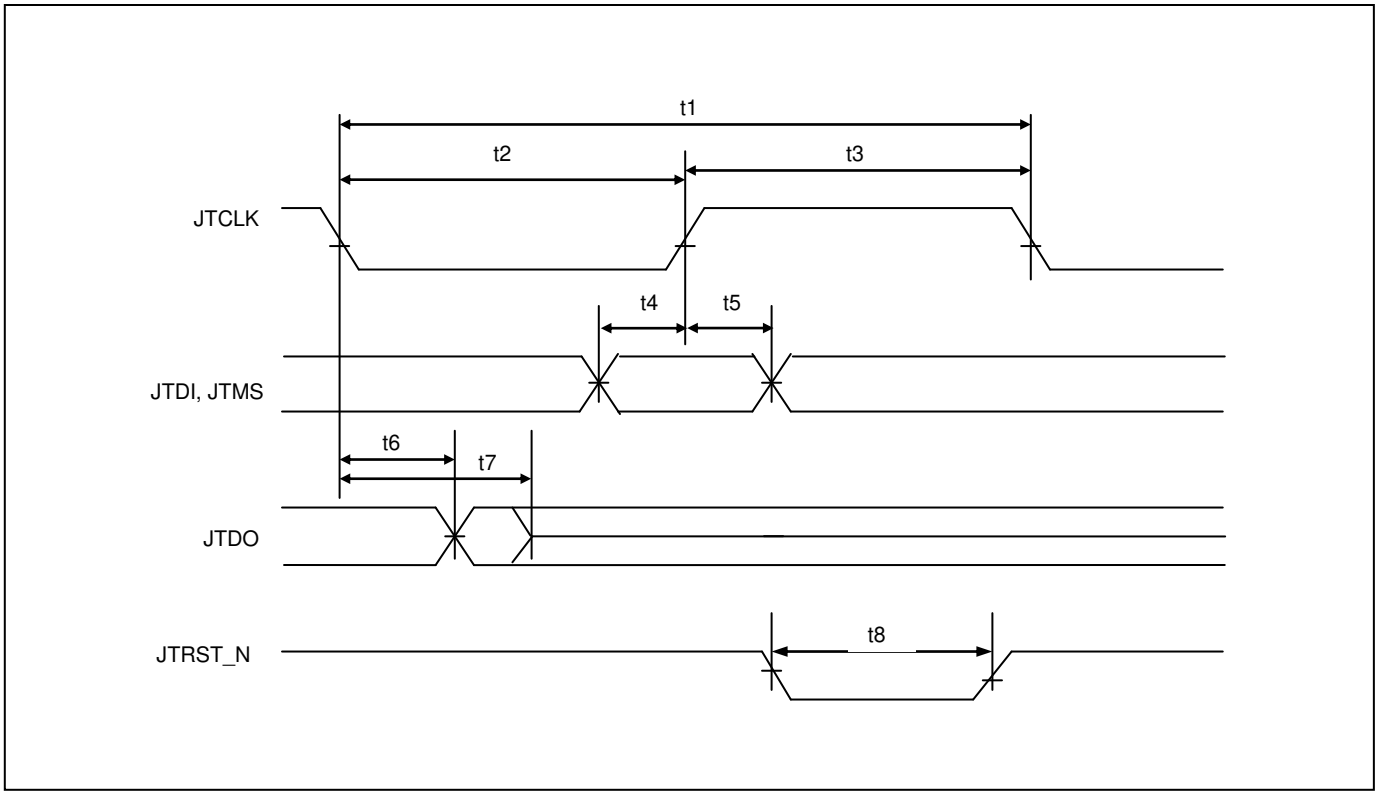
9.3.7 JTAG Interface AC Characteristics

Table 9-21. JTAG Interface Timing

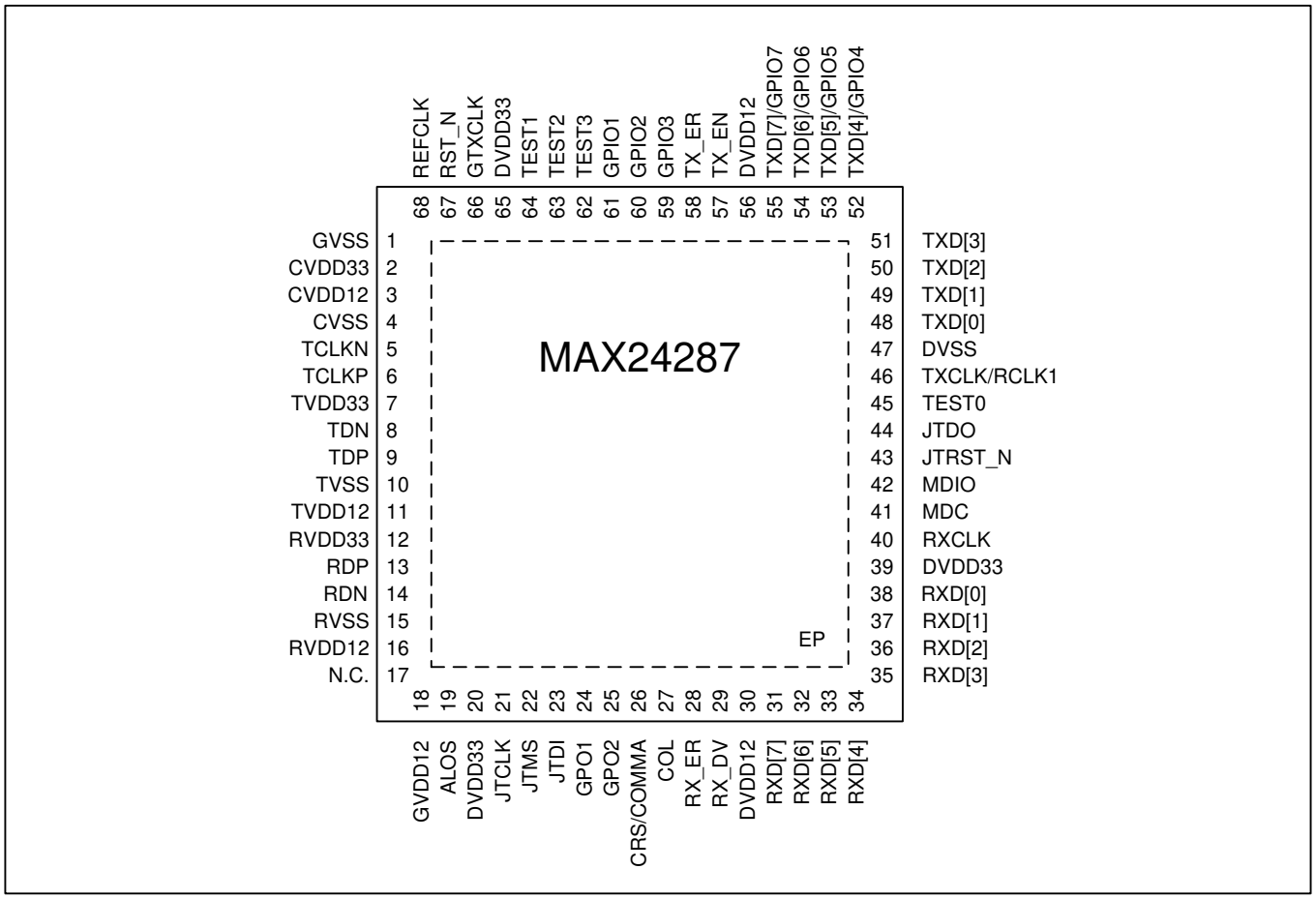
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1		1000		ns
JTCLK Clock High/Low Time (Note 1)	t2/t3	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4	50			ns
JTCLK to JTDI, JTMS Hold Time	t5	50			ns
JTCLK to JTDO Delay	t6	2		50	ns
JTCLK to JTDO High-Impedance Delay (Note 2)	t7			50	ns
JTRST_N Width Low Time	t8	100			ns

Note 1: Clock can be stopped high or low.
Note 2: All specifications in this table are guaranteed by design.

Figure 9-4. JTAG Timing Diagram



10. Pin Assignments



N.C. = Not connected internally.

11. Package and Thermal Information

Note: The exposed pad (EP) on the bottom of this package must be connected to the ground plane. EP also functions as a heatsink. Solder to the circuit-board ground plane to achieve the thermal specifications listed below.

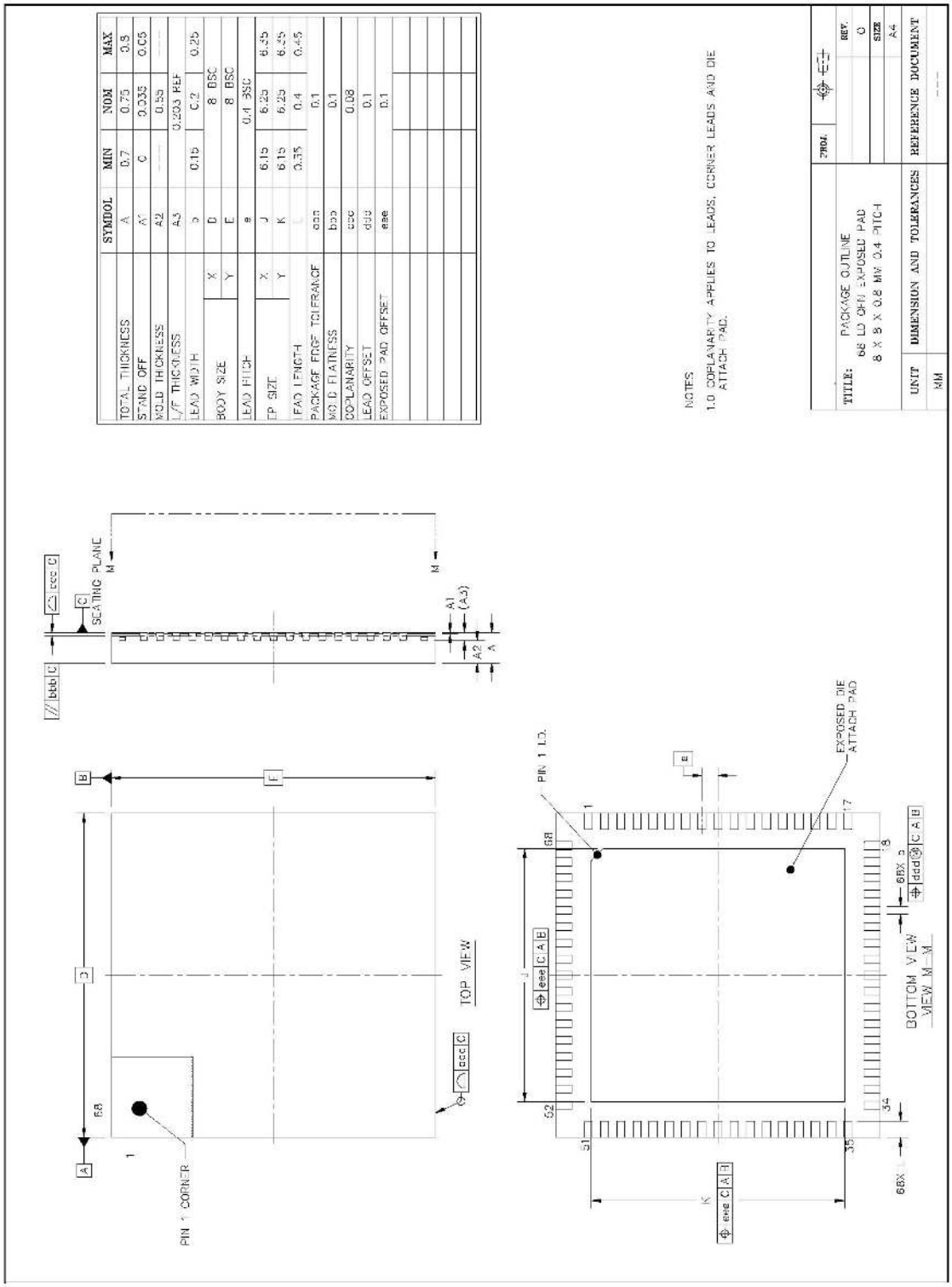


Table 11-1. Package Thermal Properties, Natural Convection

PARAMETER	CONDITIONS	MIN	TYP	MAX
Ambient Temperature	Note 1	-40°C		+85°C
Junction Temperature		-40°C		+125°C
Theta-JA (θ_{JA})	Note 2		20.2°C/W	
Theta-JC (θ_{JC})			1 °C/W	

Note 1: The package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.
Note 2: Theta-JA (θ_{JA}) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

12. Data Sheet Revision History

REVISION DATE	DESCRIPTION
2011-07	Initial release
2012-04	Reformatted for Microsemi. No content change.
2012-06	In the paragraph before Table 6-3, added a note to indicate that when RX_ER and RXD[7:4] are all high at reset the device enters factory test mode.
2012-07	Added section 6.13.
2012-09	In section 10 renamed N.C. pins 45, 64, 63, and 62 to TEST0 through TEST3, respectively. In Table 5-2 added rows for TEST0 through TEST3 pin descriptions.
2012-10	Deleted or edited statements that said or implied that microprocessor interaction over the MDIO interface is optional. Changed the description of PAGESEL.PAGE to list 10=page 2 and 11=page 3 and documented that PAGESEL bit 4 must be set to 1 for proper operation. Added section 6.14, Startup Procedure. Added register definition for PTPCR1. Updated Table 8-2 to show correct device code and revision values.
2013-01	Deleted section 6.13 because the recommendation there is no longer needed when the startup procedure in section 6.14 is followed. In section 9.3.1, loosened input REFCLK duty cycle spec from 48% min, 52% max to 40% min, 60% max and added Note 1. In Table 11-1 added Theta-JC spec. In Table 5-2 added a sentence to the REFCLK pin description to say that it is internally biased with a 10kΩ resistor to 1.2V.
2016-02	Redid section 11 to include the package outline drawing instead of referring to a separate document.
2016-04	In the JIT_DIAG.JIT_PAT description, corrected the 001 decode text from Annex 36A.4 to Annex 36A.1.
2016-11	In Table 5-4 clarified that JTRST_N should be held low during power-up.

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