AUDIO CODEC WITH USB INTERFACE, MONO MICROPHONE INPUT AND STEREO HEADPHONE OUTPUT

FEATURES

- On-Chip USB Interface:
  - With Full-Speed Transceivers
  - Fully Compliant with USB 2.0 Specification
  - Certified By USB-IF
  - Partially Programmable Descriptors
  - Adaptive Isochronous Transfer for Playback
  - Asynchronous Isochronous Transfer for Record
  - Bus Powered
- 16-Bit Delta-Sigma ADC and DAC
- Sampling Rate:
  - 8, 11.025, 16, 22.05, 32, 44.1, 48 kHz
- On-Chip Clock Generator:
  - With Single 6-MHz Clock Source
- Mono ADC with Microphone Input
  - Analog Performance at V_{BUS} = 5 V:
    - THD+N: 0.01%
    - SNR: 92 dB
    - Dynamic Range: 90 dB
  - Decimation Digital Filter
    - Pass-Band Ripple: ±0.05 dB
    - Stop-Band Attenuation: –65 dB
  - Single-Ended Voltage Input
  - Antialiasing Filter Included
  - Digital HPF Included
  - Microphone Bias, Microphone Amplifier, and Input PGA
- Stereo DAC With Headphone Output
  - Analog Performance at V_{BUS} = 5.0 V:
    - THD+N: 0.01% (R_L > 10 kΩ)
    - THD+N: 0.02% (R_L = 32 Ω)
    - SNR: 92 dB
    - Dynamic Range: 90 dB
    - PO: 13 mW (R_L = 32 Ω)
    - PO: 25 mW (R_L = 16 Ω)
  - Oversampling Digital Filter
    - Pass-Band Ripple: ±0.1 dB
    - Stop-Band Attenuation: –43 dB
    - Single-Ended Voltage Output
    - Analog LPF Included
    - Sidetone PGA, Output PGA, and HP Amplifier
- Multifunctions:
  - Suspend, Playback, and Record Status Flag
  - Microphone Amplifier, Mute, and Gain Control
- Pop/Click Noise Free
- Single Power Supply: 5 V Typ (V_{BUS})
- Package: 32-Pin TQFP

APPLICATIONS

- USB Headset
- USB Headphone
- USB Speaker
- USB Featured Consumer Audio Product
- USB Audio Interface Box
- USB Monitor
- Video Conference System

DESCRIPTION

The PCM2912 is the Texas Instruments single-chip, USB stereo audio CODEC with USB 2.0-compliant full-speed protocol controller and analog front end (AFE) function for headset application. The USB protocol controller works with no software code, but USB descriptors can be modified on request(1). The PCM2912 employs SpAct™ architecture, TI's unique system that recovers the audio clock from USB packet data. On chip analog PLLs with SpAct enables independent playback and record sampling rate with low clock jitters.

(1) The descriptor can be modified by changing a mask; contact your representative about the details.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		PCM2912	UNIT
Supply voltage	V_{BUS}	–0.3 to +6.5	V
Ground voltage differences: BGND, PGND, AGND, HGND, DGND		±0.1	V
Input voltage : V_{CCP}, V_{CCA}, V_{CCL}, V_{CCR}, V_{DD}		–0.3 to 4	V
Digital input voltage	$\overline{PLAY}$, $\overline{REC}$.	–0.3 to 6.5	V
	D+, D–, XTI, XTO, MMUTE, TEST0, TEST1, POWER, MAMP, $\overline{SSPND}$	–0.3 to 4	V
Analog input voltage	MBIAS, V_{IN}, V_{COM1}, V_{COM2}, $V_{OUT}L$, $V_{OUT}R$, FR, FL	–0.3 to 4	V
Input current (any pins except supplies)		±10	mA
Ambient temperature under bias		–40 to 125	°C
Storage temperature		–55 to 150	°C
Junction temperature		150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BUS}	Supply voltage	4.35	5.00	5.25	V
	Analog input voltage, full scale (–0 dB)		0.43 V_{CCA}		Vp-p
	Digital input logic family		TTL		
	Digital iInput clock frequency	5.997	6.000	6.003	MHz
	Analog output load resistance	32			Ω
	Analog output load capacitance			100	pF
	Digital output load capacitance			10	pF
T_A	Operating free-air temperature	–25		70	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM2912PJT			UNIT
			MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT						
	Host interface	Apply USB Revision 2.0, full-speed				
	Audio data format	USB isochronous data format				
INPUT LOGIC						
V_{IH}	Input logic level		2		3.3	VDC
V_{IL}					0.8	
I_{IH} (1)(2)	Input logic current	V_{IN} = 3.3 V			±10	µA
I_{IL} (1) (2)		V_{IN} = 0 V			±10	
I_{IH} (3)		V_{IN} = 3.3 V		65	100	µA
I_{IL} (3)		V_{IN} = 0 V			±10	
OUTPUT LOGIC						
V_{OH} (1)	Output logic level	I_{OH} = –10 mA	2.9			VDC
V_{OL} (1)		I_{OL} = 10 mA			0.3	
V_{OH} (4)		I_{OH} = –2 mA	2.8			
V_{OL} (4)		I_{OL} = 2 mA			0.5	
V_{OL} (5)		I_{OL} = 8 mA			0.5	
I_{OH} (5)	Output leak current	V_{IN} = 5 V			±10	µA
CLOCK FREQUENCY						
	Input clock frequency, XTI		5.997	6.000	6.003	MHz
MICROPHONE BIAS						
	Output voltage			0.75 V_{CCA}		VDC
	Output current			2		mA
	Output noise	R_L = 1 kΩ		5		µVrms

(1) Pins 3, 4: D–, D+.
(2) Pins 8, 23, 24, 27, 28: XTI, MAMP, POWER, TEST1, TEST0
(3) Pin 30: MMUTE
(4) Pins 7, 29: XTO, $\overline{\text{SSPND}}$
(5) Pins 31, 32: $\overline{\text{REC}}$, $\overline{\text{PLAY}}$.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER	TEST CONDITIONS	PCM2912PJT			UNIT
		MIN	TYP	MAX	
ADC CHARACTERISTICS					
Resolution			16		Bits
Audio data channel			1		channel
Sampling frequency			8, 11.025, 16, 22.05, 32, 44.1, 48		kHz
DYNAMIC PERFORMANCE(6)					
THD+N	V_{IN} = –1 dB of 0.43 V_{CCA}		0.01%	0.02%	
Dynamic range	A-weighted	82	90		dB
S/N ratio	A-weighted	84	92		dB
DC ACCURACY					
Gain error			±2	±10	% of FSR
Bipolar zero error			±0		% of FSR
ANALOG INPUT					
Input voltage			0.43 V_{CCA}		Vp-p
Center voltage			0.5 V_{CCA}		V
Antialiasing filter frequency response	–3 dB		150		kHz
	f_{IN} = 20 kHz		–0.08		dB
MICROPHONE AMPLIFIER					
Gain		0		20	dB
Input impedance			20		kΩ
INPUT PGA					
Gain range		–12		30	dB
Gain step size			1		dB
DIGITAL FILTER PERFORMANCE					
Pass band				0.454 f_S	Hz
Stop band		0.583 f_S			Hz
Pass-band ripple				±0.02	dB
Stop-band attenuation		–65			dB
Delay time			17.4/f_S		s
HPF frequency response	–3 dB		0.078 f_S		MHz

(6) f_{IN} = 1 kHz, using Audio Precision™ System Two™, RMS mode with 20 kHz LPF, 400 Hz HPF in calculation. Mic amp = 0 dB, PGA = 0 dB.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER	TEST CONDITIONS	PCM2912PJT			UNIT
		MIN	TYP	MAX	
DAC CHARACTERISTICS					
Resolution			16		Bits
Audio data channel			1, 2		channel
Sampling frequency			8, 11.025, 16, 22.05, 32, 44.1, 48		kHz
DYNAMIC PERFORMANCE(7)					
THD+N	R_L > 10 kΩ, V_{OUT} = 0 dB of 0.6 V_{CCA}		0.01%	0.02%	
	R_L = 32 Ω, V_{OUT} = 0 dB of 0.55 V_{CCA}		0.02%	0.05%	
Dynamic range	EIAJ, A-Weighted	82	90		dB
S/N ratio	EIAJ, A-Weighted	84	92		dB
Channel separation	R_L > 10 kΩ	80	88		dB
DC ACCURACY					
Gain mismatch channel-to-channel			±2	±10	% of FSR
Gain error			±2	±10	% of FSR
Bipolar zero error			±3		% of FSR
ANALOG OUTPUT					
Output voltage	R_L > 10 kΩ		0.6 V_{CCA}		Vp-p
	R_L = 32 Ω		0.55 V_{CCA}		
Center voltage			0.5 V_{CCA}		V
Output power	R_L = 32 Ω		13		mW
	R_L = 16 Ω		25		
Load impedance (AC coupling)	LINE	10			kΩ
	HEADPHONE	16	32		Ω
LPF frequency response	–3 dB		140		kHz
	f = 20 kHz		–0.1		dB
SIDETONE PROGRAMMABLE ATTENUATOR					
Gain range		–76		0	dB
Gain step size			1		dB
OUTPUT PROGRAMMABLE ATTENUATOR					
Gain range		–76		0	dB
Gain step size			1		dB
ANALOG LOOPBACK PERFORMANCE(8)					
THD+N	R_L > 10 kΩ, V_{IN} = 0 dB of 0.43 V_{CCA}		0.01%	0.02%	
	R_L = 32 Ω, V_{IN} = 0 dB of 0.43 V_{CCA}		0.02%	0.05%	
Dynamic range	EIAJ, A-weighted	82	90		dB
S/N ratio	EIAJ, A-weighted	84	92		dB

(7) f_{OUT} = 1 kHz, using Audio Precision ™System Two ™, RMS mode with 20 kHz LPF, 400 Hz HPF. Output attenuator = 0 dB, Sidetone = Mute.
(8) MIC Amp = 0 dB, Sidetone attenuator = 0 dB, Output attenuator = 0 dB.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

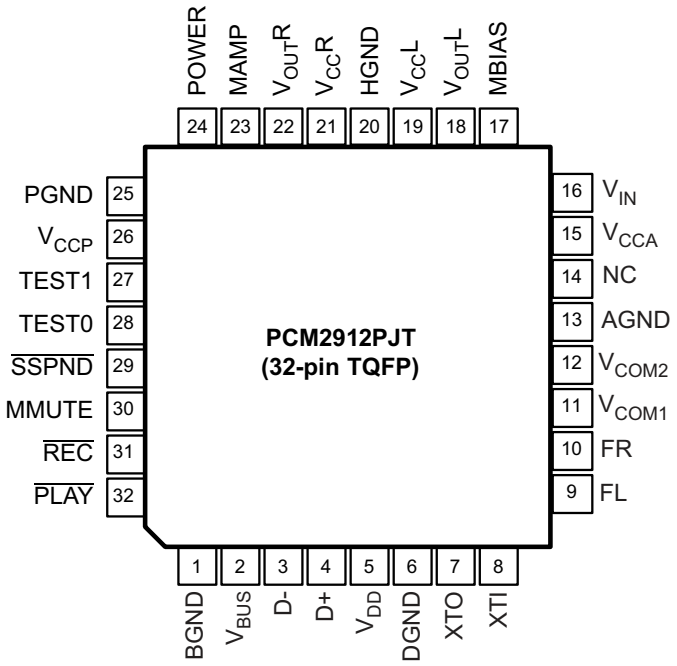
PARAMETER		TEST CONDITIONS	PCM2912PJT			UNIT
			MIN	TYP	MAX	
DIGITAL FILTER PERFORMANCE						
	Pass band				0.445 f_S	Hz
	Stop band		0.555 f_S			Hz
	Pass-band ripple				±0.1	dB
	Stop-band attenuation		–43			dB
	Delay time			14.3/f_S		s
POWER SUPPLY REQUIREMENTS						
V_{BUS}	Voltage range	Bus-powered	4.35	5.0	5.25	VDC
	Supply current	ADC, DAC operation (R_L = 32 Ω)		85	100	mA
		Suspend mode(9)		220	300	µA
	Power dissipation	ADC, DAC Operation		425	500	mW
		Suspend mode(9)		0.8	1	mW
V_{CCP},V_{CCL}, V_{CCR},V_{CCA}, V_{DD}	Internally generated power supply voltage(10)		3	3.3	3.6	VDC
TEMPERATURE RANGE						
	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance	32-pin TQFP		80		°C/W

(9) Under USB suspend state
(10) Pins 5, 15, 19, 21, 26: V_{DD}, V_{CCA}, V_{CCL}, V_{CCR}, V_{CCP}.

DEVICE INFORMATION

PIN ASSIGNMENTS

PCM2912
(TOP VIEW)

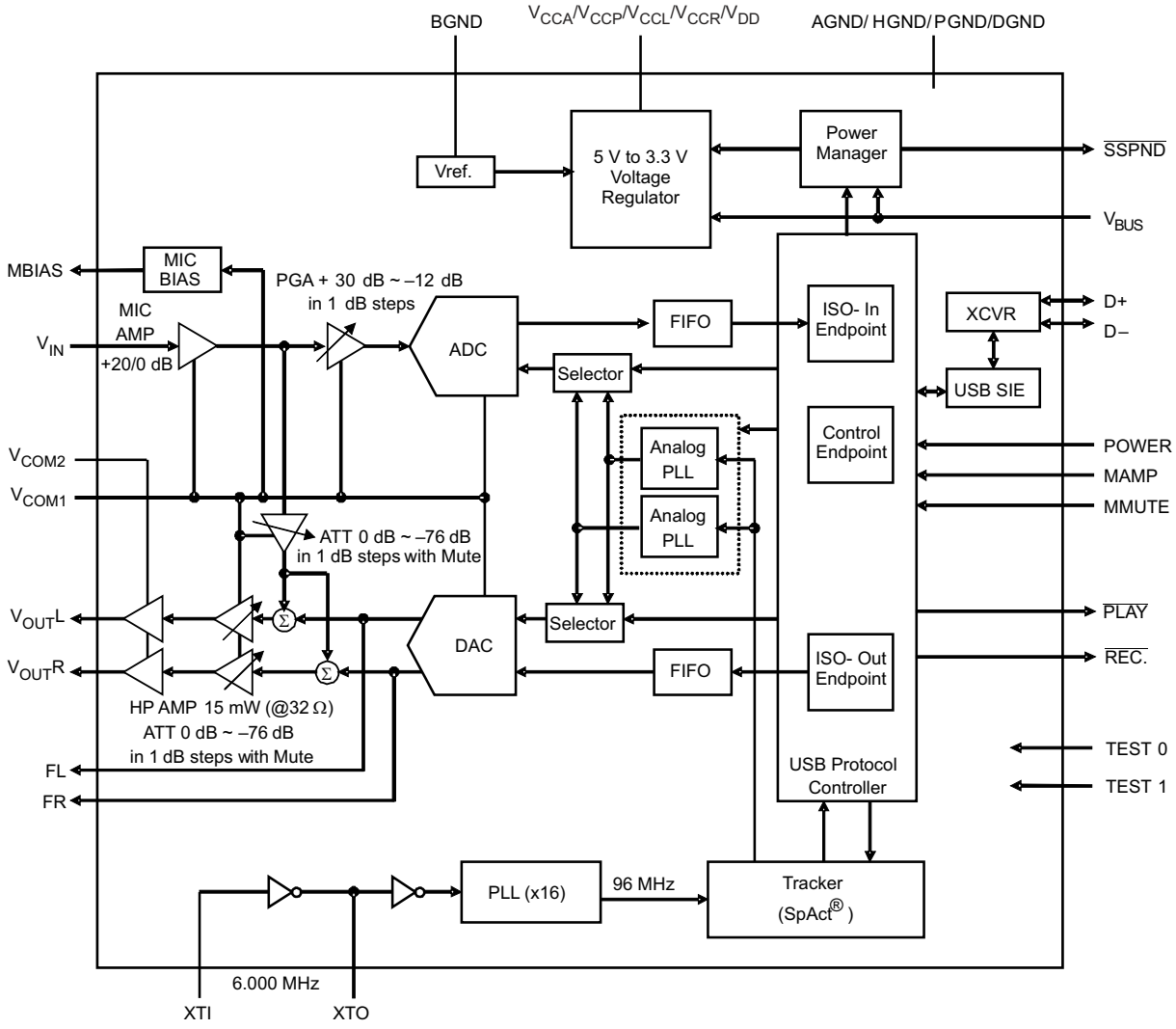


TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTIONS
NAME	PJT		
BGND	1	–	Reference for internal regulator.
V_{BUS}	2	–	Connect to USB power (V_{BUS})
D–	3	I/O	USB differential input/output minus (1)
D+	4	I/O	USB differential input/output plus (1)
V_{DD}	5	–	Digital power supply (2)
DGND	6		Digital ground
XTO	7	O	Crystal oscillator output
XTI	8	I	Crystal oscillator input (3)
FL	9	–	External filter pin of L-channel (optional)
FR	10	–	External filter pin of R-channel (optional)
V_{COM1}	11	–	Common voltage for ADC, DAC and analog front end (V_{CCA}/2). Decouple capacitor should be connected to AGND.
V_{COM2}	12	–	Common voltage for headphone (V_{CCA}/2). Decouple capacitor should be connected to AGND.
AGND	13	–	Analog ground
NC	14	–	Not connected
V_{CCA}	15	–	Analog power supply
V_{IN}	16	I	ADC microphone input
MBIAS	17	O	Microphone bias output (0.75 V_{CCA})
V_{OUT}L	18	O	Headphone output for L-channel
V_{CCL}	19	–	Analog power supply for headphone amplifier of L-channel (2)
HGND	20	–	Analog ground for headphone amplifier
V_{CCR}	21	–	Analog power supply for headphone amplifier of R-channel (2)
V_{OUT}R	22	O	Headphone output for R-channel
MAMP	23	I	Microphone preamplifier gain control (LOW: Preamplifier off, HIGH: Preamplifier on = +20 dB) (3)
POWER	24	I	Power consumption declaration select pin (LOW: 100 mA, HIGH: 500 mA) (3)
PGND	25	–	Analog ground for microphone bias, microphone amplifier, and PGA
V_{CCP}	26	–	Analog power supply for PLL (2)
TEST1	27	I	Test pin. Must be set to HIGH (3)
TEST0	28	I	Test pin. Must be set to LOW (3)
$\overline{\text{SSPND}}$	29	O	Suspend flag (LOW: Suspend, HIGH: Operational state)
MMUTE	30	I	Microphone mute control, active HIGH (LOW: Mute off, HIGH: Mute on) (4)
$\overline{\text{REC}}$	31	O	Status output for record (LOW: Record, FLASH: Mute on recode, HIGH: Stop) (5)
$\overline{\text{PLAY}}$	32	O	Status output for playback (LOW: Playback, FLASH: Mute on playback, HIGH: Stop) (5)

(1) LV-TTL level
(2) Connect decouple capacitor to corresponding ground.
(3) 3.3-V CMOS level input.
(4) 3.3-V CMOS level input with internal pulldown.
(5) 5 V tolerant, open-drain.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

ADC Digital Decimation Filter Frequency Response

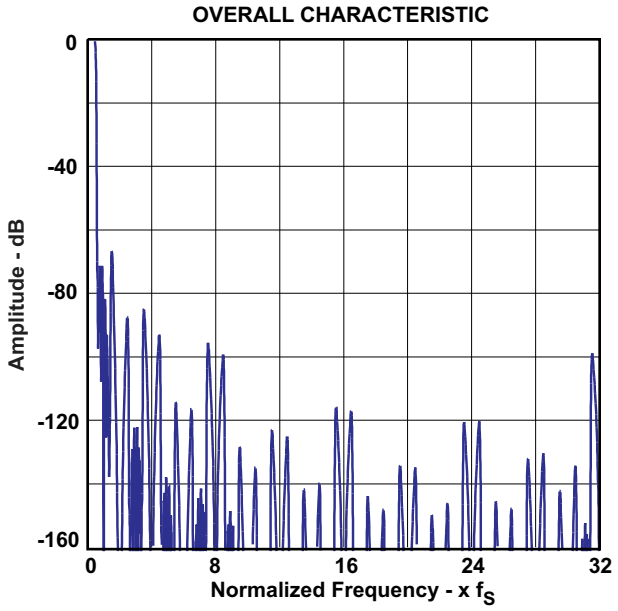


Figure 1.

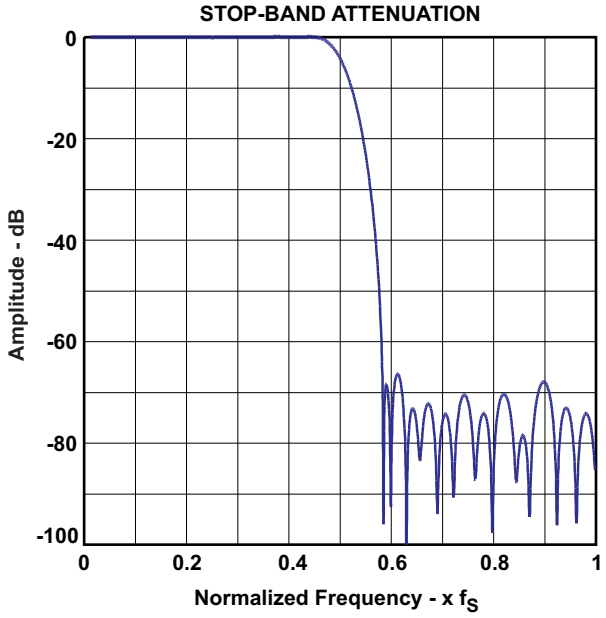


Figure 2.

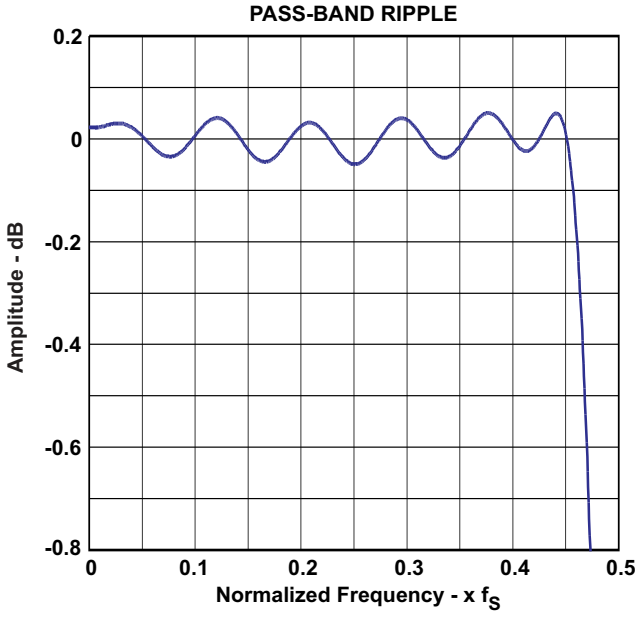


Figure 3.

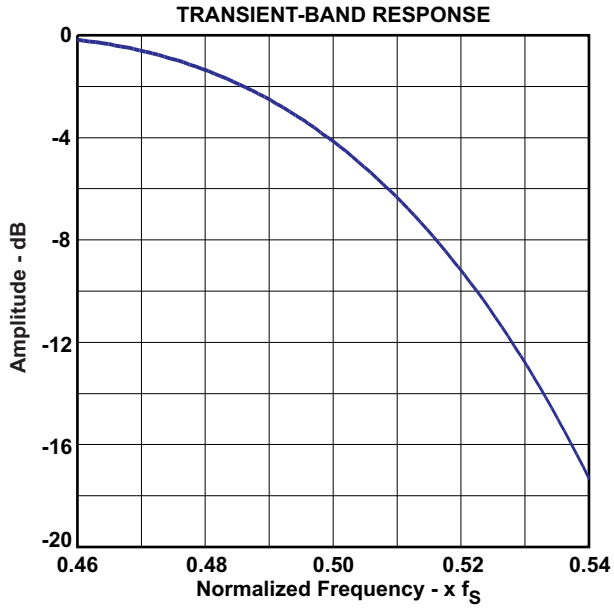


Figure 4.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

ADC Digital High-Pass Filter Frequency Response

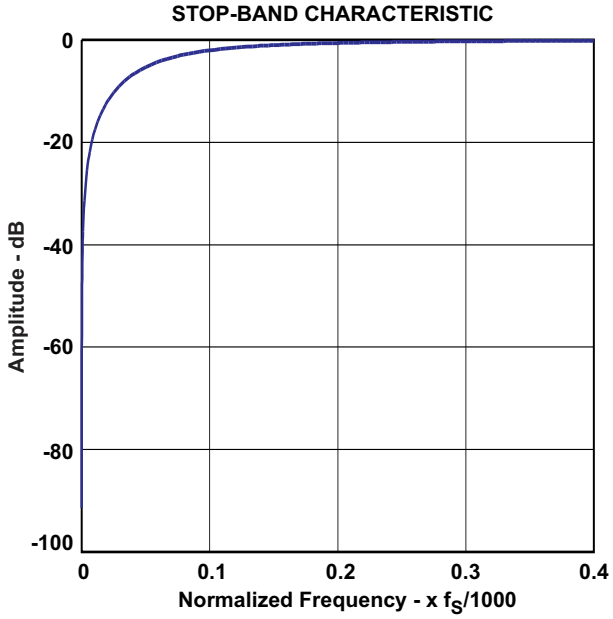


Figure 5.

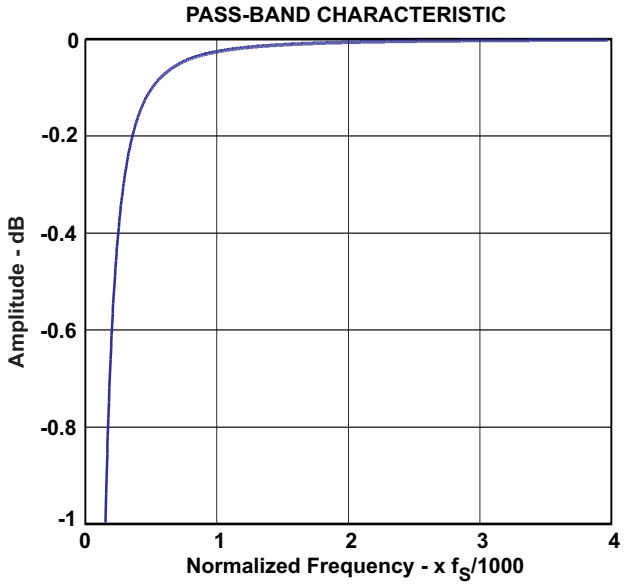


Figure 6.

ADC Analog Antialiasing Filter Frequency Response

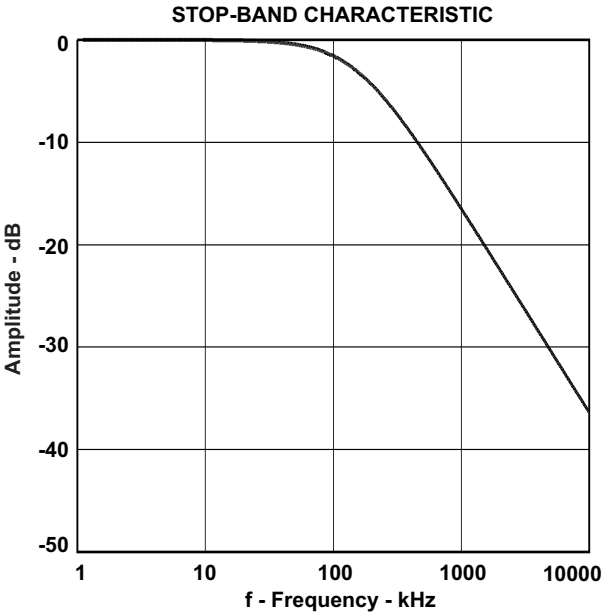


Figure 7.

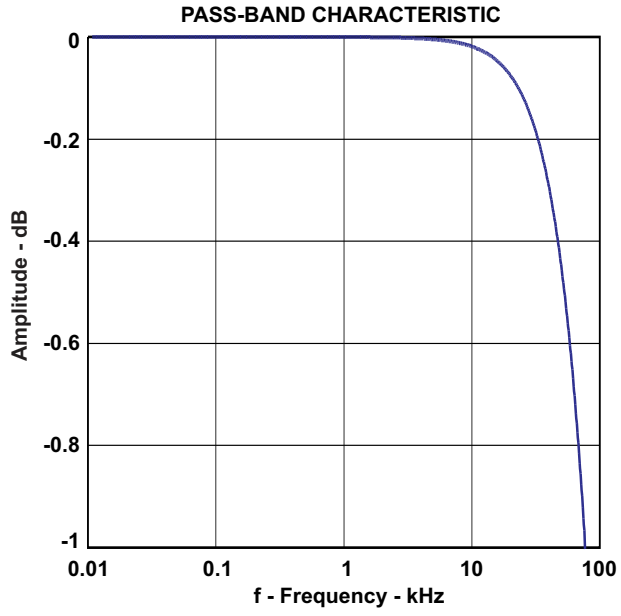


Figure 8.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

DAC Digital Interpolation Filter Frequency Response

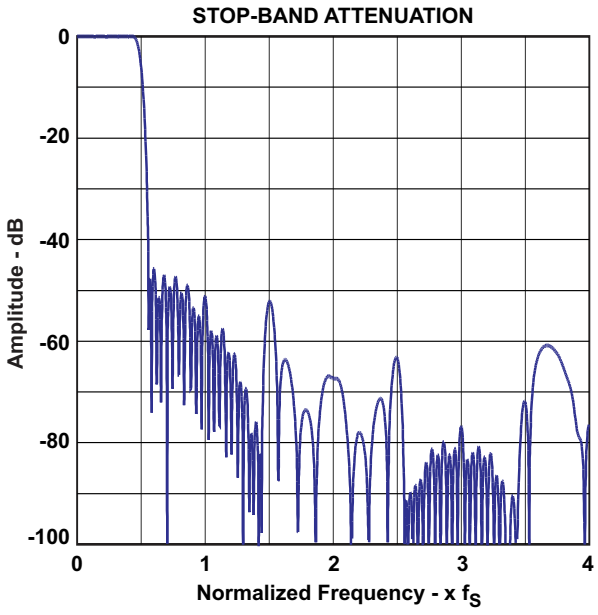


Figure 9.

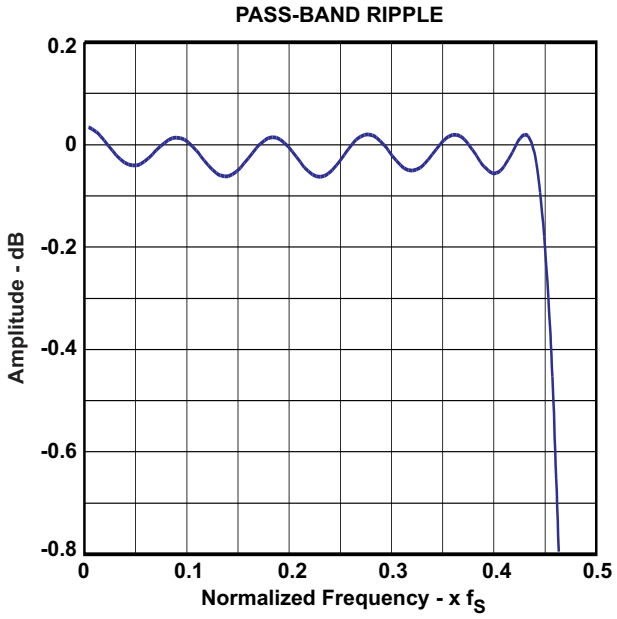


Figure 10.

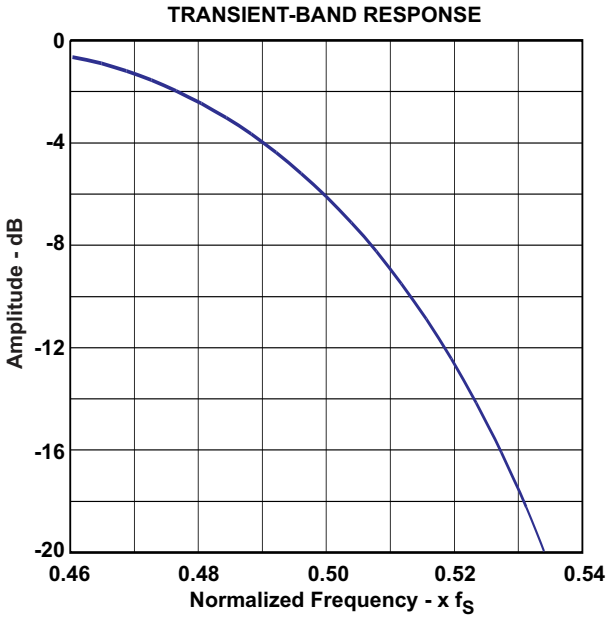


Figure 11.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

DAC Analog FIR Filter Frequency Response

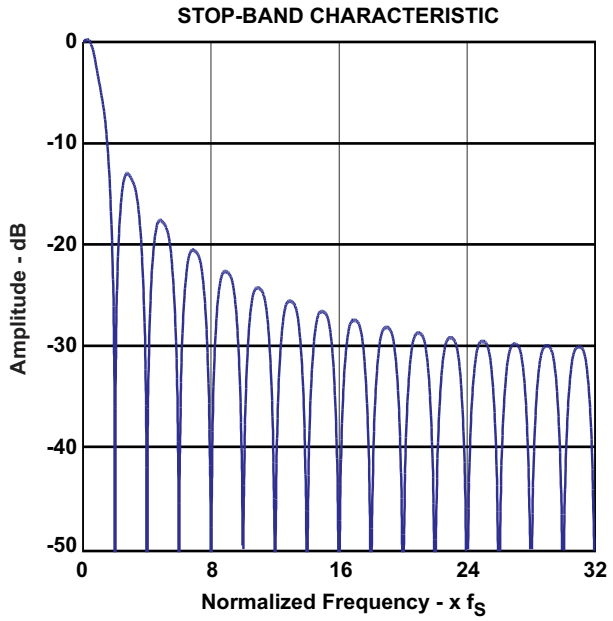


Figure 12.

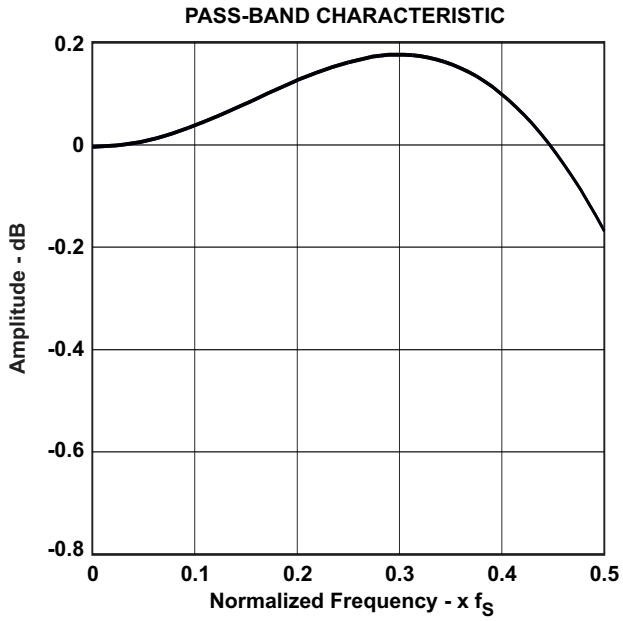


Figure 13.

DAC Analog Low-Pass Filter Frequency Response

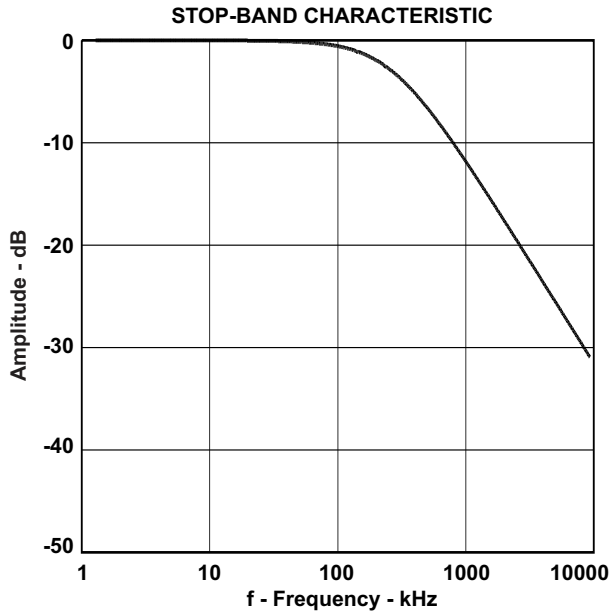


Figure 14.

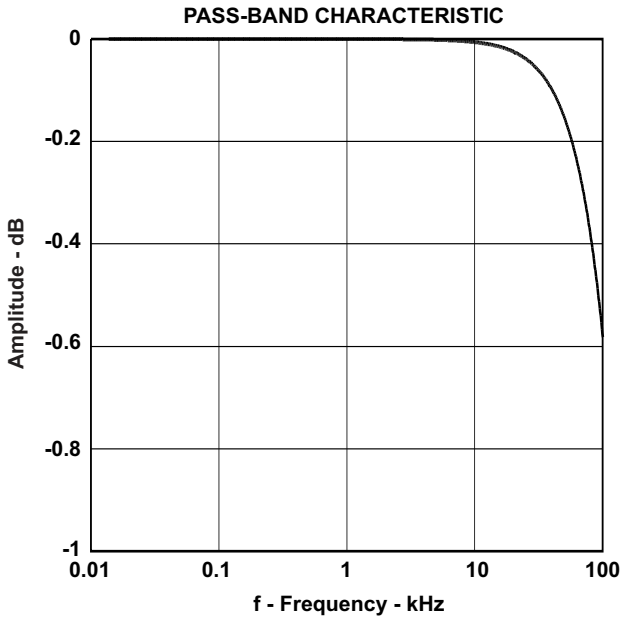


Figure 15.

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

ADC

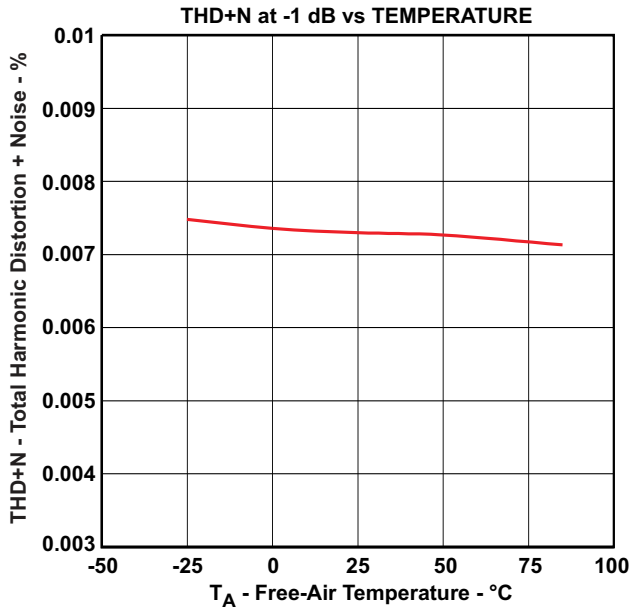


Figure 16.

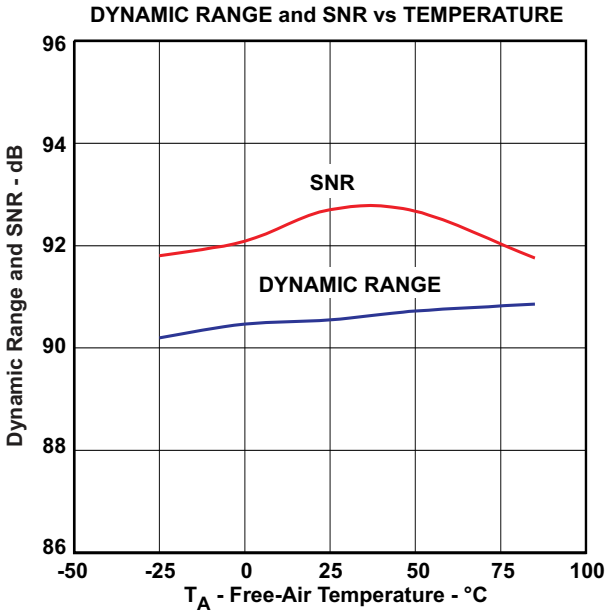


Figure 17.

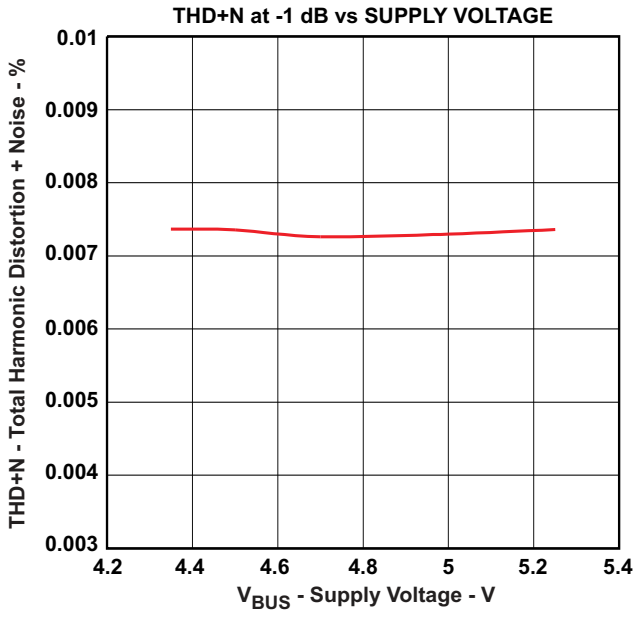


Figure 18.

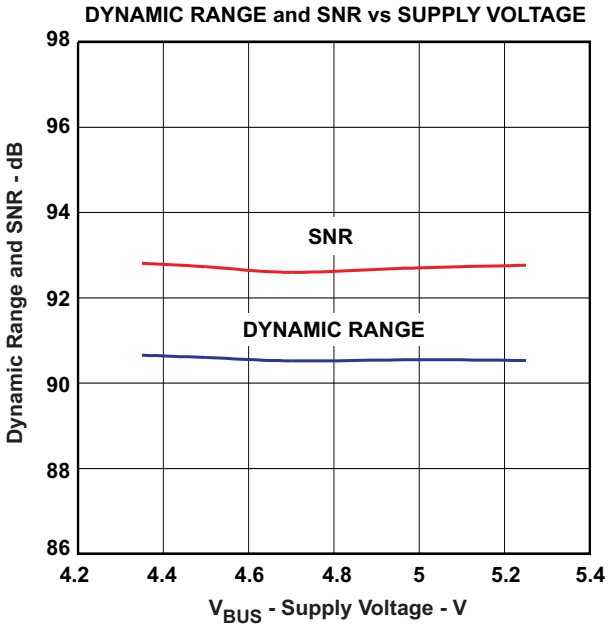


Figure 19.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

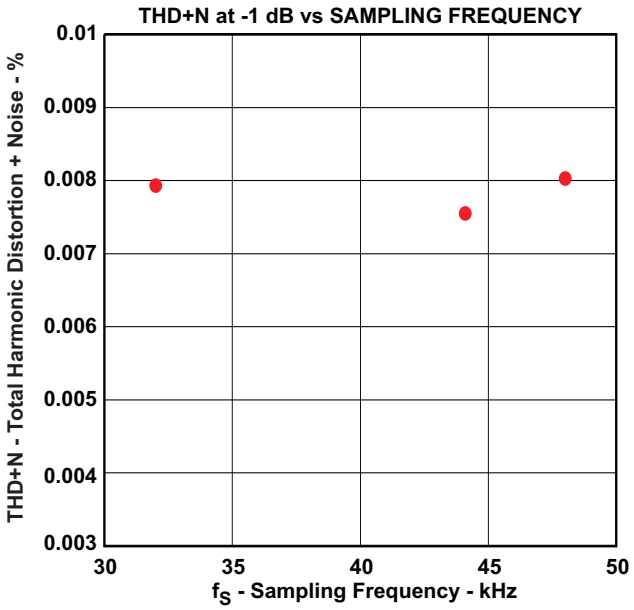


Figure 20.

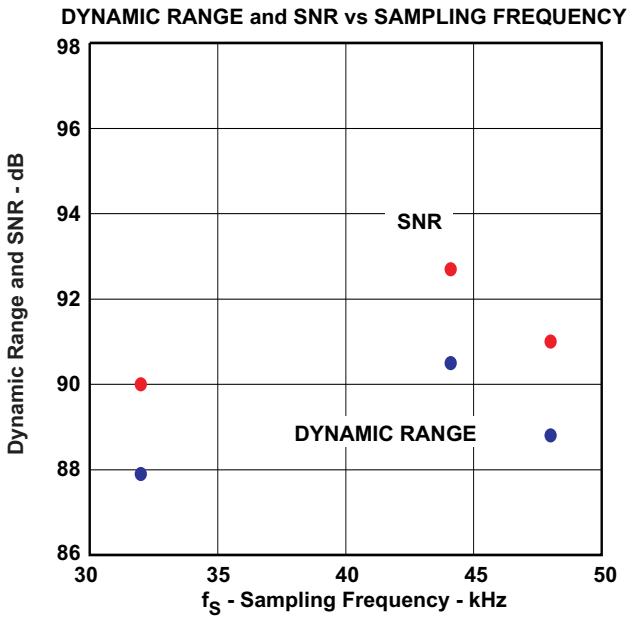


Figure 21.

DAC

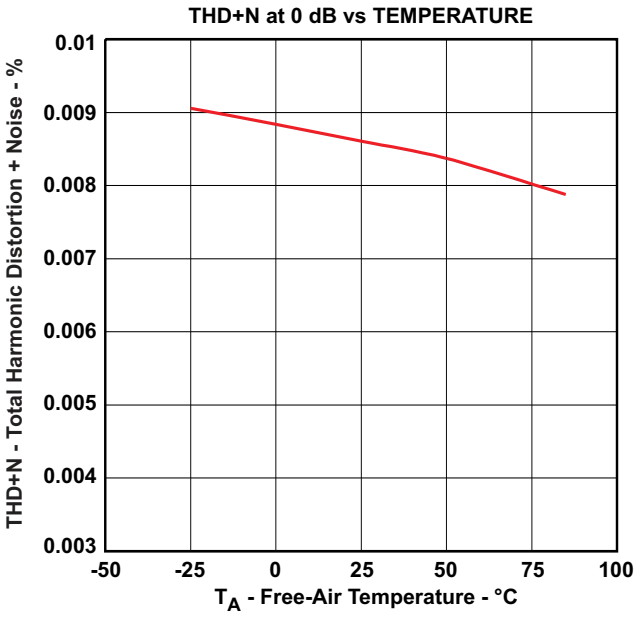


Figure 22.

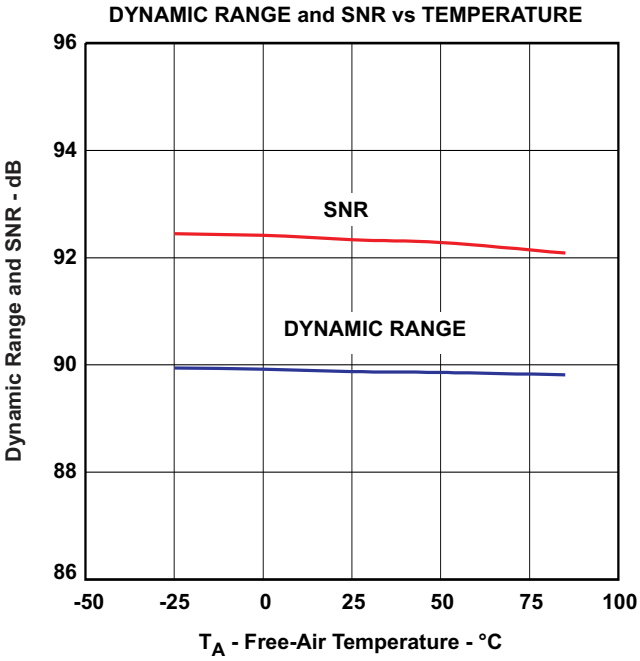


Figure 23.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

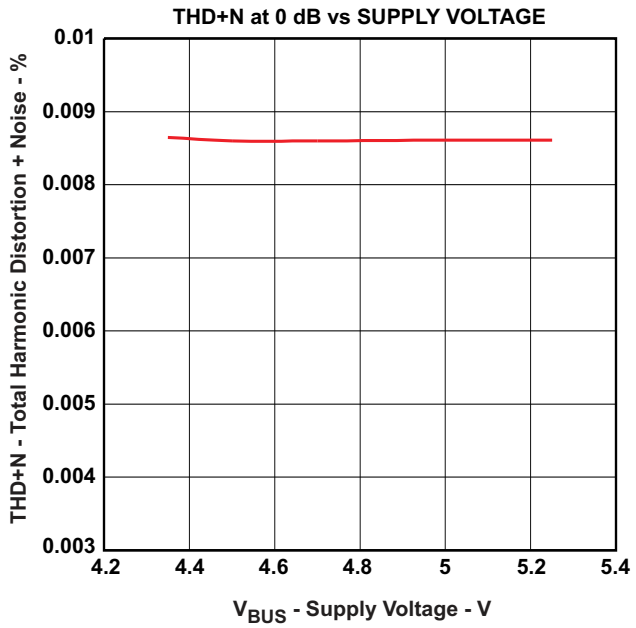


Figure 24.

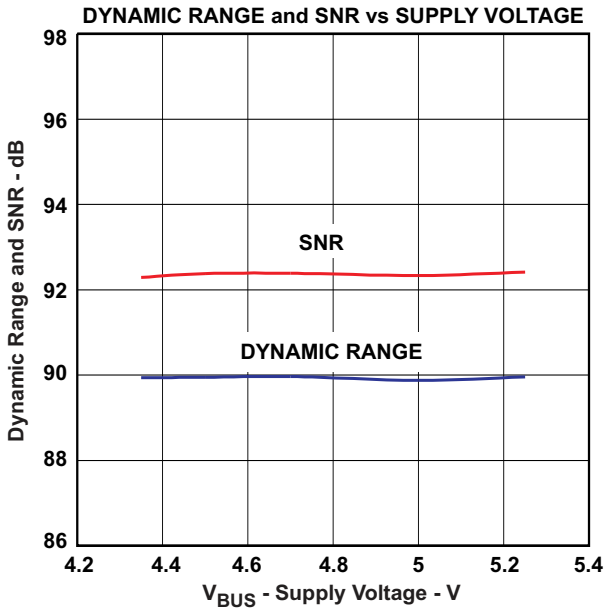


Figure 25.

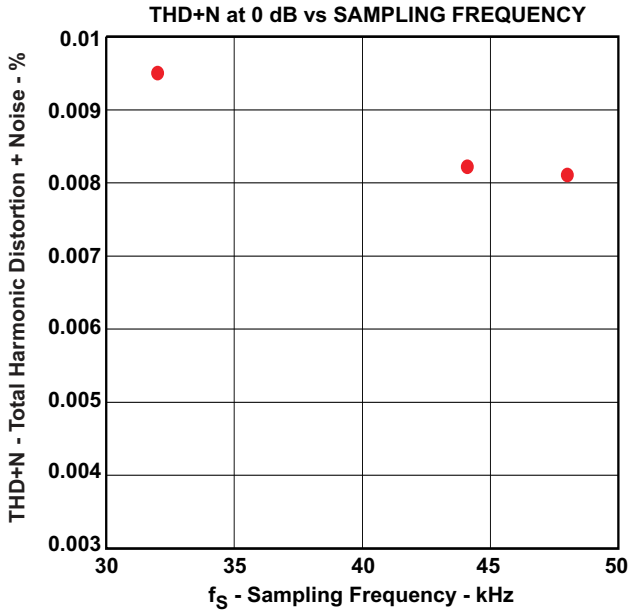


Figure 26.

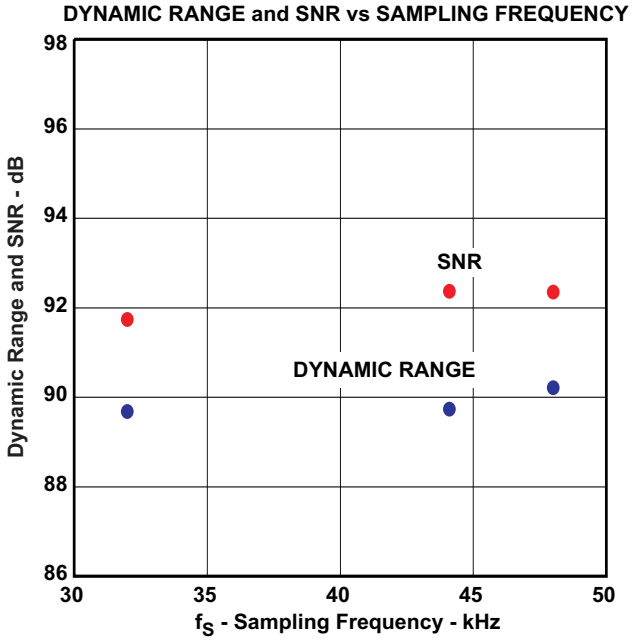


Figure 27.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

Supply Current

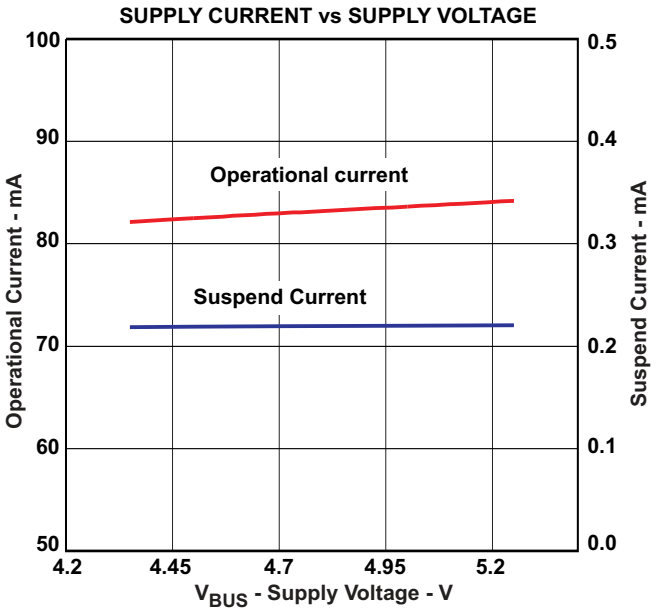


Figure 28.

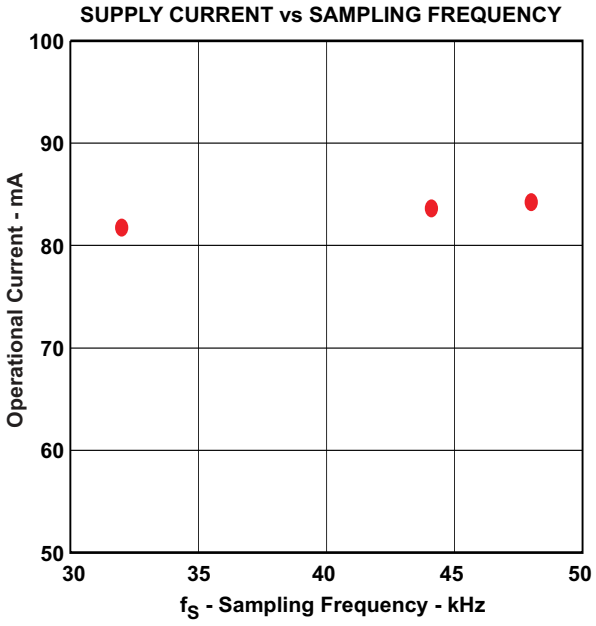


Figure 29.

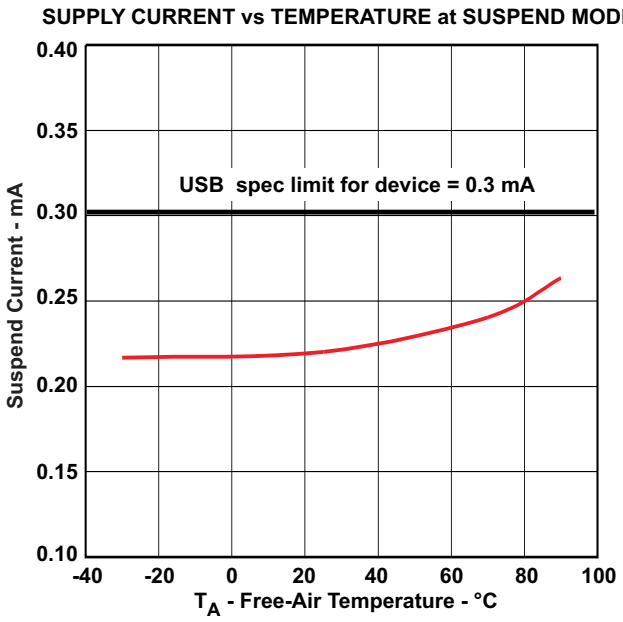


Figure 30.

USB INTERFACE

Control data and audio data are transferred to the PCM2912 via D+ (pin 4) and D– (pin 3). All data to/from the PCM2912 are performed in full-speed. The following information is described in the device descriptor. The device descriptor can be modified on request.

Table 1. Device Descriptor

USB revision	2.0 compliant
Device class	0x00 (device defined interface level)
Device sub class	0x00 (not specified)
Device protocol	0x00 (not specified)
Max packet size for endpoint 0	8 byte
Vendor ID	0x08BB
Product ID	0x2910
Device release number	0x0100 (1.00)
Number of configurations	1
Vendor string	String #1 (refer to Table 3)
Product string	String #2 (refer to Table 3)
Serial number	Not supported

The following information is described in the configuration descriptor. The configuration descriptor can be modified on request.

Table 2. Configuration Descriptor

Interface	3 interfaces
Power attribute	0x80 (Bus powered, no remote wakeup)
Max power	0x32 (100 mA at POWER=Low) / 0xFA (500mA at POWER = High)

The following information is described in the string descriptor. The string descriptor can be modified on request.

Table 3. String Descriptor

#0	0x0409
#1	Burr-Brown from TI
#2	USB audio CODEC

Device Configuration

Figure 31 illustrates USB audio function topology. The PCM2912 has three interfaces. Each interface is constructed by some alternative settings.

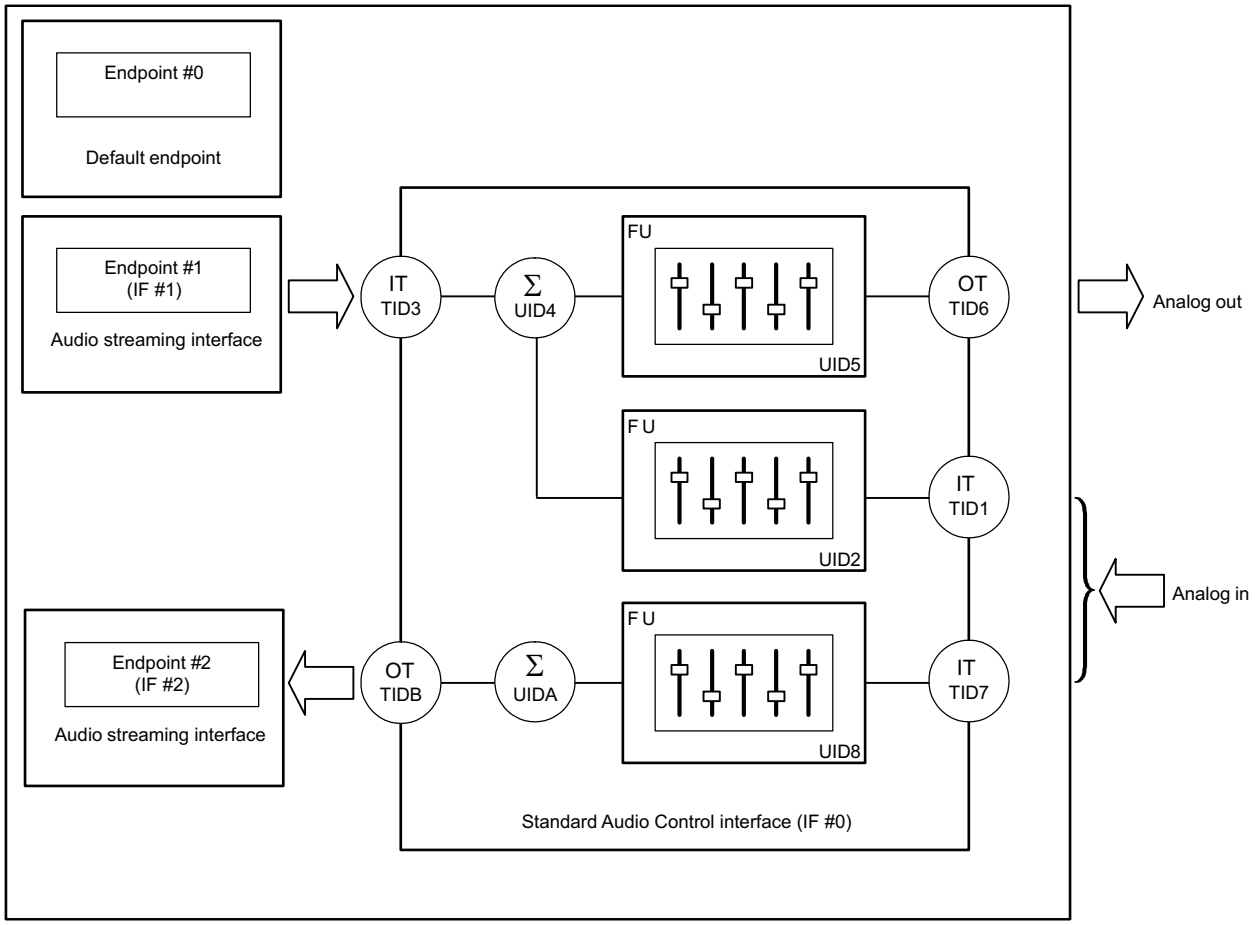


Figure 31. USB Audio Function Topology

Interface #0

Interface #0 is for control interface. Alternative setting #0 is the only possible setting for interface #0. Alternative setting #0 describes the standard audio control interface. Audio control interface is constructed by a terminal. The PCM2912 has ten terminals as follows.

- Input Terminal (Terminal ID#1) for audio analog input for sidetone
- Feature Unit (Unit ID#2) for sidetone PGA
- Input Terminal (Terminal ID#3) for isochronous-out stream
- Mixer Unit (Unit ID#4) for sidetone mixing
- Feature Unit (Unit ID#5) for analog output PGA
- Output Terminal (Terminal ID#6) for audio analog output
- Input Terminal (Terminal ID#7) for audio analog input
- Feature Unit (Unit ID#8) for analog input PGA
- Mixer Unit (Unit ID#A) for analog input
- Output Terminal (Terminal ID#B) for isochronous-in stream

The Input Terminal #3 is defined as *USB stream* (terminal type 0x0101). The Input Terminal #3 can accept 2-channel audio streams constructed by Left and Right channels. The Output Terminal #6 is defined as a *speaker* (terminal type 0x0301). The Input Terminals #1 and #7 are defined as *Microphone* (terminal type 0x0201). Physically, these two input terminals are the same input, but logically duplicated. The Output Terminal #B is defined as a *USB stream* (terminal type 0x0101). The Output Terminal #B is a single-channel audio stream. The Mixer Unit #4 mixes up the analog input (sidetone) and the audio data of the DAC. The Mixer Unit #A is placed in front of the Output Terminal #B. The Mixer Unit #A has no impact on record data. The Mixer Units #4 and #A do not have programming capability.

The Feature Unit #5 supports the following sound control features for analog outputs.

- Volume control
- Mute control

The built-in volume controller can be manipulated by an audio-class-specific request from 0 dB to –76 dB in steps of 1 dB. An individual (L and R) channel can be set for different values. The built-in mute controller can be manipulated by an audio-class-specific request. Only a master mute control request is acceptable.

The Feature Unit #2 supports the following sound control features for analog input (sidetone).

- Volume control
- Mute control

The built-in volume controller can be manipulated by an audio-class-specific request from 0 dB to –76 dB in 1-dB steps. The only master volume control is acceptable. The built-in mute controller can be manipulated by audio-class-specific request. The only master mute control request is acceptable.

The Feature Unit #8 supports the following sound control features for analog input (microphone record input).

- Volume control
- Mute control

The built-in analog volume controller can be manipulated by an audio-class-specific request from +30 dB to –12 dB in 1-dB steps. The built-in mute controller can be manipulated by an audio-class-specific request. The only master mute control request is acceptable.

Interface #1

Interface #1 is for audio streaming data-out interface. Interface #1 has the following three alternative settings. Alternative setting #0 is the zero bandwidth setting. All other alternative settings are operational settings.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero band width				
01	16 bit	Stereo	2s complement (PCM)	Adaptive	8, 11.025, 16, 22.05, 32, 44.1, 48
02	16 bit	Mono	2s complement (PCM)	Adaptive	8, 11.025, 16, 22.05, 32, 44.1, 48

Interface #2

Interface #2 is for audio streaming data in interface. Interface #2 has the following two alternative settings. Alternative setting #0 is the Zero Band Width setting. Alternative setting #1 is an operational setting.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero band width				
01	16 bit	Mono	2s complement (PCM)	Asynchronous	8, 11.025, 16, 22.05, 32, 44.1, 48

Endpoints

The PCM2912 has three endpoints as follows.

- Control endpoint (EP #0)
- Isochronous-out audio data stream endpoint (EP #1)
- Isochronous-in audio data stream endpoint (EP #2)

The control endpoint is a default endpoint. The control endpoint is used to control all functions of the PCM2912 by the standard USB request and USB audio-class-specific request from the host. Isochronous-out audio data stream endpoint is an audio sink endpoint, which receives the PCM audio data. The isochronous-out audio data stream endpoint accepts the adaptive transfer mode. Isochronous-in audio data stream endpoint is an audio source endpoint, which transmits the PCM audio data. The isochronous-in audio data stream endpoint uses synchronous transfer mode.

Internal Regulator

All required power sources are generated by five internal regulators.

Each regulator generates 3.3 V (typical, without load) from V_{BUS} (pin 2). Each regulator has an output pin and ground return pin as follows, and this pair must be decoupled with an appropriate capacitor. Note that this capacitance affects inrush-current limitation. One band-gap reference circuit supplies reference voltage for all regulators. BGND (pin 1) is provided for reference ground of the band-gap reference.

SUPPLIED CIRCUIT	OUTPUT	RETURN
Digital	V_{DD} (pin 5)	DGND (pin 6)
Analog	V_{CCA} (pin 15)	AGND (pin 13)
Headphone (L-ch)	V_{CCL} (pin 19)	HGND (pin 20)
Headphone (R-ch)	V_{CCR} (pin 21)	HGND (pin 20)
PLL	V_{CCP} (pin 26)	PGND (pin 25)

Clock and Reset

The PCM2912 requires a 6-MHz (±500 ppm) clock for USB function and audio function, which can be generated by a built-in crystal oscillator with a 6-MHz crystal resonator. The 6-MHz crystal resonator must be connected to XTI (pin 8) and XTO (pin 7) with one high (1-MΩ) resistor and two small capacitors, whose capacitance depends on the load capacitance of the crystal resonator. An external clock can be supplied from XTI; if an external clock is supplied, XTO must be left open. Because there is no clock disabling signal, using the external clock supply is not recommended. $\overline{SSPND}$ (pin 29) is unable to use clock disabling.

The PCM2912 has an internal power-on-reset circuit, which works automatically when V_{BUS} (pin 2) exceeds 2.5 V, typical (2.2 V–2.7 V), and approximately 700 μs is required until the internal reset is released.

DAC

The PCM2912 has the stereo delta-sigma DAC which uses a 64-f_S oversampling technique with 8-f_S oversampling digital filter. DAC outputs are provided through the headphone amplifier, V_{OUT}L (pin 18), and V_{OUT}R (pin 22) can provides 13 mW at 32 Ω and 0.6 V_{CCL}/V_{CCR} Vp-p at 10-kΩ load.

ADC

The PCM2912 has the mono delta-sigma ADC which uses a 64-f_S oversampling technique with 1/64-f_S decimation digital filter. Microphone input, V_{IN} (pin 16), is fed to ADC through +20-dB microphone amplifier and PGA which has +30 dB to –12 dB in 1-dB steps.

Microphone Bias

The PCM2912 has the microphone bias generator, which provides low-noise, 0.75-V_{CCA}, 2-mA source current output with appropriate output impedance for electret-microphone driving. This output, MBIAS (pin 17) should be bypassed to AGND (pin 13) through an appropriate capacitor for reducing output noise level.

Microphone Amplifier

The PCM2912 has the low-noise, single-ended mono microphone amplifier with mute function which is controlled by MUTE (pin 30). The signal gain is selectable by MAMP (pin 23). The noise level at input node is 5 μVrms, and the input impedance is 20 kΩ.

Input PGA

The PCM2912 has the low-noise input programmable gain amplifier (PGA) for the microphone amplifier output/ADC input, whose gain range is +30 dB to –12 dB in 1dB/step.

Sidetone Programmable Attenuator

The PCM2912 has the low-noise, sidetone programmable attenuator with mute function for the sidetone signal path (microphone amplifier output to output PGA input), whose gain range is 0 dB to –76 dB in 1 dB/step.

Output Programmable Attenuator

The PCM2912 has the low-noise output programmable attenuator with mute function for mixed signal, which affects DAC output signal and sidetone signal. The output PGA gain range is 0 dB to –76 dB in 1 dB/step.

V_{COM1} and V_{CCM2}

V_{COM2} (pin 12) is provided for the center voltage of a headphone amplifier. V_{COM1} (pin 11) is provided for the center voltage of all other analog circuit. Each V_{COM} pin must be decoupled with an appropriate capacitor. Because the headphone output is disconnected when entering the suspend state, determining the capacitance is important to prevent the pop-noise, especially for the V_{COM2} (pin 12). The equivalent resistance of V_{COM2} is 500 kΩ, and V_{COM1} is 15 kΩ.

Filter Pins

FL (pin 9) and FR (pin 10) are provided to make an LPF to decrease the DAC outband noise.

This is optional.

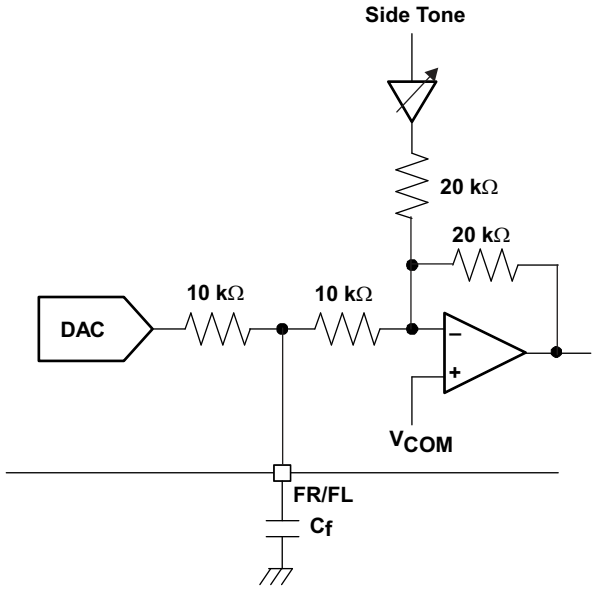


Figure 32. Filter Circuit

INTERFACE SEQUENCE

Power-On, Attach, and Play Back Sequence

The PCM2912 is ready for setup when the reset sequence has finished and the USB bus is attached. After a connection has been established by setup, the PCM2912 is ready to accept USB audio data. While awaiting the audio data (idle state), the analog output is set to bipolar zero (BPZ).

When receiving the audio data, the PCM2912 stores the first audio packet, which contained 1-ms audio data, into the internal storage buffer. The PCM2912 starts playing the audio data when detecting the following Start of Frame (SOF) packet.

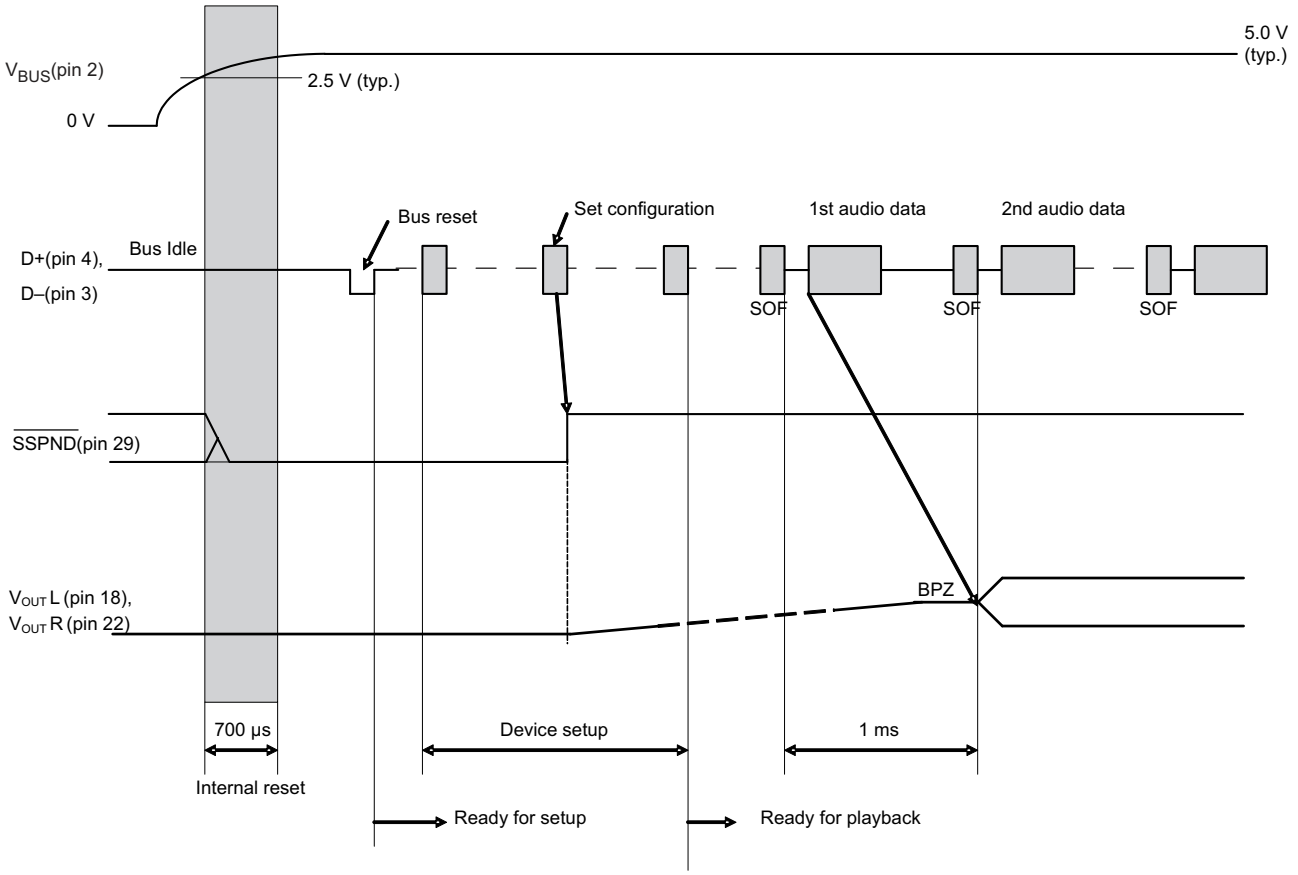


Figure 33. Initial Sequence

Play Stop and Detach Sequence

When the host finishes or aborts the playing back, the PCM2912 stops the playing after last audio data has played.

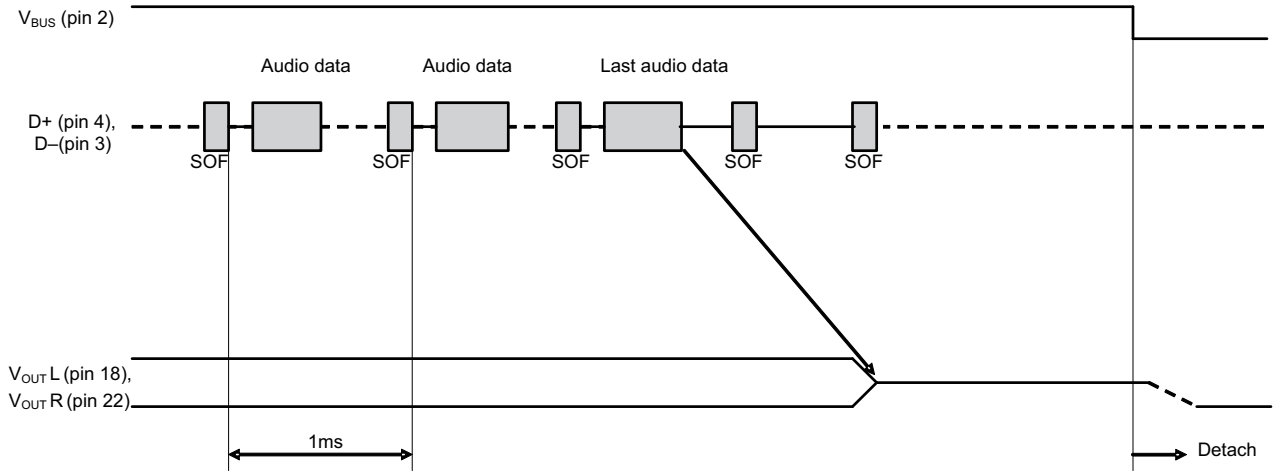


Figure 34. Play, Stop, and Detach

Record Sequence

The PCM2912 starts the audio capture into the internal memory after receiving the SET_INTERFACE command.

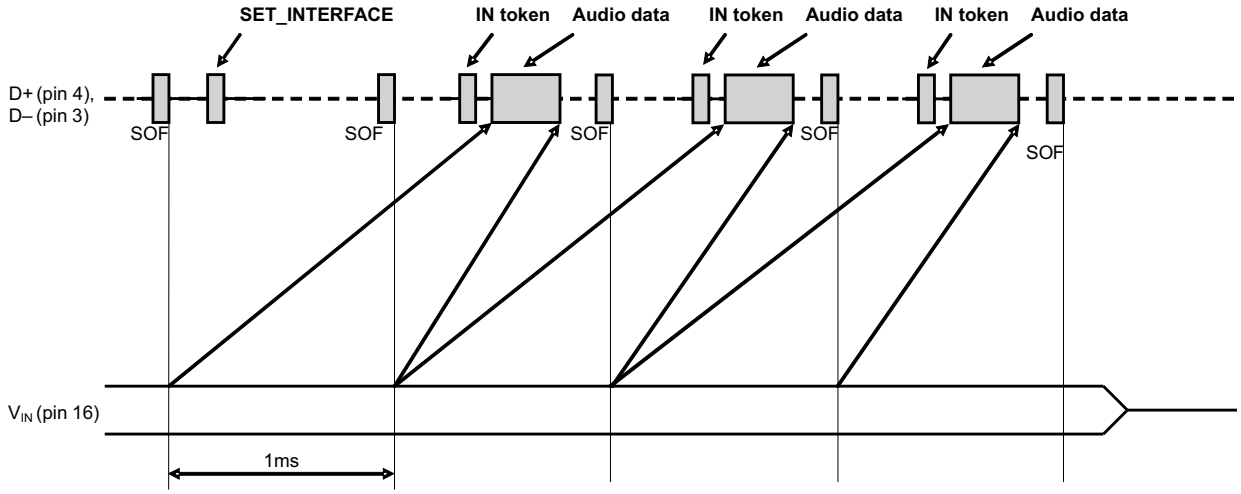


Figure 35. Record Sequence

Suspend and Resume Sequence

The PCM2912 enters the suspend state after it sees a constant Idle state on the USB bus after approximately 5 ms. When the PCM2912 enters the suspend state, $\overline{\text{SSPND}}$ flag (pin 29) is asserted. The PCM2912 wakes up immediately when detecting the non-idle state on the USB bus.

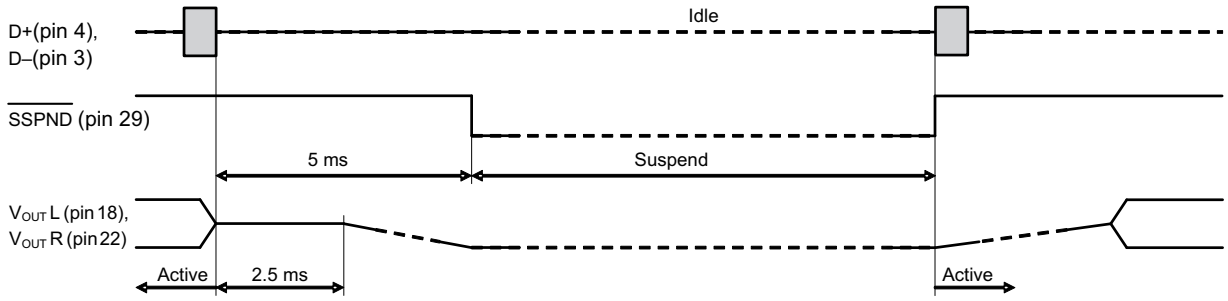
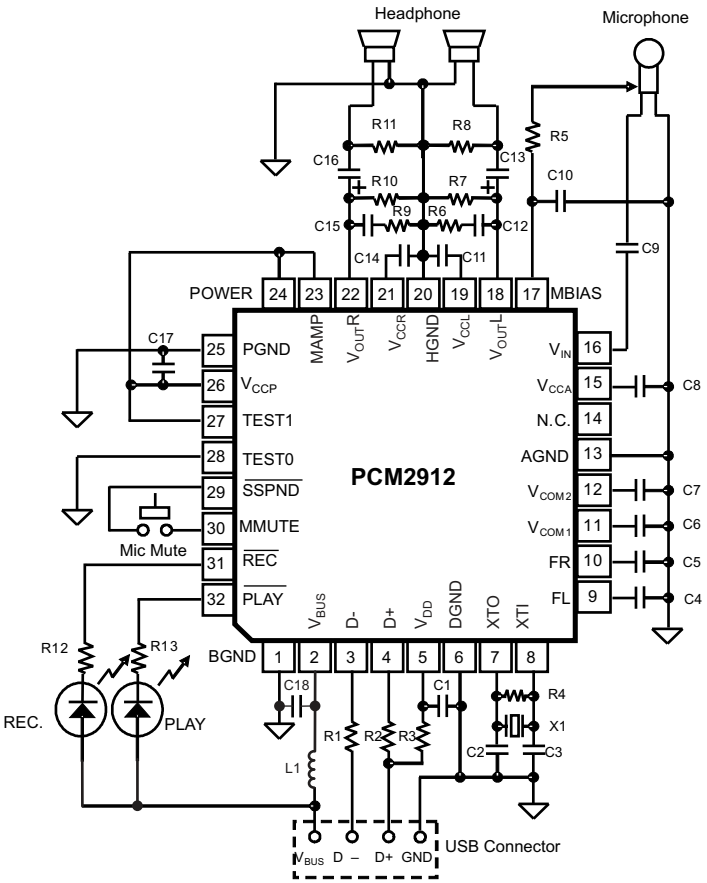


Figure 36. Suspend and Resume

TYPICAL CIRCUIT CONNECTION

A bus-powered (Hi-power), +20-dB microphone amplifier application example follows.



NOTE: X_1: 6-MHz crystal resonator
C_1, C_8, C_{11}, C_{14}, C_{17}, C_{18}: 1 µF ceramic
C_2, C_3: 10 pF to 33 pF (depending on load capacitance of crystal resonator)
C_4, C_5: 100 pF ceramic
C_6, C_{10}: 3.3 µF
C_7: 0.1 µF
C_9: 0.22 µF electrolytic (depending on required frequency response for microphone input)
C_{12}, C_{15}: 0.022 µF ceramic
C_{13}, C_{16}: 100 µF electrolytic (depending on required frequency response for headphone output)
R_1, R_2: 22 Ω to 33 Ω
R_3: 1.5 kΩ
R_4: 1 MΩ
R_5: 1 kΩ (depending on microphone characteristic)
R_6, R_9: 16 Ω
R_7, R_8, R_{10}, R_{11}: 3.3 kΩ
R_{12}, R_{13}: 820 Ω (depending on LED drive current)
L_1: 1 µH (DC resistance <0.6 Ω)
It is possible to change maximum power, if total power of actual application does not require over 100 mA (POWER = *Low* to configure as *low-power* device).

Figure 37. USB Headset Application

NOTE:

The preceding circuit is for information only. Total board design should be considered in order to meet the USB specification as a USB-compliant product.

Related Documentation from Texas Instruments

For additional information concerning the PCM2912 device, see TI application report *Operating Envronments for PCM2912 Applications* (SLAA387).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM2912PJT	NRND	TQFP	PJT	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2912	
PCM2912PJTR	NRND	TQFP	PJT	32	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2912	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

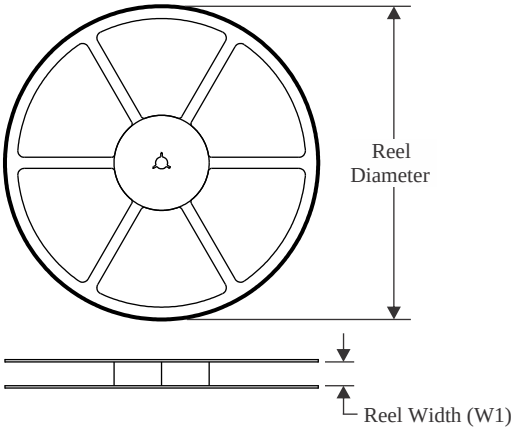
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

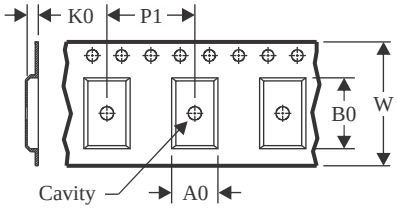
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

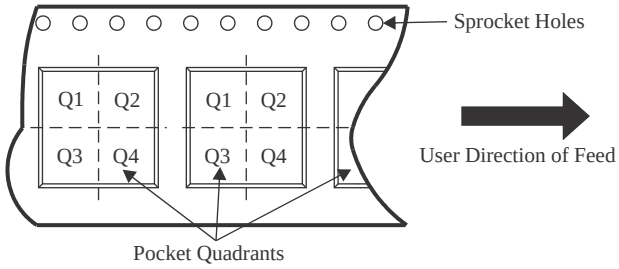


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

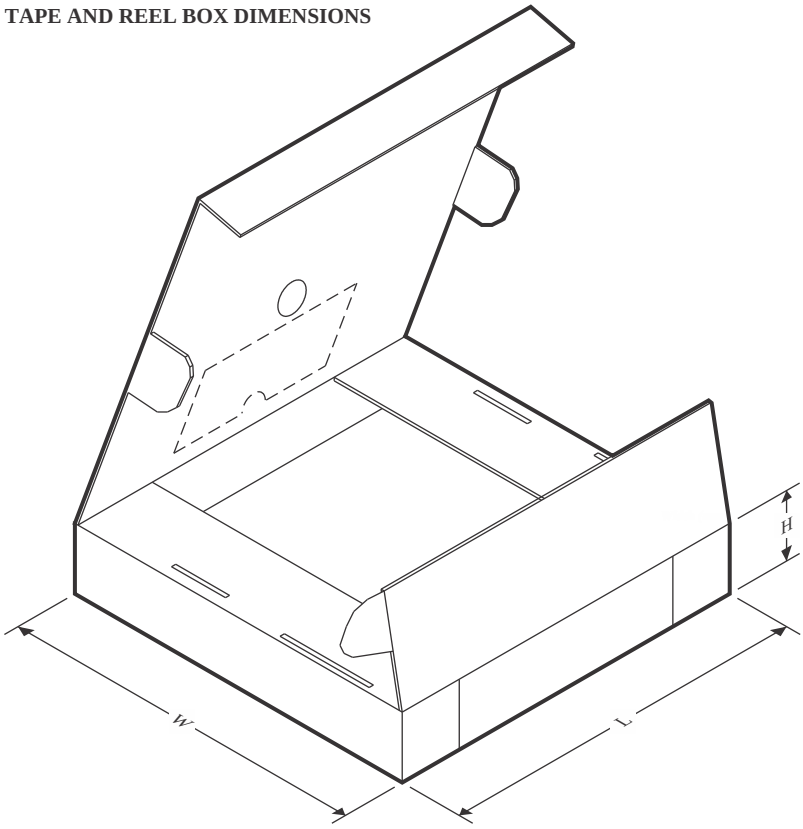
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM2912PJTR	TQFP	PJT	32	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

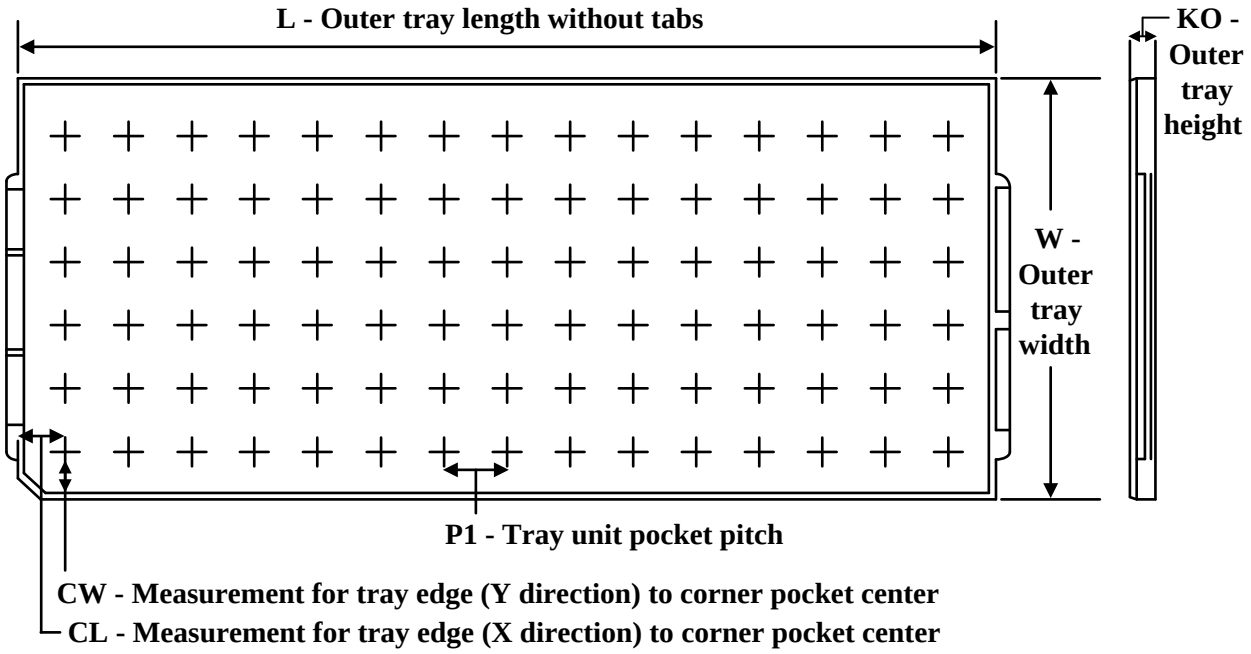
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM2912PJTR	TQFP	PJT	32	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

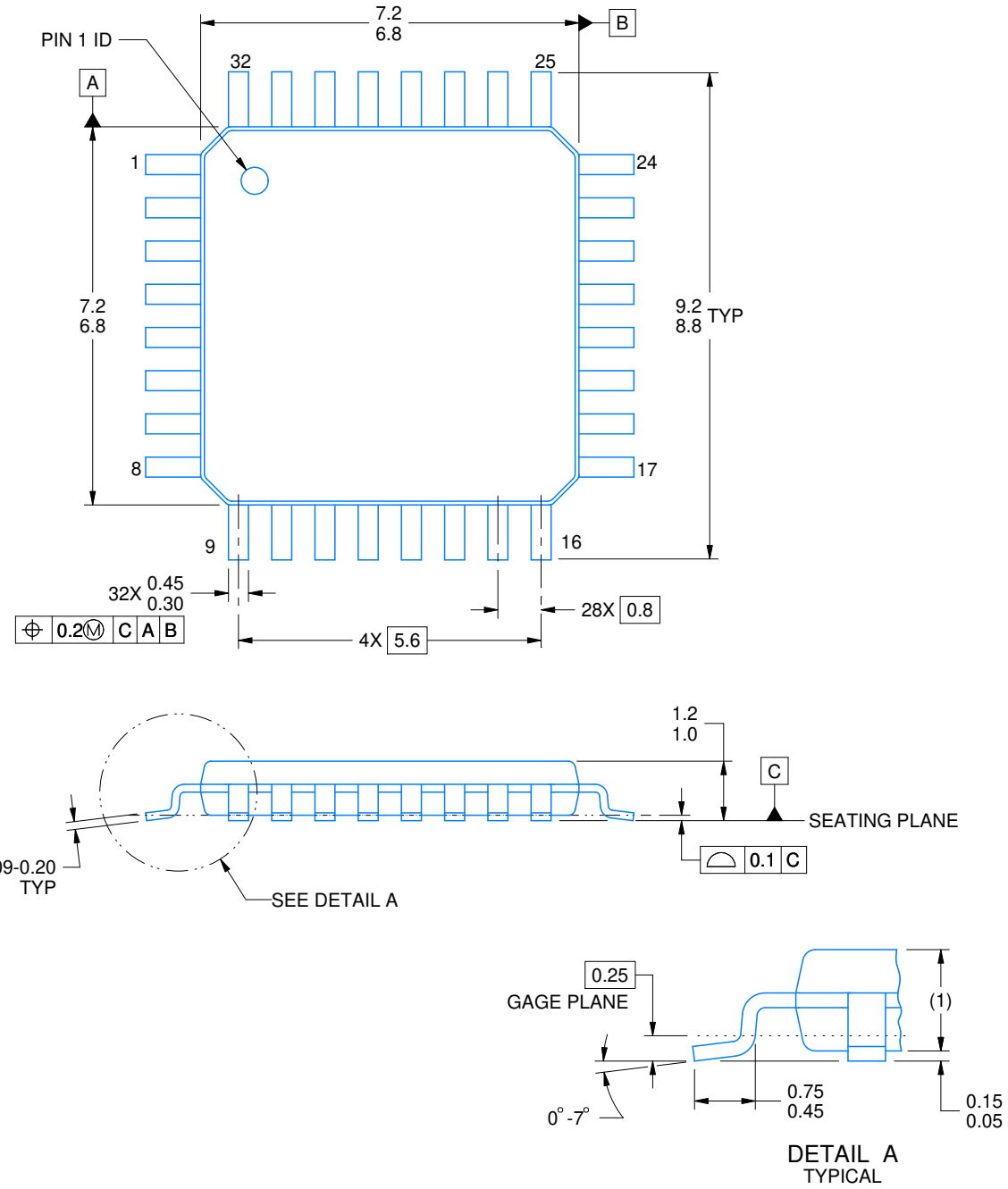
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
PCM2912PJT	PJT	TQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PACKAGE OUTLINE

PJT0032A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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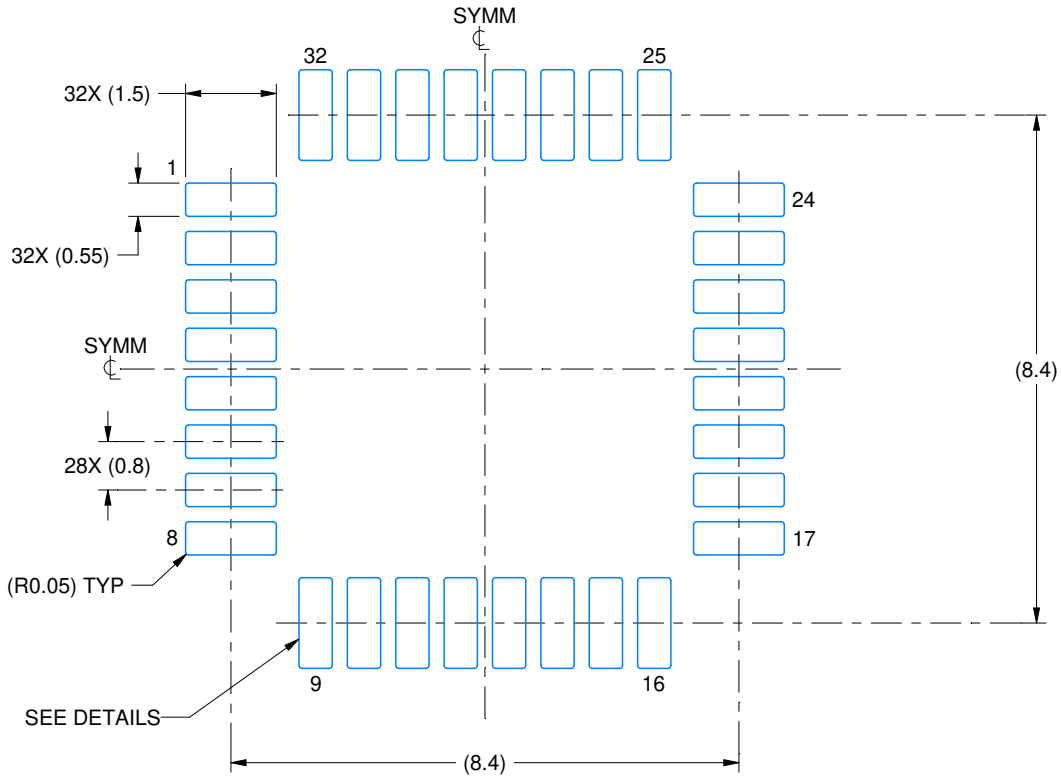
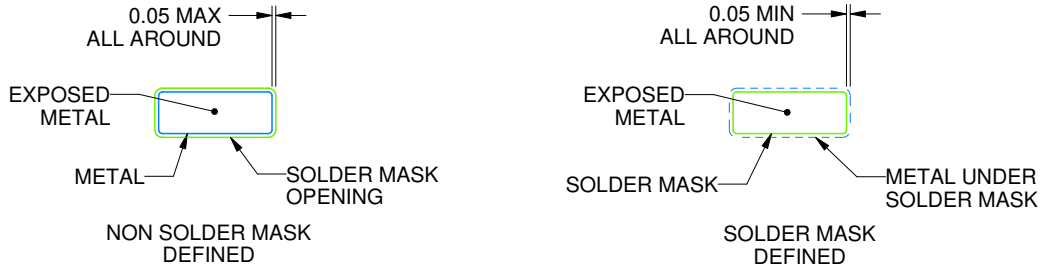
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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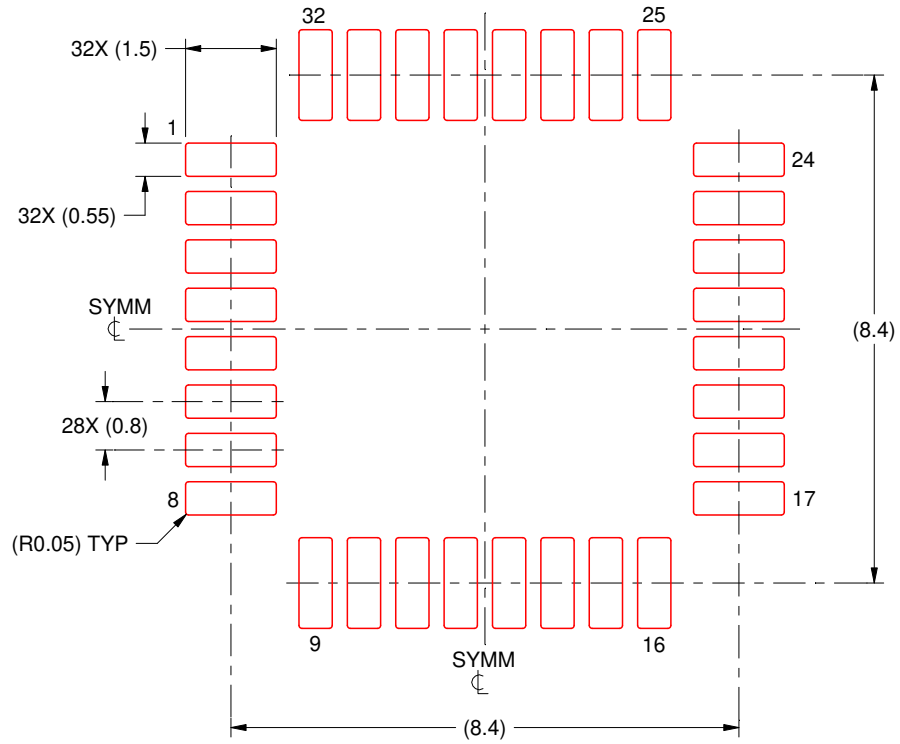
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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