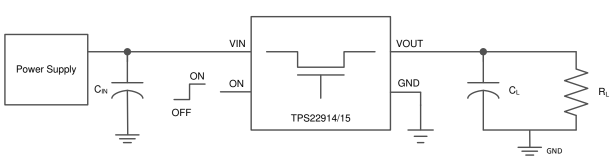
TPS2291xx, 5.5-V, 2-A, 37-mΩ On-Resistance Load Switch

1 Features

- Integrated Single Channel Load Switch
- Input Voltage Range: 1.05 V to 5.5 V
- Low On-Resistance (R_{ON})
  - R_{ON} = 37 mΩ (Typical) at V_{IN} = 5 V
  - R_{ON} = 38 mΩ (Typical) at V_{IN} = 3.3 V
  - R_{ON} = 43 mΩ (Typical) at V_{IN} = 1.8 V
- 2-A Maximum Continuous Switch Current
- Low Quiescent Current
  - 7.7 µA (Typical) at V_{IN} = 3.3 V
- Low Control Input Threshold Enables Use of 1 V or Higher GPIO
- Controlled Slew Rate
  - t_R(TPS22914B/15B) = 64 µs at V_{IN} = 3.3 V
  - t_R(TPS22914C/15C) = 913 µs at V_{IN} = 3.3 V
- Quick Output Discharge (TPS22915 only)
- Ultra-Small Wafer-Chip-Scale Package
  - 0.78 mm × 0.78 mm, 0.4-mm Pitch, 0.5-mm Height (YFP)
- ESD Performance Tested per JESD 22
  - 2-kV HBM and 1-kV CDM

2 Applications

- Smartphones, Mobile Phones
- Ultrathin, Ultrabook™ / Notebook PC
- Tablet PC, Phablet
- Wearable Technology
- Solid State Drives
- Digital Cameras



Simplified Schematic

3 Description

The TPS22914/15 is a small, low R_{ON}, single channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1.05 V to 5.5 V and can support a maximum continuous current of 2 A. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals.

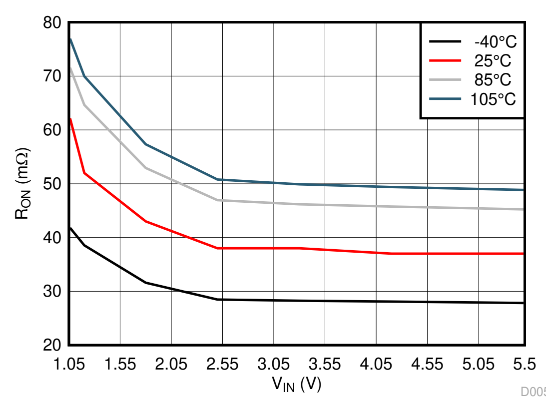
The small size and low R_{ON} makes the device ideal for being used in space constrained, battery powered applications. The wide input voltage range of the switch makes it a versatile solution for many different voltage rails. The controlled rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The TPS22915 further reduces the total solution size by integrating a 143-Ω pull-down resistor for quick output discharge (QOD) when the switch is turned off.

The TPS22914/15 is available in a small, space-saving 0.78 mm x 0.78 mm, 0.4-mm pitch, 0.5-mm height 4-pin Wafer-Chip-Scale (WCSP) package (YFP). The device is characterized for operation over the free-air temperature range of –40°C to +105°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22914B	DSBGA (4)	0.74 mm x 0.74 mm
TPS22914C		
TPS22915B		
TPS22915C		

(1) For all available packages, see the orderable addendum at the end of the datasheet.



R_{ON} vs V_{IN} (I_{OUT} = –200 mA)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2016) to Revision E (October 2020) — **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document ... 1
- Updated the body size in the *Device Information* table ... 1

Changes from Revision C (July 2015) to Revision D (September 2016) — **Page**

- Changed "TPS22915B" only, to "TPS22915B/C only" in the *Electrical Characteristics* table ... 5

Changes from Revision B (September 2014) to Revision C (July 2015) — **Page**

- Updated T_A ratings in datasheet from 85°C to 105°C ... 1

Changes from Revision A (June 2014) to Revision B (September 2014) — **Page**

- Updated X-axis scales in th Typical Characteristics section. ... 9

Changes from Revision * (June 2014) to Revision A (June 2014) — **Page**

- Initial release of full version. ... 1

5 Device Comparison Table

DEVICE	R_{ON} at 3.3V (TYPICAL)	t_R at 3.3V (TYPICAL)	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22914B	38 mΩ	64 µs	No	2 A	Active High
TPS22914C	38 mΩ	913 µs	No	2 A	Active High
TPS22915B	38 mΩ	64 µs	Yes	2 A	Active High
TPS22915C	38 mΩ	913 µs	Yes	2 A	Active High

6 Pin Configuration and Functions

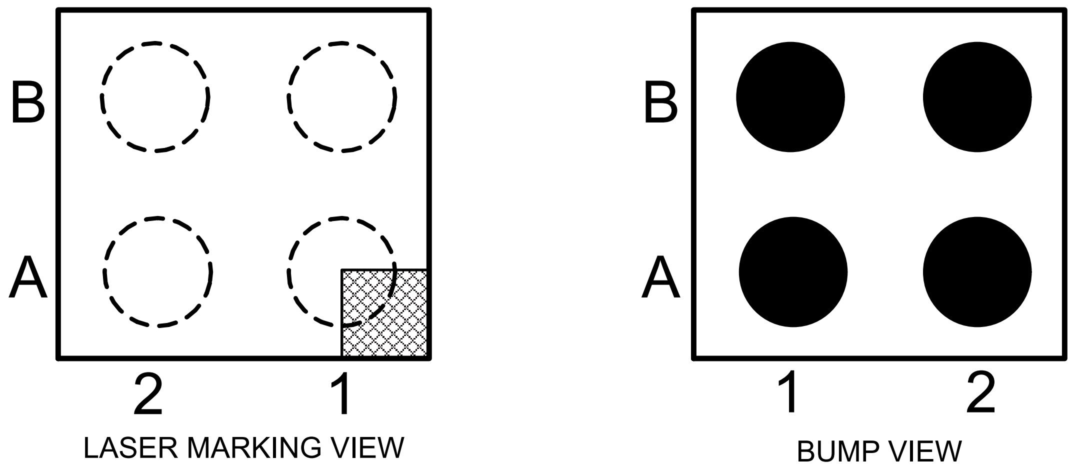


Figure 6-1. YFP PACKAGE 4 PIN DSBGA TOP VIEW

Table 6-1. Pin Description

B	ON	GND
A	VIN	VOUT
	2	**1**

Table 6-2. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	VOUT	O	Switch output. Place ceramic bypass capacitor(s) between this pin and GND. See the *Detailed Description* section for more information
A2	VIN	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the *Detailed Description* section for more information
B1	GND	—	Device ground
B2	ON	I	Active high switch control input. Do not leave floating

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ON}	ON voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		2.5	A
T_J	Maximum junction temperature		125	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage		1.05	5.5	V
V_{ON}	ON voltage		0	5.5	V
V_{OUT}	Output voltage			V_{IN}	V
$V_{IH, ON}$	High-level input voltage, ON	V_{IN} = 1.05 V to 5.5 V	1	5.5	V
$V_{IL, ON}$	Low-level input voltage, ON	V_{IN} = 1.05 V to 5.5 V	0	0.5	V
T_A	Operating free-air temperature range[1]		–40	105	°C
C_{IN}	Input Capacitor		1[2]		µF

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(MAX)}$], the maximum power dissipation of the device in the application [$P_{D(MAX)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(MAX)} = T_{J(MAX)} – (\theta_{JA} \times P_{D(MAX)})$.
(2) Refer to the *Detailed Description* section.

7.4 Thermal Information

THERMAL METRIC[1]		TPS2291x YFP (DSBGA) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	2.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12	°C/W

7.4 Thermal Information (continued)

THERMAL METRIC[1]		TPS2291x YFP (DSBGA) 4 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	36	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ +105°C. **Typical values are for T_A = 25°C.**

PARAMETER		TEST CONDITION		T_A	MIN	TYP	MAX	UNIT
$I_{Q, VIN}$	Quiescent current (TPS22914B/15B)	V_{ON} = 5 V, I_{OUT} = 0 A	V_{IN} = 5.5 V	–40°C to +85°C		7.7	10.8	µA
				–40°C to +105°C			12.1	
			V_{IN} = 5 V	–40°C to +85°C		7.6	9.6	
				–40°C to +105°C			11.9	
			V_{IN} = 3.3 V	–40°C to +85°C		7.7	9.6	
				–40°C to +105°C			12	
			V_{IN} = 1.8 V	–40°C to +85°C		8.4	11	
				–40°C to +105°C			13.5	
			V_{IN} = 1.2 V	–40°C to +85°C		7.4	10.4	
				–40°C to +105°C			13.9	
			V_{IN} = 1.05 V	–40°C to +85°C		6.7	10.9	
				–40°C to +105°C			11.7	
	Quiescent current (TPS22914C/15C)	V_{ON} = 5 V, I_{OUT} = 0 A	V_{IN} = 5.5 V	–40°C to +85°C		7.7	11.5	µA
				–40°C to +105°C			14.1	
			V_{IN} = 5 V	–40°C to +85°C		7.6	11.1	
				–40°C to +105°C			13.7	
			V_{IN} = 3.3 V	–40°C to +85°C		7.7	10.7	
				–40°C to +105°C			13.3	
			V_{IN} = 1.8 V	–40°C to +85°C		8.4	11.7	
				–40°C to +105°C			13.4	
			V_{IN} = 1.2 V	–40°C to +85°C		7.4	11	
				–40°C to +105°C			12.8	
			V_{IN} = 1.05 V	–40°C to +85°C		6.7	10.9	
				–40°C to +105°C			10.9	

7.5 Electrical Characteristics (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ +105°C. **Typical values are for T_A = 25°C.**

PARAMETER		TEST CONDITION		T_A	MIN	TYP	MAX	UNIT
$I_{SD, VIN}$	Shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 5.5 V	–40°C to +85°C		0.5	2	µA
				–40°C to +105°C			3	
			V_{IN} = 5.0 V	–40°C to +85°C		0.5	2	
				–40°C to +105°C			3	
			V_{IN} = 3.3 V	–40°C to +85°C		0.5	2	
				–40°C to +105°C			3	
			V_{IN} = 1.8 V	–40°C to +85°C		0.5	2	
				–40°C to +105°C			3	
			V_{IN} = 1.2 V	–40°C to +85°C		0.4	2	
				–40°C to +105°C			3	
			V_{IN} = 1.05 V	–40°C to +85°C		0.4	2	
				–40°C to +105°C			3	
I_{ON}	ON pin input leakage current	V_{IN} = 5.5 V, I_{OUT} = 0 A		–40°C to +105°C			0.1	µA
R_{ON}	On-resistance	V_{IN} = 5.5 V, I_{OUT} = –200 mA		25°C		37	40	mΩ
				–40°C to +85°C			51	
				–40°C to +105°C			57	
		V_{IN} = 5 V, I_{OUT} = –200 mA		25°C		37	41	mΩ
				–40°C to +85°C			51	
				–40°C to +105°C			57	
		V_{IN} = 4.2 V, I_{OUT} = –200 mA		25°C		37	41	mΩ
				–40°C to +85°C			52	
				–40°C to +105°C			58	
		V_{IN} = 3.3 V, I_{OUT} = –200 mA		25°C		38	41	mΩ
				–40°C to +85°C			52	
				–40°C to +105°C			59	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA		25°C		38	42	mΩ
				–40°C to +85°C			53	
				–40°C to +105°C			58	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA		25°C		43	48	mΩ
				–40°C to +85°C			59	
				–40°C to +105°C			66	
		V_{IN} = 1.2 V, I_{OUT} = –200 mA		25°C		52	61	mΩ
				–40°C to +85°C			73	
				–40°C to +105°C			85	
		V_{IN} = 1.05 V, I_{OUT} = –200 mA		25°C		63	96	mΩ
				–40°C to +85°C			102	
				–40°C to +105°C			107	

7.5 Electrical Characteristics (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ +105°C. **Typical values are for T_A = 25°C.**

PARAMETER		TEST CONDITION	T_A	MIN	TYP	MAX	UNIT
V_{HYS}	ON pin hysteresis	V_{IN} = 5.5 V	25°C		102		mV
		V_{IN} = 5 V			100		
		V_{IN} = 3.3 V			98		
		V_{IN} = 2.5 V			96		
		V_{IN} = 1.8 V			96		
		V_{IN} = 1.2 V			94		
		V_{IN} = 1.05 V			92		
R_{PD} (1)	Output pull down resistor	V_{IN} = V_{OUT} = 3.3 V, V_{ON} = 0 V	–40°C to +105°C		143	200	Ω

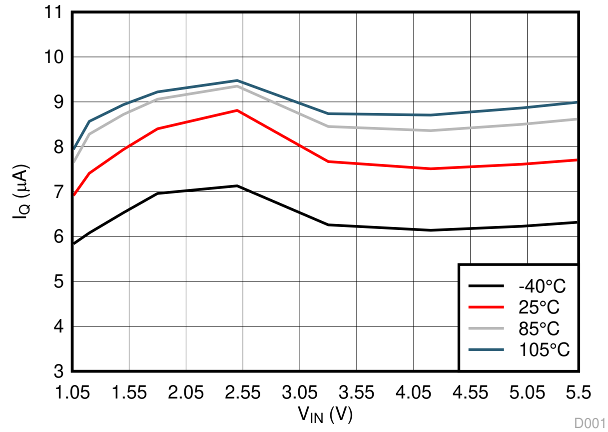
(1) TPS22915B/C only.

7.6 Switching Characteristics

Refer to the timing test circuit in Figure 8-1 (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN is already in steady state condition before the ON pin is asserted high.

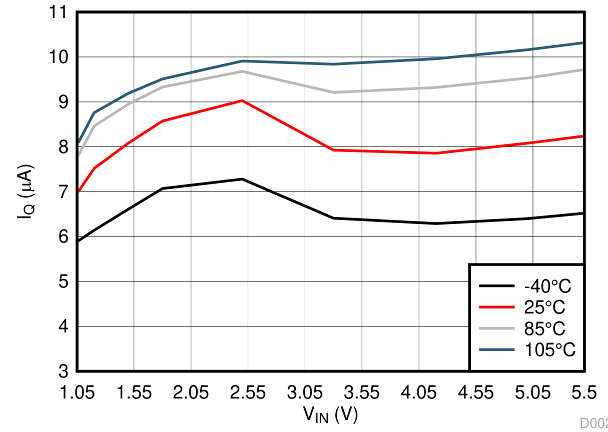
PARAMETER		TEST CONDITION	TYP (TPS22914B/15B)	TYP (TPS22914C/15C)	UNIT
V_{IN} = 5 V, V_{ON} = 5 V, T_A = 25°C (unless otherwise noted)					
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	104	1300	µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	2	2	µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	89	1277	µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	2	2	µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	59	663	µs
V_{IN} = 3.3 V, V_{ON} = 5 V, T_A = 25°C (unless otherwise noted)					
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	83	1077	µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	2	2	µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	64	913	µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	2	2	µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	52	622	µs
V_{IN} = 1.05 V, V_{ON} = 5 V, T_A = 25°C (unless otherwise noted)					
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	61	752	µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	3	3	µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	28	409	µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	2	2	µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF	47	547	µs

7.7 Typical DC Characteristics



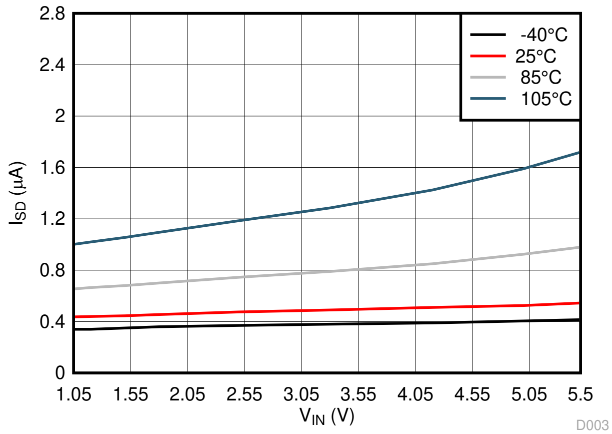
V_{ON} = 5 V I_{OUT} = 0 A

Figure 7-1. I_Q vs V_{IN} (TPS22914B/15B)



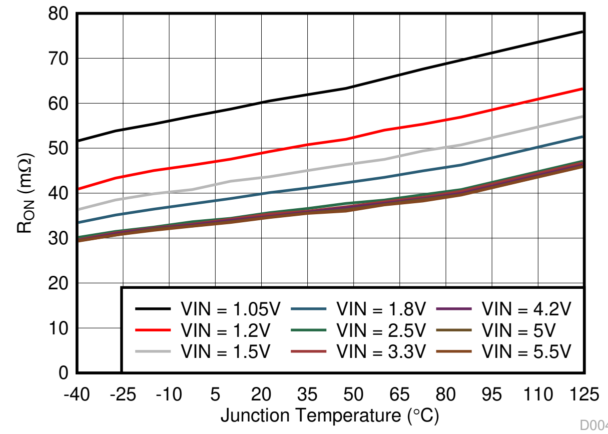
V_{ON} = 5 V I_{OUT} = 0 A

Figure 7-2. I_Q vs V_{IN} (TPS22914C/15C)



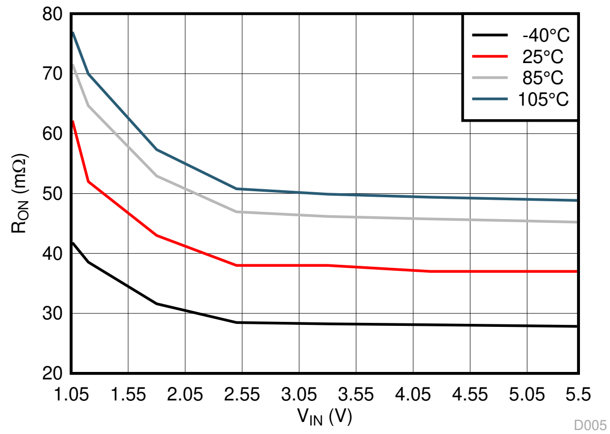
V_{ON} = 0 V I_{OUT} = 0 A

Figure 7-3. I_{SD} vs V_{IN}



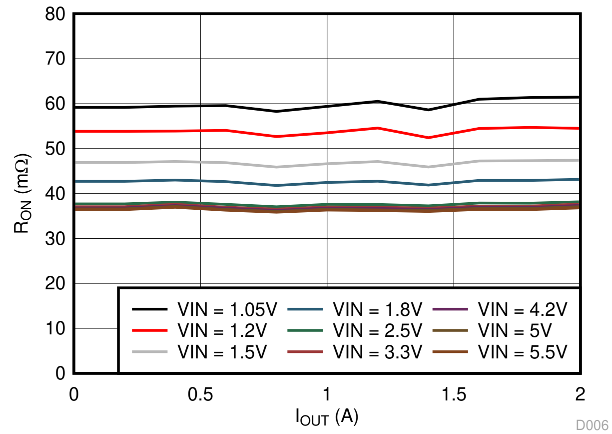
V_{ON} = 5 V I_{OUT} = –200 mA

Figure 7-4. R_{ON} vs T_J



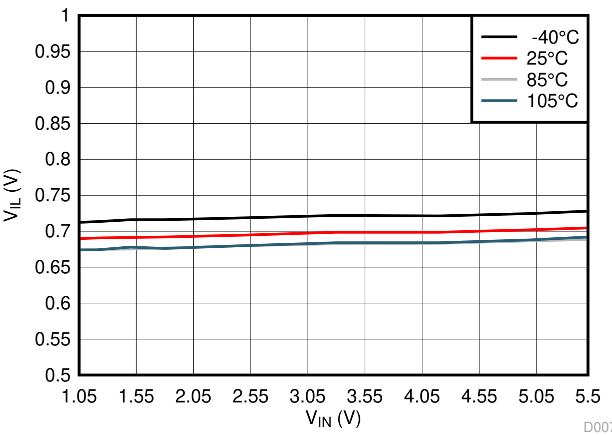
V_{ON} = 5 V I_{OUT} = –200 mA

Figure 7-5. R_{ON} vs V_{IN}



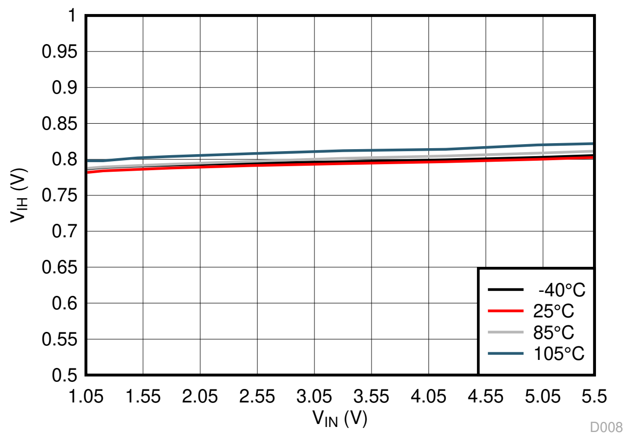
V_{ON} = 5 V T_A = 25°C

Figure 7-6. R_{ON} vs I_{OUT}



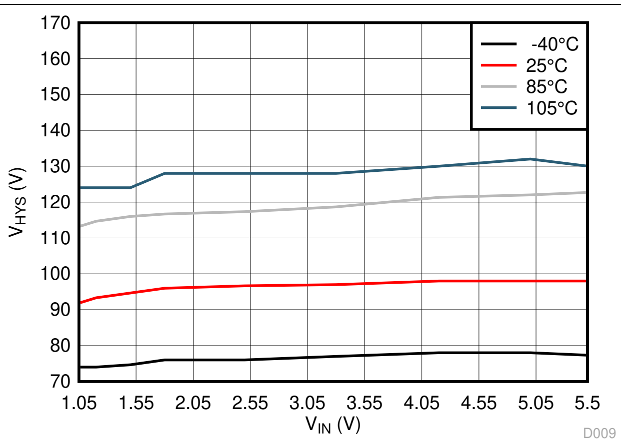
I_{OUT} = 0 A

Figure 7-7. V_{IL} vs V_{IN}



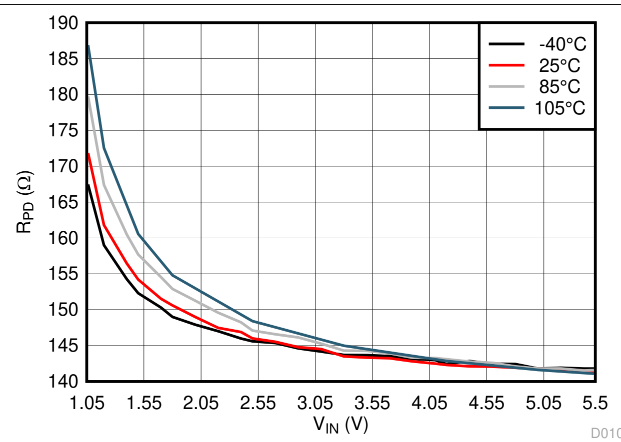
I_{OUT} = 0 A

Figure 7-8. V_{IH} vs V_{IN}



I_{OUT} = 0 A

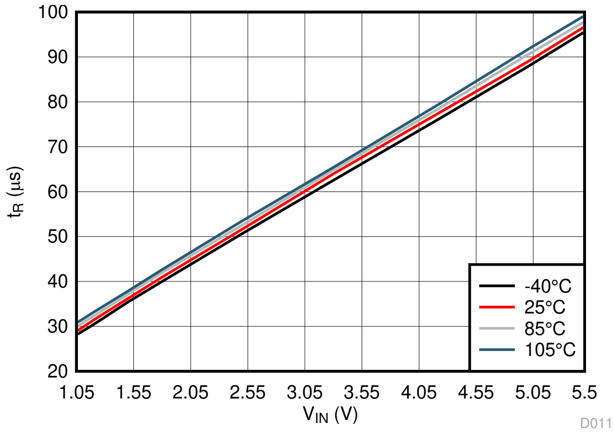
Figure 7-9. V_{HYS} vs V_{IN}



V_{IN} = V_{OUT} V_{ON} = 0 V

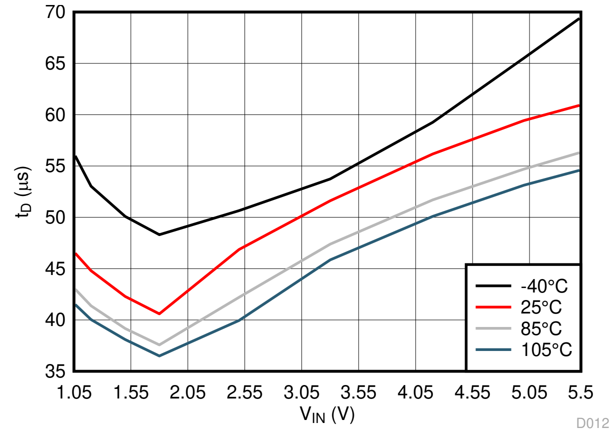
Figure 7-10. R_{PD} vs V_{IN}

7.8 Typical AC Characteristics (TPS22914B/15B)



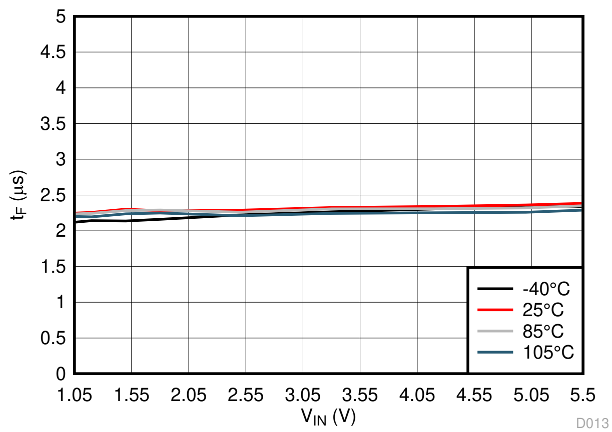
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 7-11. t_R vs V_{IN}



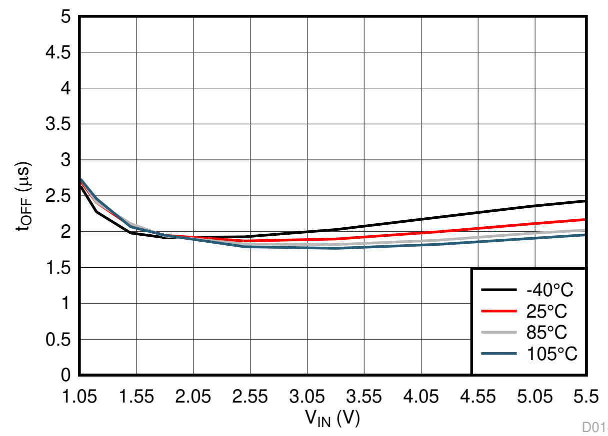
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 7-12. t_D vs V_{IN}



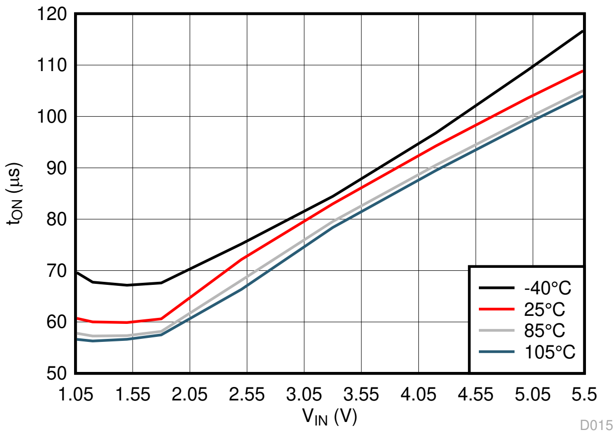
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 7-13. t_F vs V_{IN}



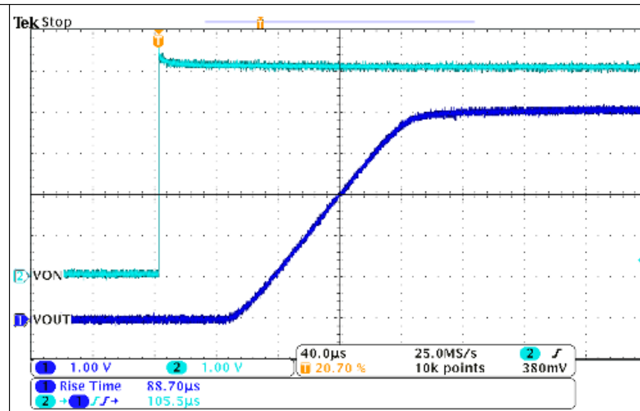
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 7-14. t_{OFF} vs V_{IN}



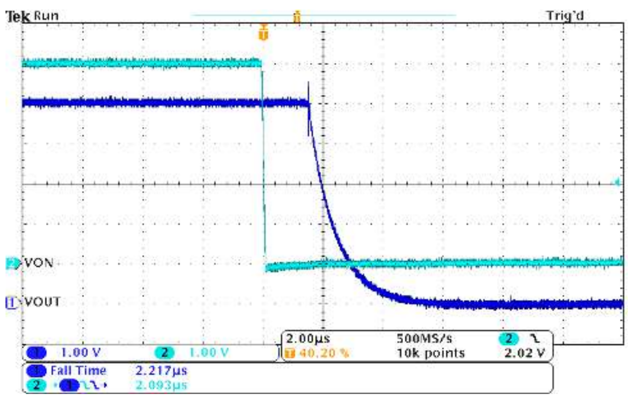
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 7-15. t_{ON} vs V_{IN}



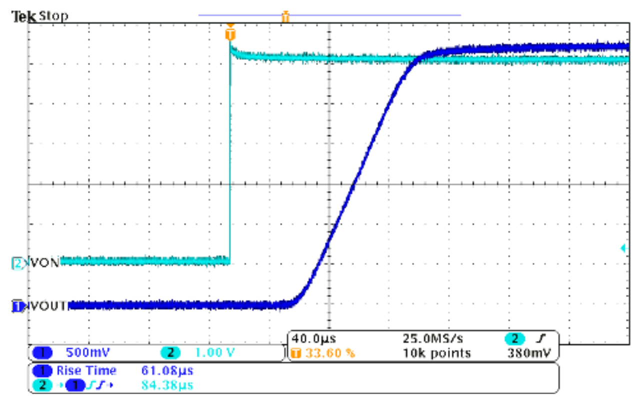
V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 7-16. t_R at V_{IN} = 5 V



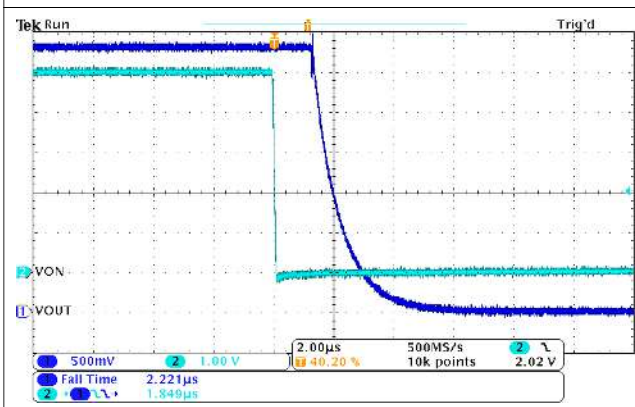
V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 7-17. t_F at V_{IN} = 5 V



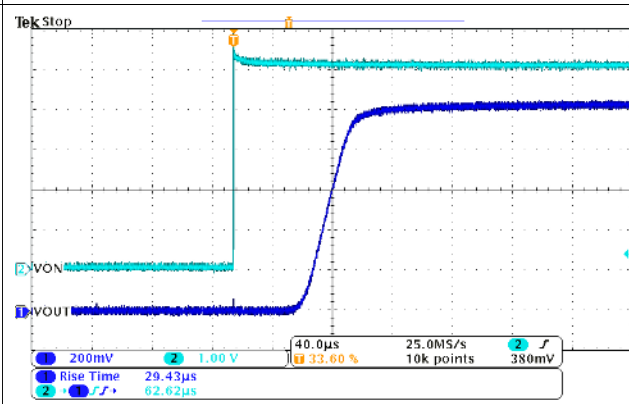
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 7-18. t_R at V_{IN} = 3.3 V



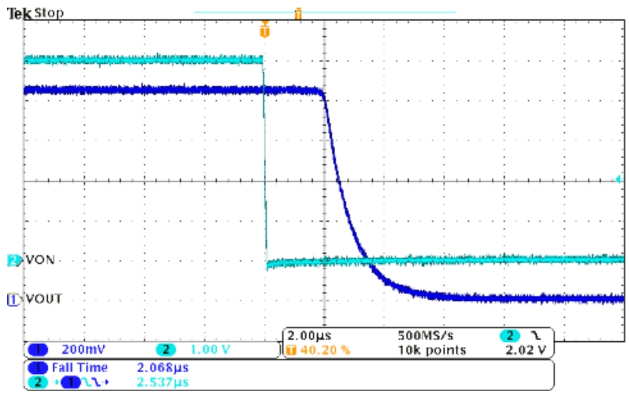
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 7-19. t_F at V_{IN} = 3.3V



V_{IN} = 1.05 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

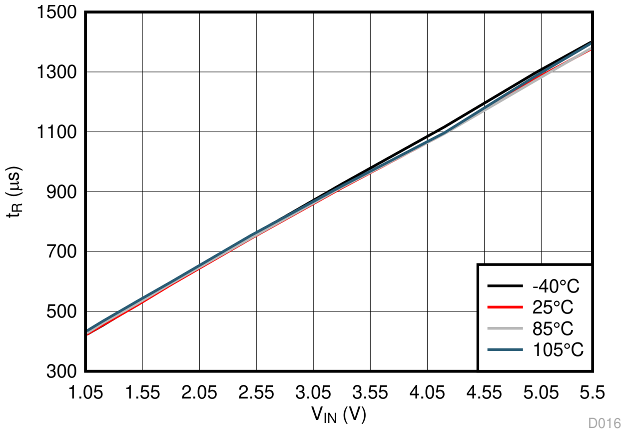
Figure 7-20. t_R at V_{IN} = 1.05V



V_{IN} = 1.05 V C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

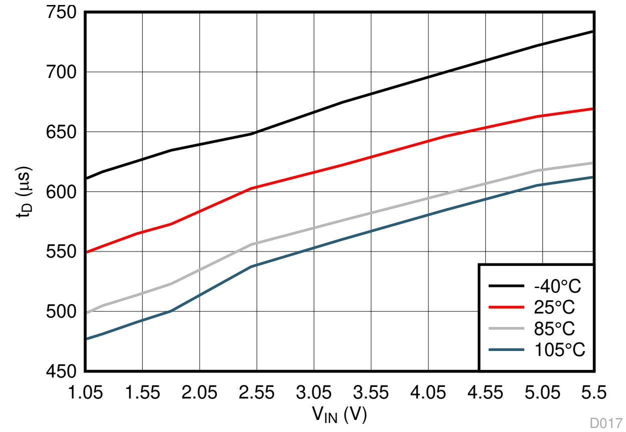
Figure 7-21. t_F at V_{IN} = 1.05 V

7.9 Typical AC Characteristics (TPS22914C/15C)



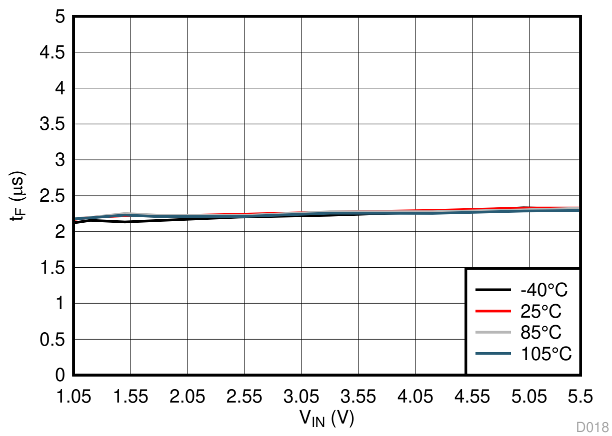
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 7-22. t_R vs V_{IN}



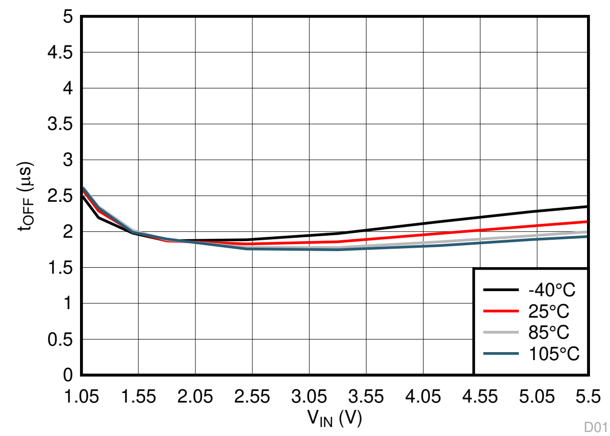
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 7-23. t_D vs V_{IN}



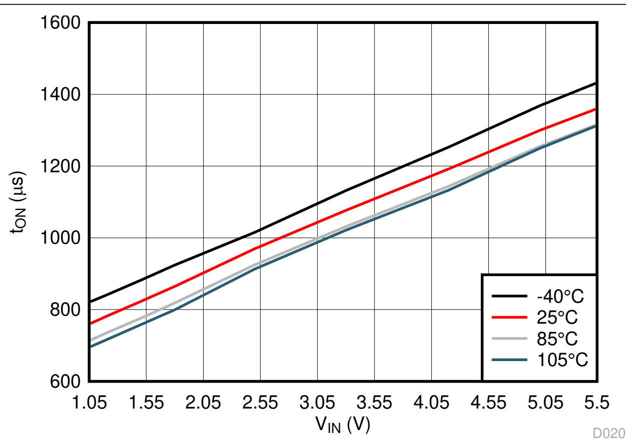
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 7-24. t_F vs V_{IN}



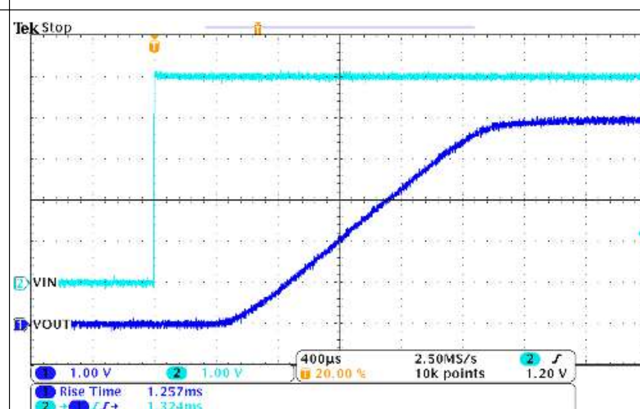
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 7-25. t_{OFF} vs V_{IN}



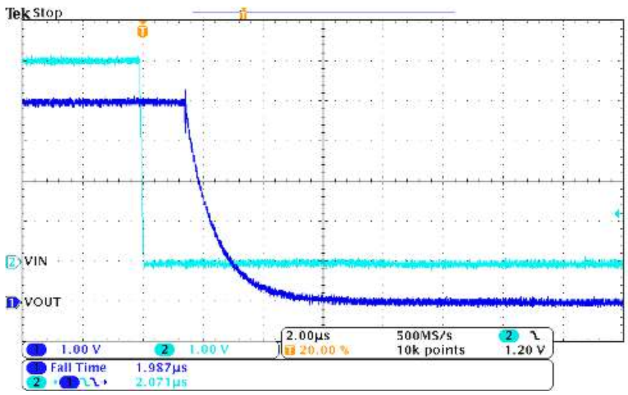
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 7-26. t_{ON} vs V_{IN}



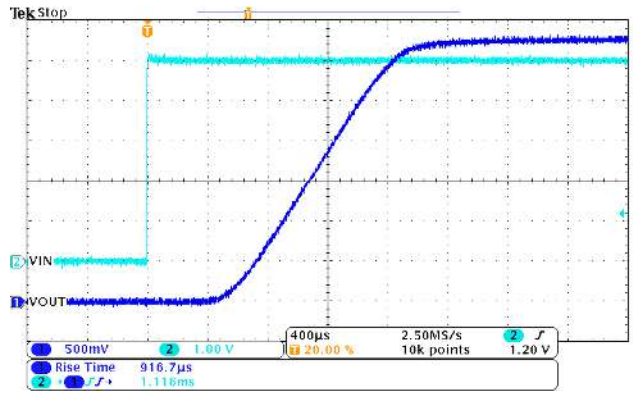
V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 7-27. t_R at V_{IN} = 5 V



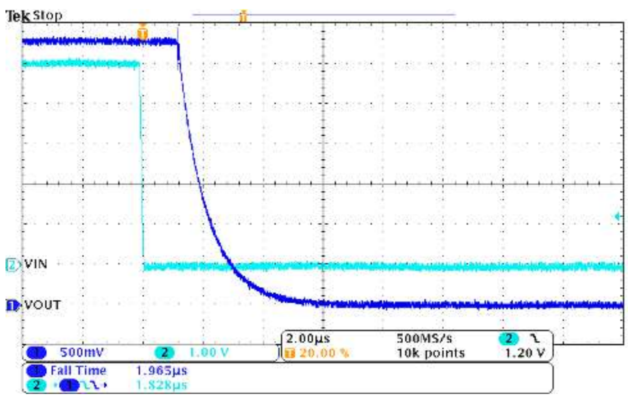
V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 7-28. t_F at V_{IN} = 5 V



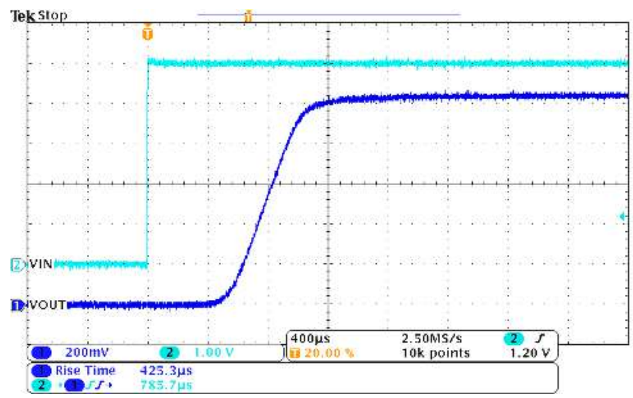
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 7-29. t_R at V_{IN} = 3.3 V



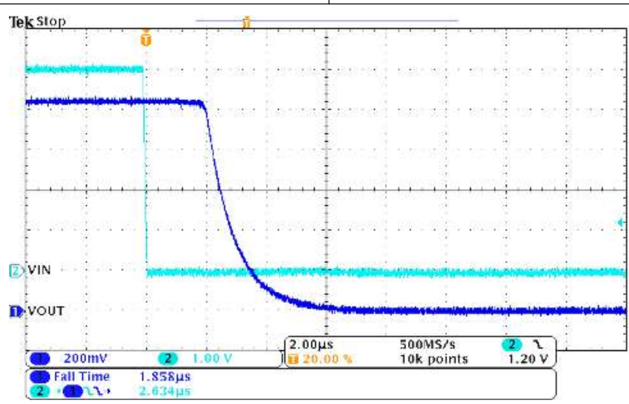
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 7-30. t_F at V_{IN} = 3.3 V



V_{IN} = 1.05 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

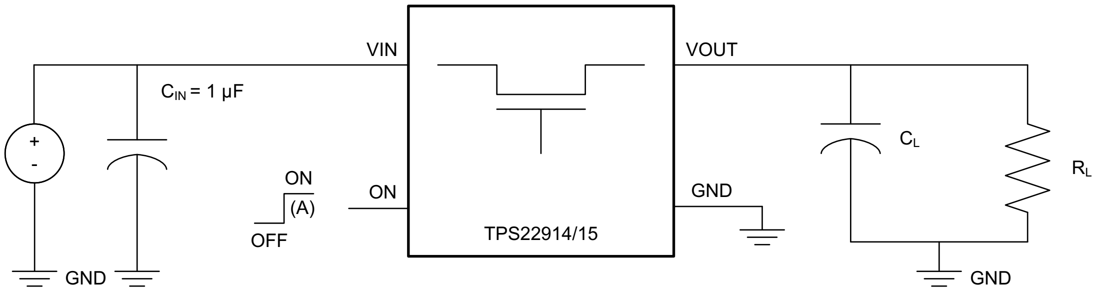
Figure 7-31. t_R at V_{IN} = 1.05 V



V_{IN} = 1.05 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 7-32. t_F at V_{IN} = 1.05 V

8 Parameter Measurement Information



A. Rise and fall times of the control signal is 100ns

Figure 8-1. Test Circuit

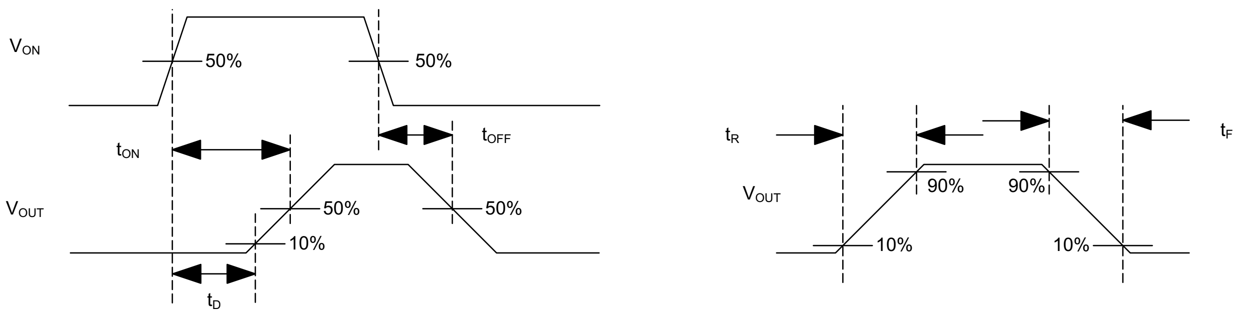


Figure 8-2. Timing Waveforms

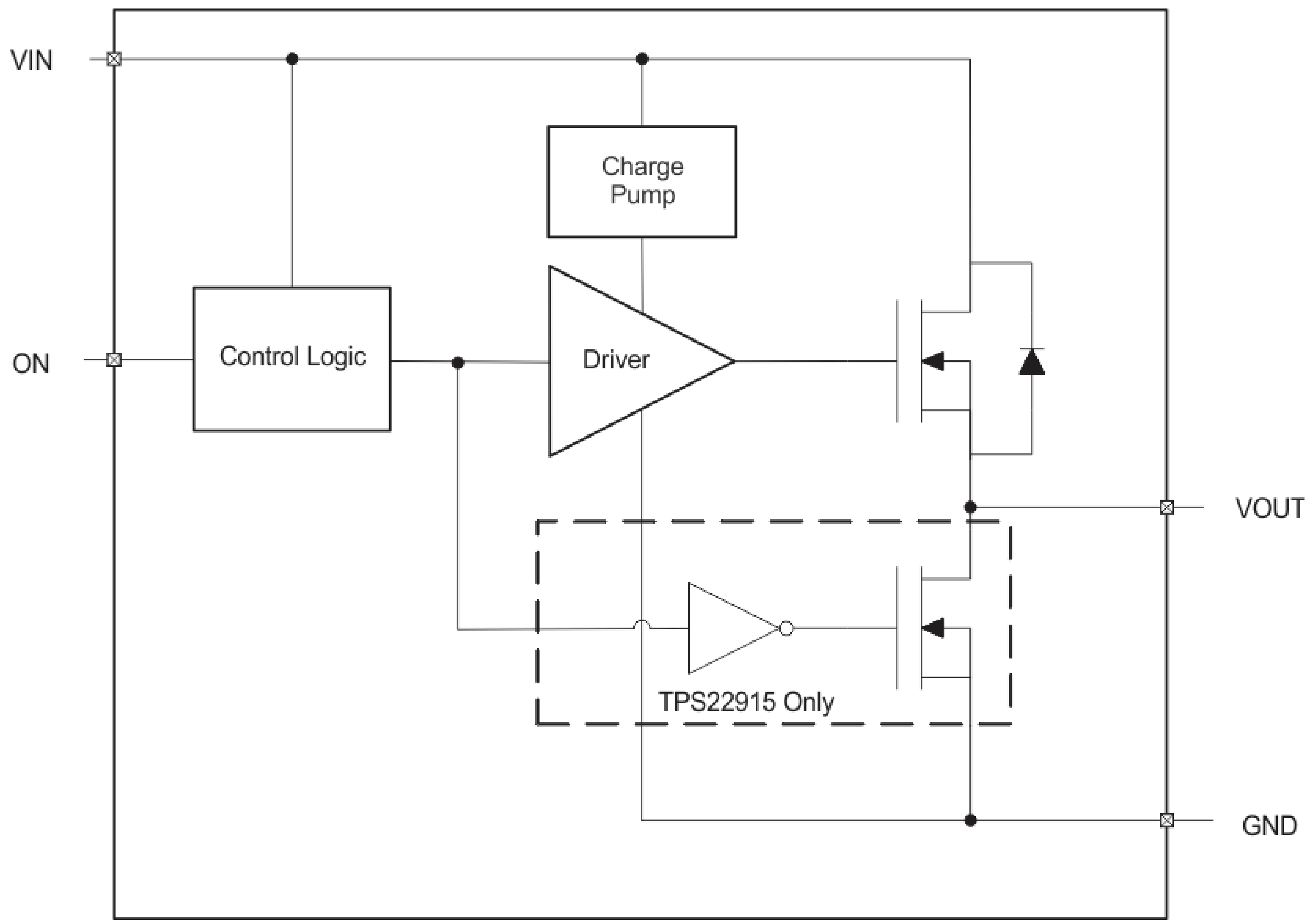
9 Detailed Description

9.1 Overview

The device is a 5.5-V, 2-A load switch in a 4-pin YFP package. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance N-channel MOSFET which reduces the drop out voltage through the device.

The device has a controlled and fixed slew rate which helps reduce or eliminate power supply droop due to large inrush currents. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 On and Off Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

9.3.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.3.3 Output Capacitor (C_L)

Due to the integrated body diode in the MOSFET, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

9.4 Device Functional Modes

Table 9-1 describes the connection of the VOUT pin depending on the state of the ON pin.

Table 9-1. VOUT Connection

ON	TPS22914	TPS22915
L	Open	GND
H	VIN	VIN

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device.

10.2 Typical Application

This typical application demonstrates how the TPS22914 and TPS22915 can be used to power downstream modules.

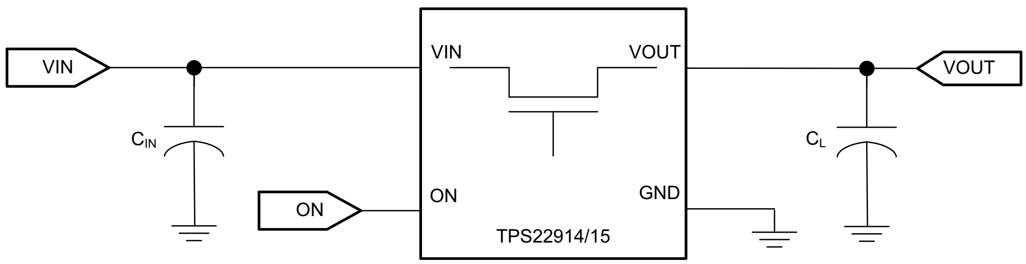


Figure 10-1. Typical Application Schematic

10.2.1 Design Requirements

For this design example, use the input parameters shown in Table 10-1.

Table 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	5 V
Load current	2 A

10.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- Load Current

10.2.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics* table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use Equation 1 to calculate the VIN to VOUT voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \tag{1}$$

where

- ΔV = voltage drop from VIN to VOUT
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.2.2.2 Inrush Current

To determine how much inrush current is caused by the C_L capacitor, use Equation 2.

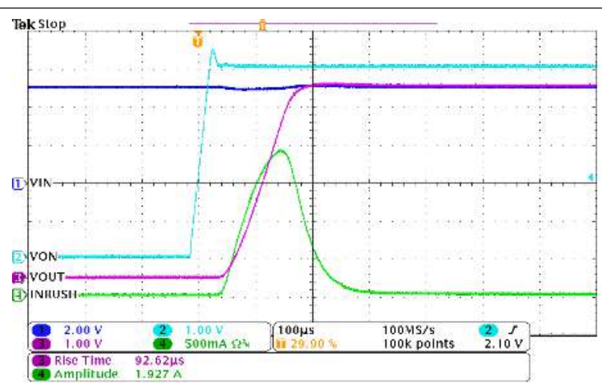
$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \tag{2}$$

where

- I_{INRUSH} = amount of inrush caused by C_L
- C_L = capacitance on VOUT
- dt = rise time in VOUT during the ramp up of VOUT when the device is enabled
- dV_{OUT} = change in VOUT during the ramp up of VOUT when the device is enabled

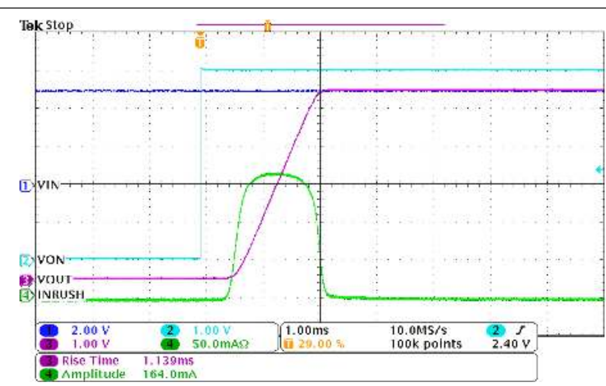
An appropriate C_L value must be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

10.2.3 Application Curves



V_{IN} = 5 V C_L = 47 µF

Figure 10-2. TPS22914B/15B Inrush Current



V_{IN} = 5 V C_L = 47 µF

Figure 10-3. TPS22914C/15C Inrush Current

11 Power Supply Recommendations

The device is designed to operate from a VIN range of 1.05 V to 5.5 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 µF may be sufficient.

12 Layout

12.1 Layout Guidelines

1. VIN and VOUT traces must be as short and wide as possible to accommodate for high current.
2. The VIN pin must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
3. The VOUT pin must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor must be placed as close to the device pins as possible.

12.1.1 Thermal Considerations

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 3.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (3)$$

where

- $P_{D(MAX)}$ = maximum allowable power dissipation
- $T_{J(MAX)}$ = maximum allowable junction temperature (125°C for the TPS22914/15)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. Refer to the *Thermal Information* table. This parameter is highly dependent upon board layout.

12.2 Layout Example

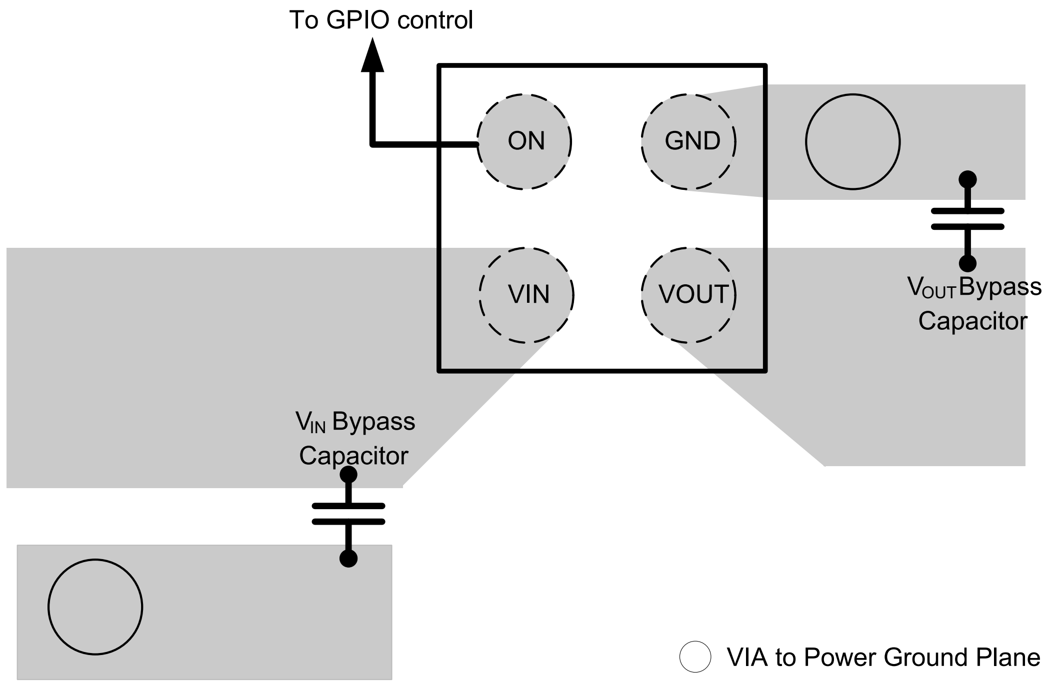


Figure 12-1. Recommended Board Layout

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *Basics of Load Switches*
- *Managing Inrush Current*
- *Load Switch Thermal Considerations*
- *Using the TPS22915BEVM-078 Single Channel Load Switch IC*
- *Implementing Ship Mode Using the TPS22915B Load Switches*

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 13-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS22914B	Click here	Click here	Click here	Click here	Click here
TPS22914C	Click here	Click here	Click here	Click here	Click here
TPS22915B	Click here	Click here	Click here	Click here	Click here
TPS22915C	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

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13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22914BYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S3	Samples
TPS22914BYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S3	Samples
TPS22914CYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S6	Samples
TPS22914CYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S6	Samples
TPS22915BYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	S4	Samples
TPS22915BYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	S4	Samples
TPS22915CYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S7	Samples
TPS22915CYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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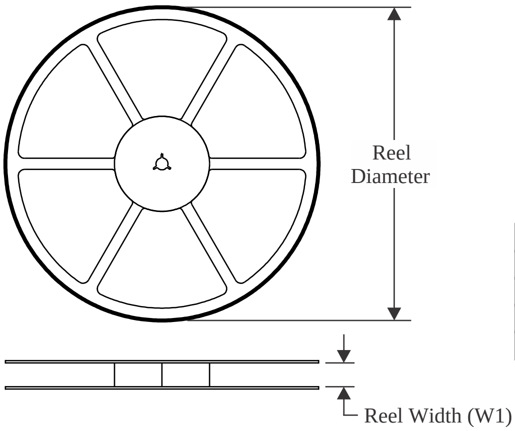
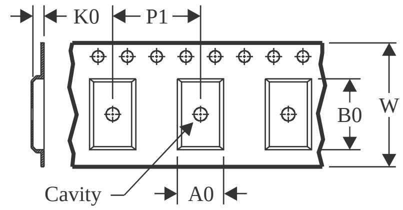
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

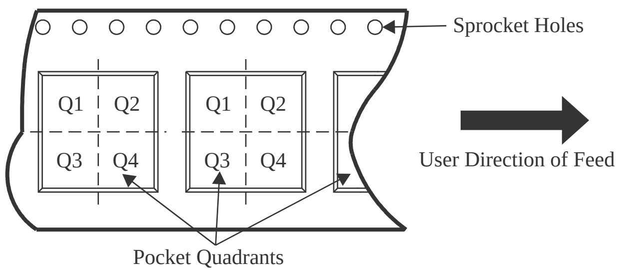


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

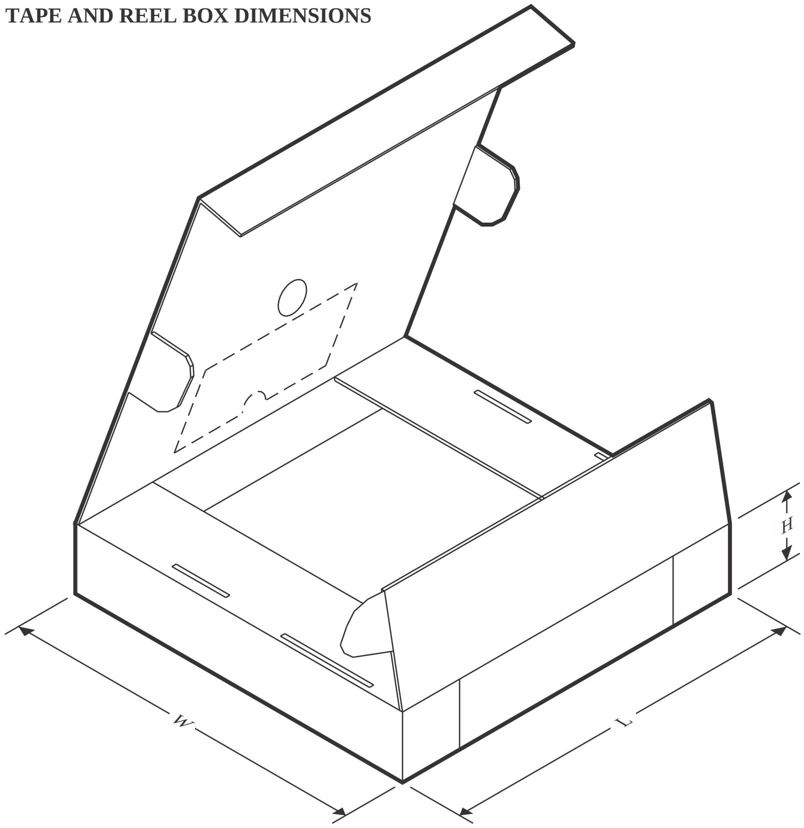
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

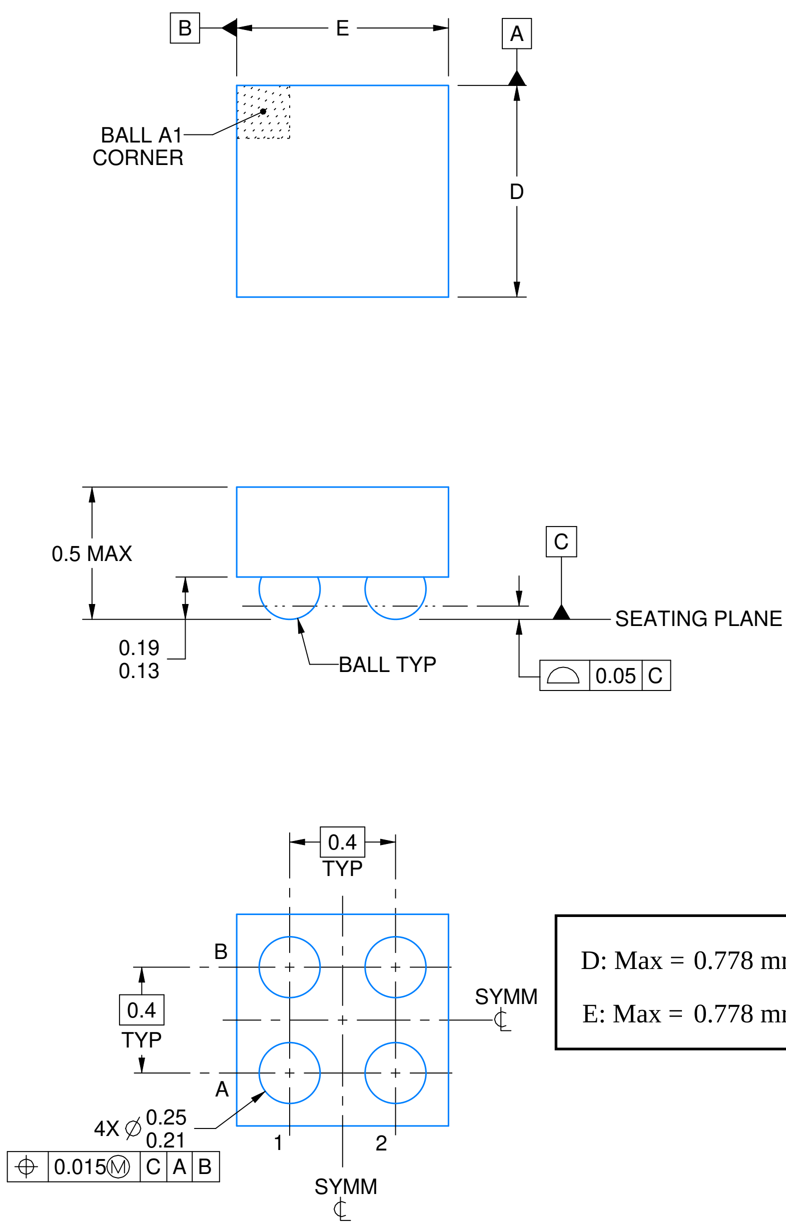
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22914BYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22914BYFPT	DSBGA	YFP	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22914BYFPT	DSBGA	YFP	4	250	178.0	9.2	0.85	0.85	0.59	4.0	8.0	Q1
TPS22914CYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22914CYFPT	DSBGA	YFP	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22915BYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22915BYFPR	DSBGA	YFP	4	3000	178.0	9.2	0.85	0.85	0.59	4.0	8.0	Q1
TPS22915BYFPT	DSBGA	YFP	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22915BYFPT	DSBGA	YFP	4	250	178.0	9.2	0.85	0.85	0.59	4.0	8.0	Q1
TPS22915CYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22915CYFPT	DSBGA	YFP	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22914BYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22914BYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22914BYFPT	DSBGA	YFP	4	250	220.0	220.0	35.0
TPS22914CYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22914CYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22915BYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22915BYFPR	DSBGA	YFP	4	3000	220.0	220.0	35.0
TPS22915BYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22915BYFPT	DSBGA	YFP	4	250	220.0	220.0	35.0
TPS22915CYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22915CYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0



D: Max = 0.778 mm, Min =0.718 mm

E: Max = 0.778 mm, Min =0.718 mm

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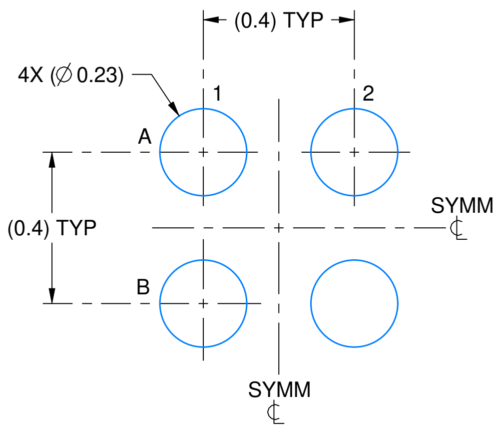
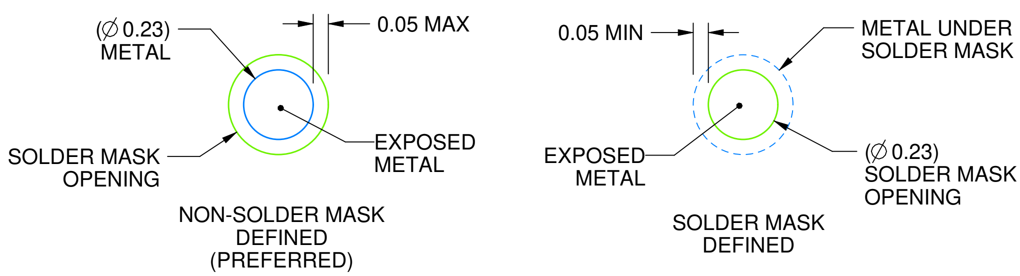
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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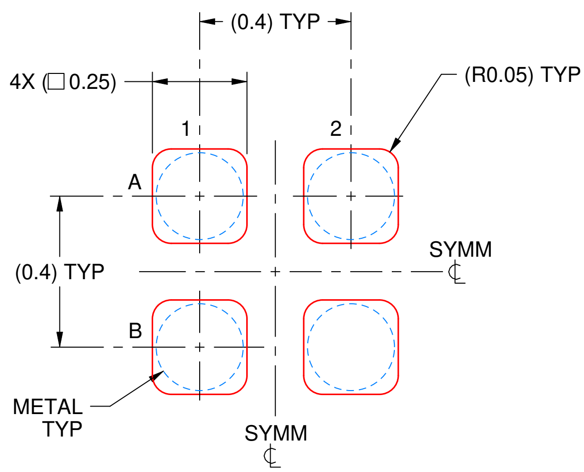
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.