μPA2825T1S

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Rev.1.00
May 25, 2012

MOS FIELD EFFECT TRANSISTOR

Description

The μPA2825T1S is N-channel MOS Field Effect Transistor designed for power management applications of a notebook computer and Lithium-Ion battery protection circuit.

Features

- V_{DSS} = 30 V (T_A = 25°C)
- Low on-state resistance
  — $R_{DS(on)}$ = 4.6 mΩ MAX. (V_{GS} = 10 V, I_D = 24 A)
- 4.5 V Gate-drive available
- Small & thin type surface mount package with heat spreader (HWSON-8)
- Pb-free, Halogen Free

Ordering Information

Part No.	Lead Plating	Packing	Package
μPA2825T1S-E2-AT *1	Pure Sn (Tin)	Tape 5000 p/reel	HWSON-8 typ. 0.022 g

Note: *1. Pb-free (This product does not contain Pb in external electrode and other parts.)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±24	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±96	A
Total Power Dissipation *2	P_{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) *2	P_{T2}	3.8	W
Total Power Dissipation (T_C = 25°C)	P_{T3}	16.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Current *3	I_{AS}	18	A
Single Avalanche Energy *3	E_{AS}	32.4	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	7.6	°C/W

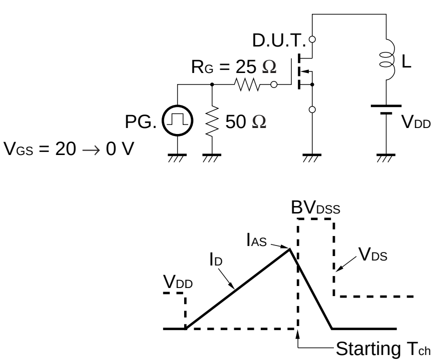
Notes: *1. PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt
*3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

Electrical Characteristics (T_A = 25°C)

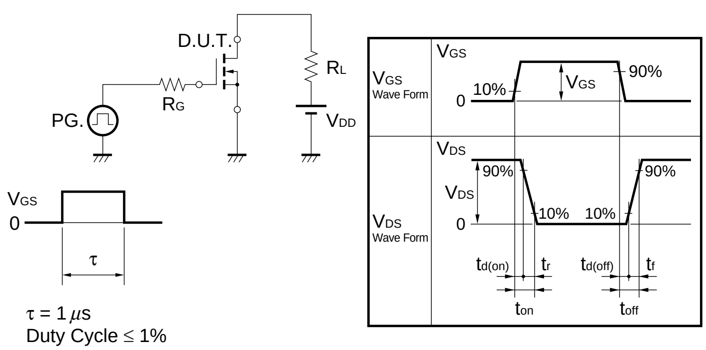
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS} = 30 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±16 V, V_{DS} = 0 V
Gate Cut-off Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance *1	| y_{fs} |	16			S	V_{DS} = 10 V, I_D = 6 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		3.7	4.6	mΩ	V_{GS} = 10 V, I_D =24 A
	$R_{DS(on)2}$		7.0	12	mΩ	V_{GS} = 4.5 V, I_D = 6 A
Input Capacitance	C_{iss}		2600		pF	V_{DS} = 10 V,
Output Capacitance	C_{oss}		850		pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		800		pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		17		ns	V_{DD} = 15 V, I_D =12 A,
Rise Time	t_r		86		ns	V_{GS} = 10 V,
Turn-off Delay Time	$t_{d(off)}$		100		ns	R_G = 10 Ω
Fall Time	t_f		58		ns	
Total Gate Charge	Q_G		57		nC	V_{GS} = 10 V,
			35		nC	V_{GS} = 5 V
Gate to Source Charge	Q_{GS}		7.5		nC	V_{DD} = 15 V,
Gate to Drain Charge	Q_{GD}		22		nC	I_D =24 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9		V	I_F = 24 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		42		ns	I_F = 24 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		37		nC	di/dt = 100 A/μs

Note: *1. Pulsed

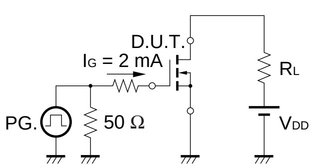
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

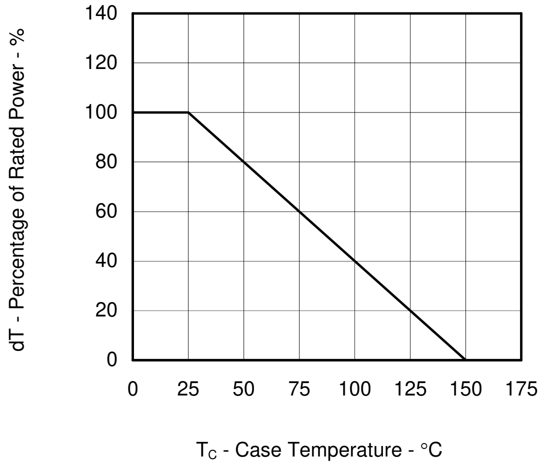


TEST CIRCUIT 3 GATE CHARGE

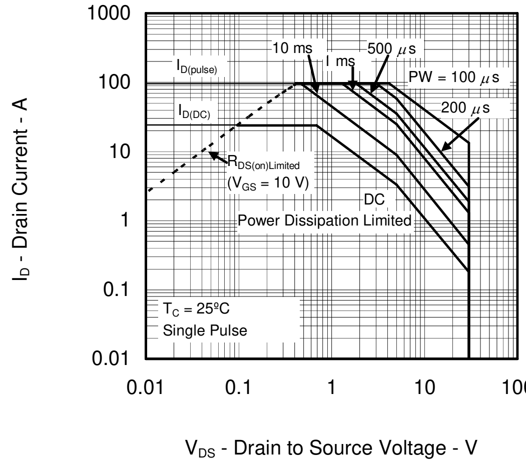


Typical Characteristics (T_A = 25°C)

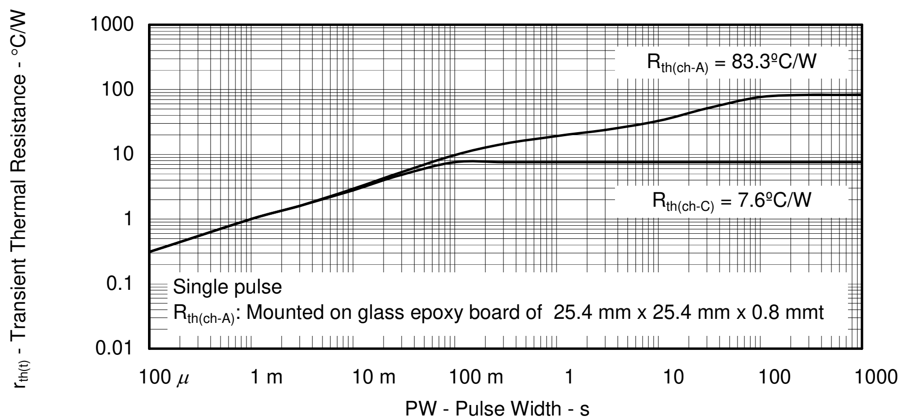
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



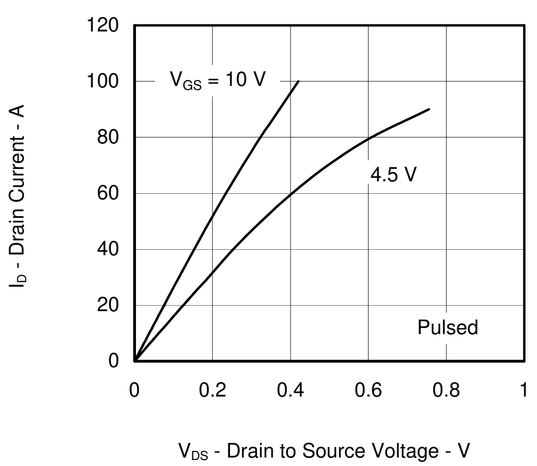
FORWARD BIAS SAFE OPERATING AREA



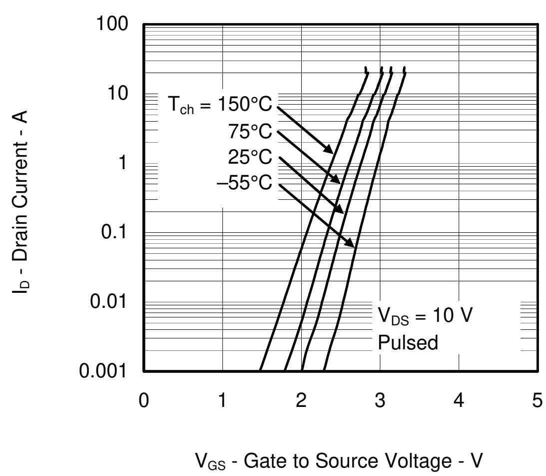
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



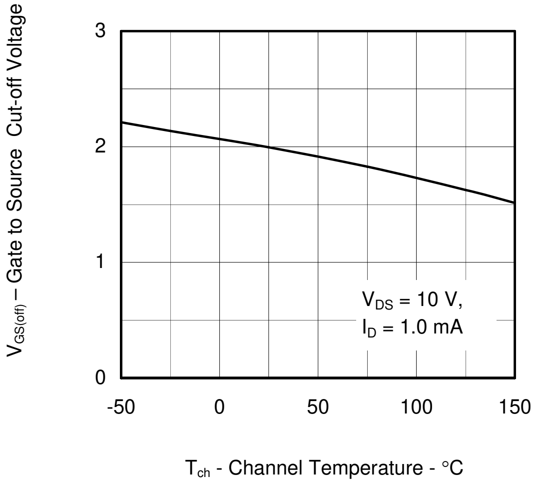
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



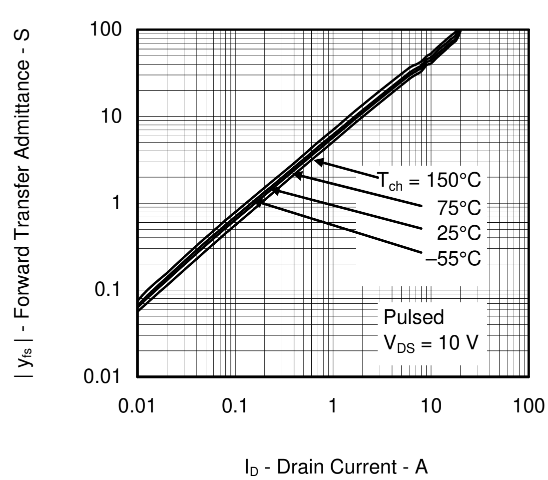
FORWARD TRANSFER CHARACTERISTICS



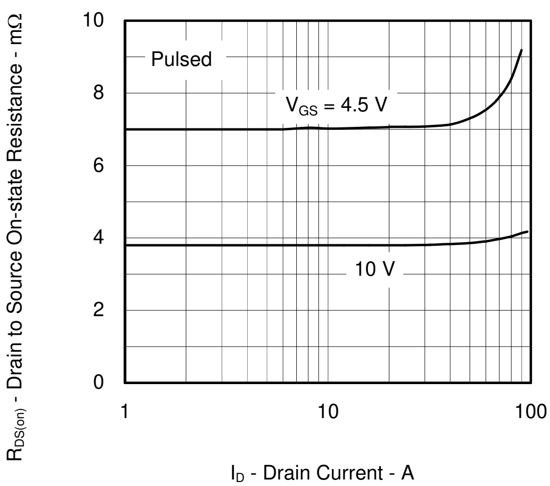
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



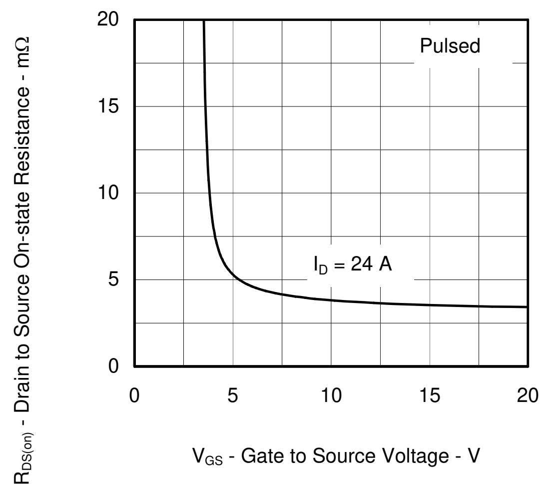
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



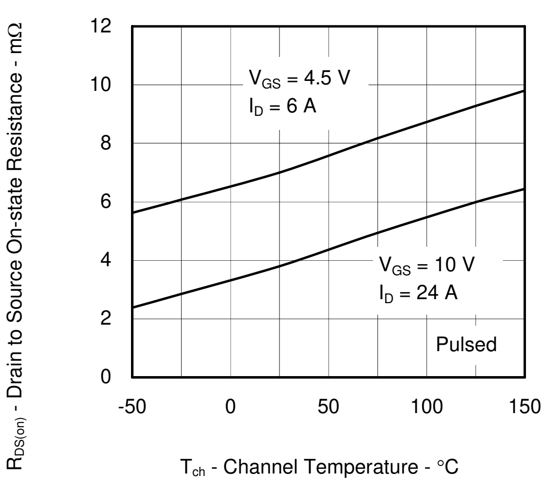
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



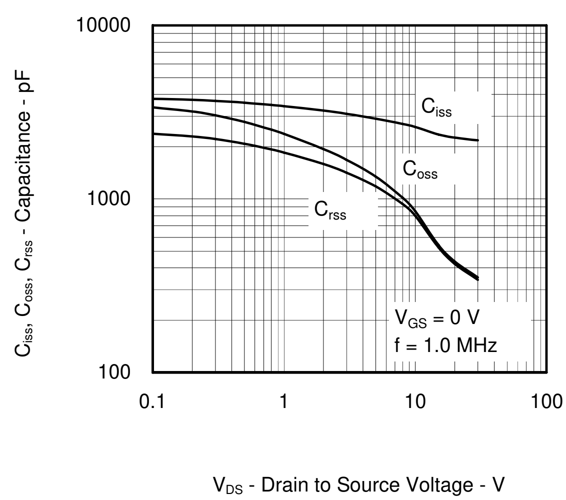
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



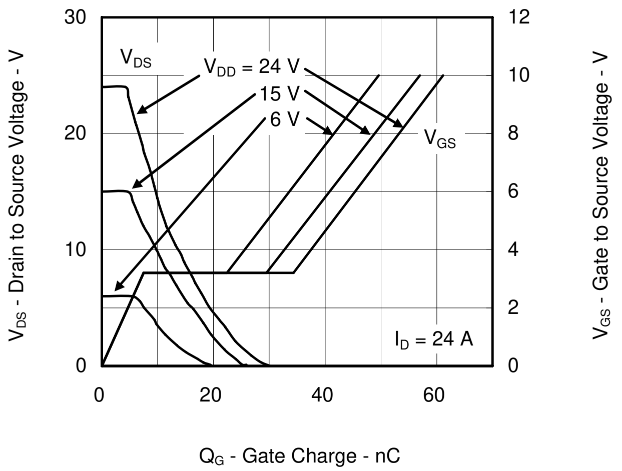
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



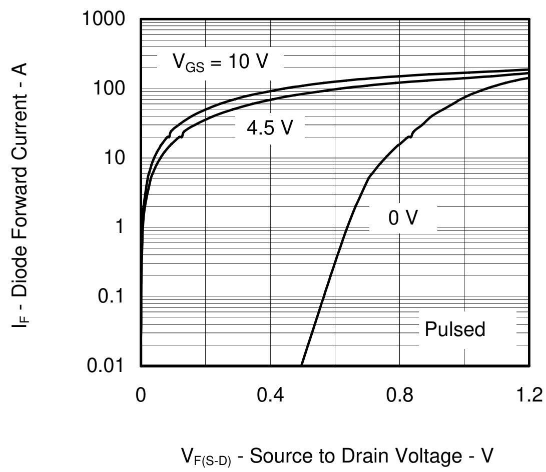
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

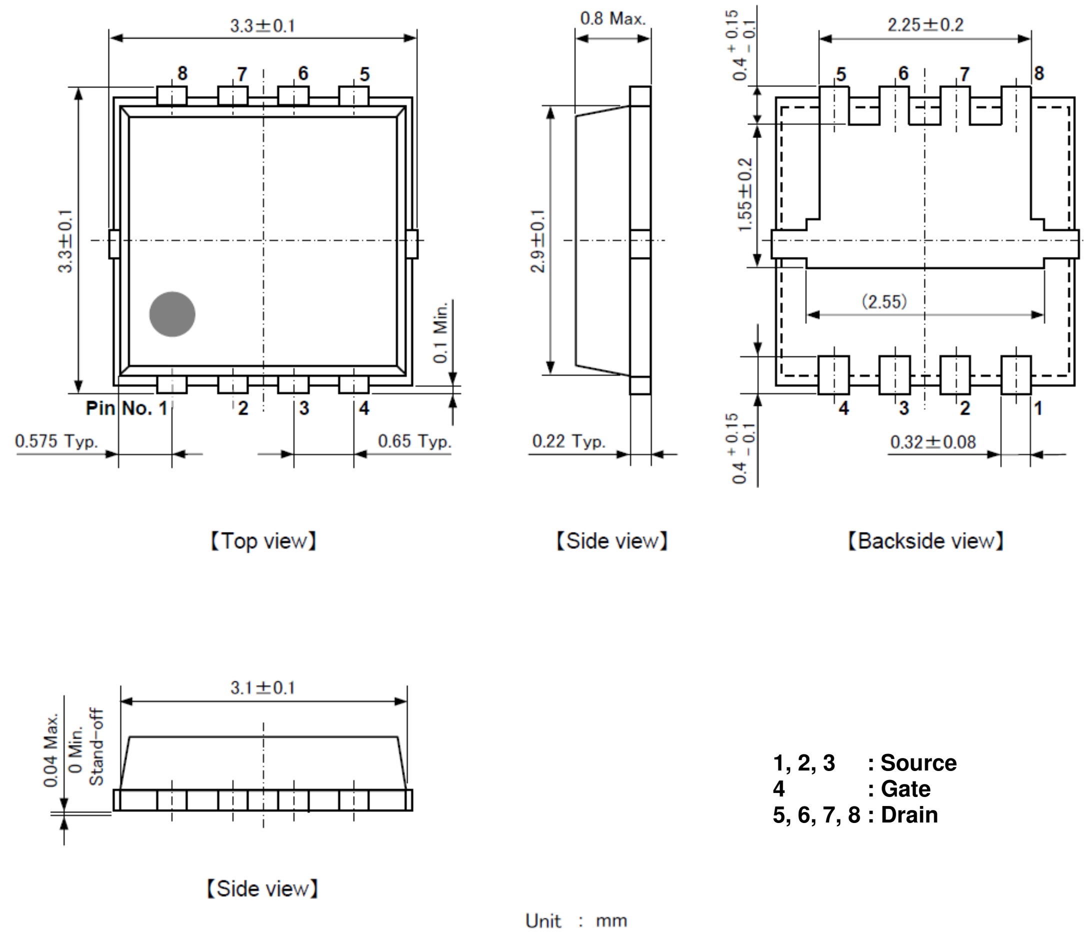


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

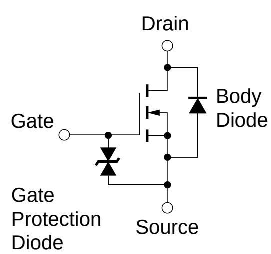


Package Drawings (Unit: mm)

HWSON-8



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History	μPA2825T1S Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	May 25, 2012	–	First Edition Issued

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