Data Sheet

ACFL-3161

10-Amp Peak Gate Drive Optocoupler for SiC MOSFET/IGBT in SO-12 Package

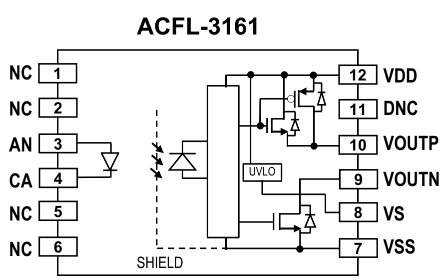
Description

The Broadcom® ACFL-3161 driver is a 10A peak, rail-to-rail output gate drive optocoupler. The ACFL-3161 comes in a compact, surface-mountable SO-12 package for space-savings. It provides an isolation voltage of 5 kV_{rms} between input and output channels.

The ACFL-3161 is primarily designed with high peak driving current capability to ensure optimum performance for direct driving SiC MOSFET or IGBT in various applications. The ACFL-3161 features fast propagation delay and tight dead time distortion, which make it ideal for driving SiC MOSFET and IGBTs at high frequency.

Broadcom isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

Figure 1: Functional Diagram



CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The component featured in this data sheet is not to be used in military or aerospace applications or environments. The component is also not AEC-Q100 qualified and not recommended for automotive applications.

Features

- Features
- Industrial temperature range: –40°C to +125°C
- High output driving current: 10A peak
- Rail-to-rail output voltage
- Propagation delay: 95 ns max.
- Dead time distortion: 35 ns max.
- Wide operating supply (V_{DD}) range: 15V to 30V
- Under Voltage Lock-out (UVLO) protection with hysteresis
- Low supply current allows bootstrap half-bridge topology: I_{DD} = 4 mA max.
- Common Mode Transient Immunity (CMTI): 100 kV/µs at V_{CM} = 1000V
- High noise immunity
  – Direct LED input with low input impedance and low noise sensitivity
- Single-channel in SO-12 package with 8 mm creepage and clearance
- Regulatory approvals:
  – UL1577 5k V_{rms} for 1 min
  – CAN/CSA-C22.2 No. 62368-1
  – IEC/EN 60747-5-5 V_{IORM} = 1230 V_{PEAK}

Applications

- Motor drive for Industrial automation and robotics
- Power supply and charger
- Renewable energy inverter and storage

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	UL 5000 V_{rms}/ 1 Minute Rating	IEC/EN 60747-5-5	Quantity
ACFL-3161	-000E	Stretched SO-12	X	—	X	X	80 per tube
	-500E		X	X	X	X	1000 per reel

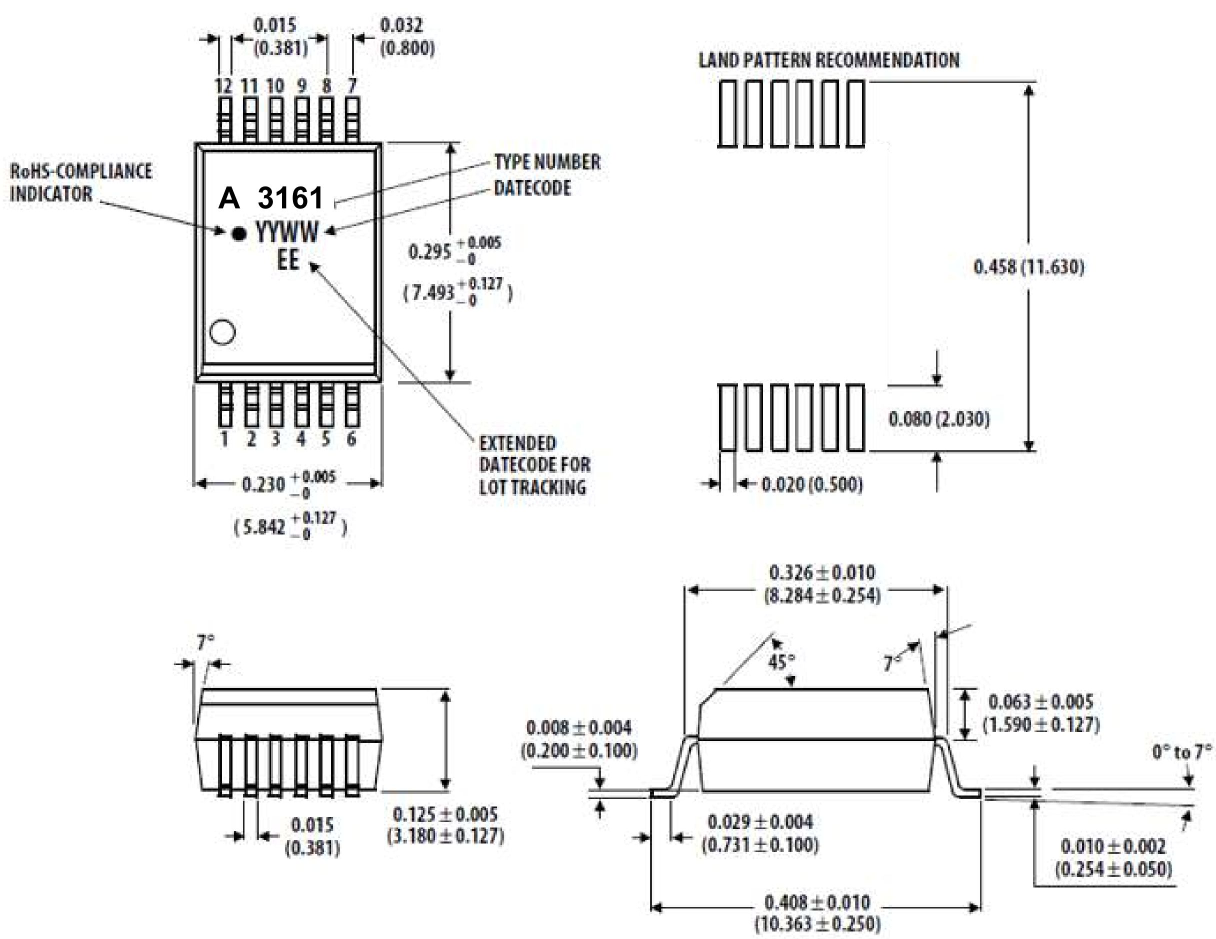
To order, choose a part number from the part number column and combine it with the desired option from the option column to form an order entry.

Example: ACFL-3161-500E to order the product of SSO-12 Surface Mount package in Tape and Reel packaging with IEC/EN 60747-5-5 Safety Approval in RoHS compliant.

Options data sheets are available. Contact your Broadcom sales representative or an authorized distributor for information.

Package Outline Drawing

Figure 2: ACFL-3161 Outline Drawing



Dimensions in inches (millimeters)

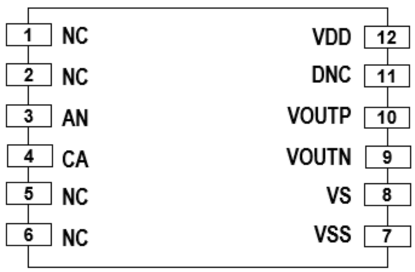
Lead coplanarity = 0.004 inches (0.1 mm)

Product Overview Description

The ACFL-3161 (shown in Figure 1) is a single channel, high peak driving current, rail-to-rail output isolated SiC MOSFET/ IGBT gate driver in compact SO-12 package. It can operate over wide V_{DD} range of 15V to 30V with undervoltage lock-out protection. The ACFL-3161 has a pair of source and sink outputs to facilitate tuning of turn-on and turn-off gate resistors. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increasing noise immunity.

Package Pinout

Figure 3: ACFL-3161 Pinouts



Pin Description

Pin Number	Name	Function
1	NC	No connection
2	NC	No connection
3	AN	Anode
4	CA	Cathode
5	NC	No connection
6	NC	No connection

Pin Number	Name	Function
12	V_{DD}	Driver positive supply voltage
11	DNC	Do not connect (Internally connected to VSS lead frame)
10	V_{OUTP}	Driver output to turn on gate of MOSFET/IGBT
9	V_{OUTN}	Driver output to turn off gate of MOSFET/IGBT
8	V_S	Driver common (connect to MOSFET source/ IGBT emitter reference)
7	V_{SS}	Driver negative power supply

Recommended PB-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Non-halide flux should be used.

Regulatory Information

The ACFL-3161 is approved by the following organizations:

- **UL** – Recognized under UL 1577, component recognition program up to V_{ISO} = 5000 V_{rms}
- **CSA** – CAN/CSA-C22.2 No. 62368-1
- **IEC/EN 60747-5-5** – IEC 60747-5-5, EN 60747-5-5

IEC/EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1 For Rated Mains Voltage ≤ 150 V_{rms} For Rated Mains Voltage ≤ 300 V_{rms} For Rated Mains Voltage ≤ 600 V_{rms} For Rated Mains Voltage ≤ 1000 V_{rms}		 I – IV I – IV I – IV I – III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1230	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial discharge < 5 pC	V_{PR}	2306	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial discharge < 5 pC	V_{PR}	1968	V_{PEAK}
Highest Allowable Overvoltage[a] (Transient Overvoltage t_{ini} = 60 seconds)	V_{IORM}	8000	V_{PEAK}
Safety-limiting values – maximum values allowed in the event of a failure[b] Case Temperature Input Current Output Power	 T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulation section IEC/EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

b. Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in application. Surface mount classification is Class A in accordance with CECCOO802.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.3	mm	Through insulation, distance conductor to conductor, usually the straight-line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 600	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		I	—	Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Unless otherwise specifies, all voltages at output IC reference to V_{SS}

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	–55	150	°C	
Operating Temperature	T_A	–40	125	°C	
IC Junction Temperature	T_J	—	150	°C	a
Average LED Input Current	$I_{F(AVG)}$	—	20	mA	
Peak Transient LED Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$	—	1	A	
Reverse Input Voltage ($V_{CA} – V_{AN}$)	V_R	—	6	V	
Total Output IC Supply Voltage	$(V_{DD} – V_{SS})$	–0.5	35	V	
Positive Output IC Supply Voltage	$(V_{DD} – V_S)$	–0.5	$35 – (V_S – V_{SS})$	V	
Negative Output IC Supply Voltage	$(V_S – V_{SS})$	–0.5	17	V	
High Side Output Voltage	$V_{OH(PEAK)}$	$V_{SS} – 0.5$	V_{DD}	V	
Low Side Output Voltage	$V_{OL(PEAK)}$	$V_{SS} – 0.5$	V_{DD}	V	
V_{OH} Output Sourcing Current	I_{OH}	–10	—	A	b
V_{OL} Output Sinking Current	I_{OL}	—	10	A	b
Output IC Power Dissipation	P_O	—	500	mW	c
Total Power Dissipation	P_T	—	550	mW	a

a. Total power dissipation is derated linearly above 105°C at a rate of 21 mW/°C to 130 mW at 125°C. Maximum LED and IC junction temperature must not exceed 150°C.

b. Maximum pulse width = 100 ns and duty cycle at 0.4%.

c. Output IC power dissipation is derated linearly above 105°C from 500 mW to 360 mW at 125°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Operating Temperature	T_A	–40	125	°C	
Total Output IC Supply Voltage	$(V_{DD} – V_{SS})$	15	30	V	
Positive Output IC Supply Voltage	$(V_{DD} – V_S)$	15	$30 – (V_S – V_{SS})$	V	
Negative Output IC Supply Voltage	$(V_S – V_{SS})$	0	15	V	
Input LED Turn on Current (ON)	$I_{F(ON)}$	10	16	mA	
Input LED Turn off Voltage ($V_{AN} – V_{CA}$)	$V_{F(OFF)}$	–5.5	0.8	V	
Output IC Supply Decoupling Capacitor ($V_{DD} – V_{SS}$)	C_{VDD}	10	—	µF	a
Minimum Input Pulse Width	$t_{ON(LED)}$	100	—	ns	b

a. It is recommended to check external decoupling capacitor derating guidelines.

b. Minimum input pulse width for a guarantee output pulse under no load condition.

Electric Specifications (DC)

Unless otherwise specified, all minimum/maximum specifications are at recommended operating conditions. All typical values are at T_A = 25°C, $V_{DD} – V_S$ = 15V, $V_{SS} – V_S$ = –15V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
V_{OUTP} High Level Peak Sourcing Current	I_{OH}	—	–10	–6	A	$V_{DD} – V_{OUTP}$ = 15V	15	a
V_{OUTN} Low Level Peak Sinking Current	I_{OL}	6	9	—	A	$V_{OUTN} – V_{SS}$ = 15V	14	a
V_{OUTP} Output Transistor $R_{DS(ON)}$	$R_{DS,OH}$	0.4	0.8	1.3	Ω	I_{OH} = –3A		b
V_{OUTN} Output Transistor $R_{DS(ON)}$	$R_{DS,OL}$	0.2	0.6	1.2	Ω	I_{OL} = 3A		b
V_{OUTP} Output Voltage	V_{OH}	V_{DD} – 0.3	V_{DD} – 0.07	—	V	I_F = 10 mA, I_{OH} = –10 mA		c
V_{OUTN} Output Voltage	V_{OL}	—	0.06	0.3	V	V_F = 0V, I_{OL} = 100 mA		
UVLO Threshold Low to High, $V_{DD} – V_S$	V_{UVLO+}	13	13.6	14.2	V	I_F = 10 mA, V_{OH} > 5V		
UVLO Threshold High to Low, $V_{DD} – V_S$	$V_{UVLO–}$	12	12.5	13.1	V	I_F = 10 mA, V_{OL} < 5V		
UVLO Hysteresis, $V_{DD} – V_S$	V_{UVLO_HYS}	0.8	1.1	1.3	V			
High Level Supply Current	I_{DDH}	—	2.8	4	mA	I_F = 10 mA, No Load	13	
Low Level Supply Current	I_{DDL}	—	2.7	4	mA	V_F = 0V, No Load	12	
LED Current Threshold (Low to High)	I_{TH+}	0.5	2.5	7	mA			
LED Current Threshold (High to Low)	$I_{TH–}$	—	1.9	6	mA			
LED Turn on Current Hysteresis	I_{TH_HYS}	—	0.6	—	mA			
LED Forward Voltage ($V_{AN} – V_{CA}$)	V_F	1.25	1.55	1.85	V	I_F = 10 mA	11, 16	
Temperature Coefficient of LED Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.7	—	mV/°C	I_F = 10 mA		
LED Threshold Voltage (High to Low)	V_{FHL}	0.8	—	—	V			
LED Reverse Breakdown Voltage ($V_{CA} – V_{AN}$)	V_{BR}	6	—	—	V	I_F = –100 µA		
LED Input Capacitance	C_{IN}	—	30	—	pF			

a. Short circuit pulsed current at $V_{DD} – V_{SS}$ = 30V and pulse duration less than 1 µs.

b. Output is sourced at –3A or 3A with maximum pulse width of 10 µs.

c. V_{OH} is measured with a DC load current. Maximum pulse width = 1 ms. When driving capacitive loads, V_{OH} will approach V_{DD} as I_{OH} approaches zero amps.

Switching Specifications (AC)

Unless otherwise specified, all minimum/maximum specifications are at recommended operating conditions. All typical values at T_A = 25°C, $V_{DD} - V_S$ = 15V, $V_{SS} - V_S$ = –15V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
Input Pulse to High Level Output Propagation Delay Time	t_{PLH}	45	67	95	ns	C_L= 2.2 nF, f = 20 kHz, Duty cycle = 50% Rg = 4.7Ω Rin = 240Ω V_{IN} = 5V	8, 4, 5	
Input Pulse to Low Level Output Propagation Delay Time	t_{PHL}	45	67	95	ns		9, 4, 5	
Pulse Width Distortion ($t_{PHL} - t_{PLH}$)	PWD	–25	—	25	ns		10	a
Dead Time Distortion Caused by Any Two Parts ($t_{PLH} - t_{PHL}$)	DTD	–35	—	35	ns			b
Propagation Delay Skew	t_{PSK}	—	—	35	ns			c
Output Rise Time (20% to 80%)	t_R	—	7	15	ns			
Output Fall Time (80% to 20%)	t_F	—	7	15	ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	100	—	—	kV/µs	T_A = 25°C, V_{DD} = 30V, V_{CM} = 1 kV, with current limiting resistors at both AN and CA node	6	d
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	100	—	—	kV/µs		7	e

a. Pulse width distortion (PWD) is defined as $t_{PHL} - t_{PLH}$ for any given device.

b. Dead time distortion (DTD) is defined as $t_{PLH} - t_{PHL}$ between any two parts under the same test condition. A negative DTD reduces original system dead time; while a positive DTD increases original system dead time.

c. Propagation delay skew (t_{PSK}) is the difference in the t_{PHL} or t_{PLH} between any two units under the same test conditions.

d. Common mode transient immunity in the high state is the maximum tolerable dVCM/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in the high state, (i.e., V_O > 10V).

e. Common mode transient immunity in a low state is the maximum tolerable dVCM/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in a low state (i.e., V_O < 1.0V).

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{rms}	RH < 50%, t = 1 min. T_A = 25°C	
Resistance (Input-Output)	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 V_{DC}	
Capacitance (Input-Output)	C_{I-O}	—	0.4	—	pF	f = 1 MHz	

Parameter Measurements

Figure 4 depicts the test setup to measure the gate driver's propagation delay. Note that without the load capacitance, typical measured delays can be reduced by 7% to 10%. These settings correlate to the loading effects found in most applications.

Figure 4: Propagation Delay Measurement Test Setup

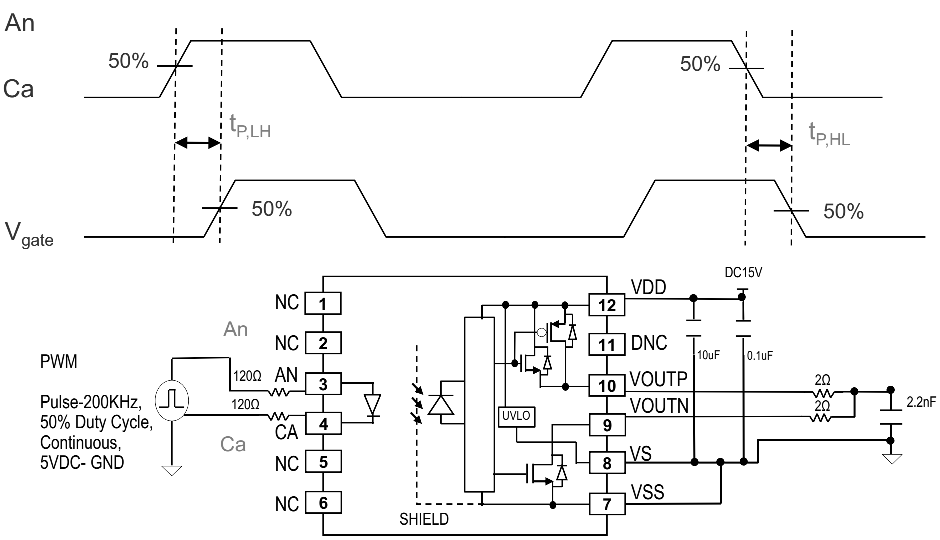
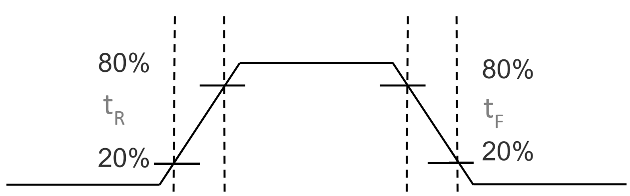


Figure 5 shows the 20% to 80% rise and fall time measurement.

Figure 5: Rise and Fall Time Measurement



The common mode rejection test circuitries are shown in the following figures. Both CMR High (Figure 6) and Low (Figure 7) V_O are probed in the presence of V_{CM} at 1000V.

Figure 6: CMR V_O High Test Circuit

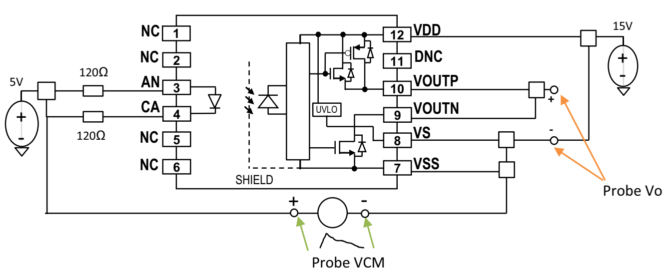
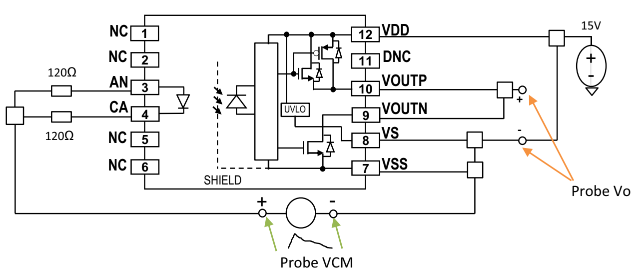


Figure 7: CMR V_O Low Test Circuit



Typical Performance Plots

$V_{DD} – V_S$ = 15V, $V_{SS} – V_S$ = –15V. With capacitance load of 2.2 nF, unless otherwise noted.

Figure 8: t_{PLH} vs Temperature (V_{OUTP})

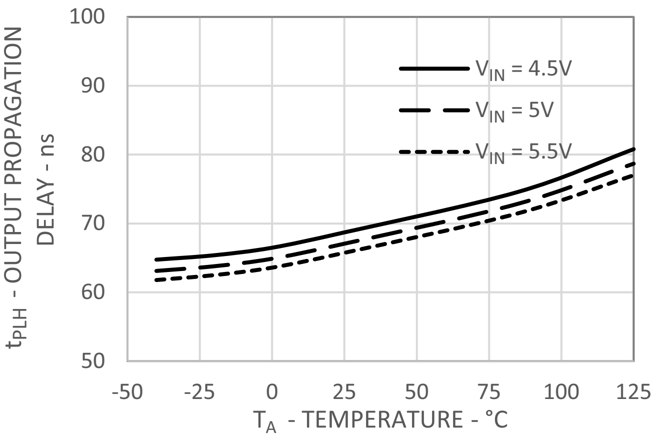


Figure 9: t_{PHL} vs Temperature (V_{OUTN})

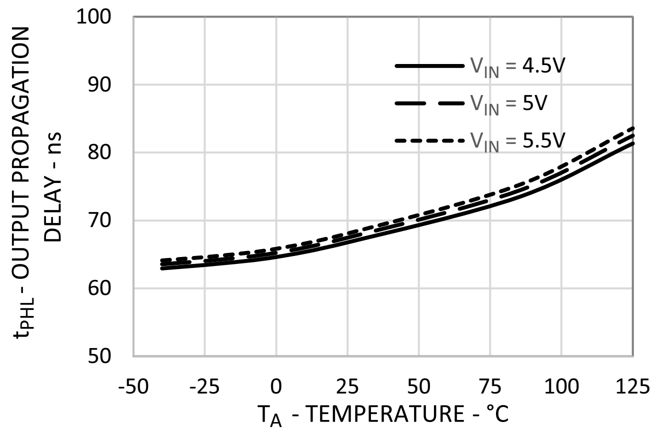


Figure 10: Pulse Width Distortion vs Temperature

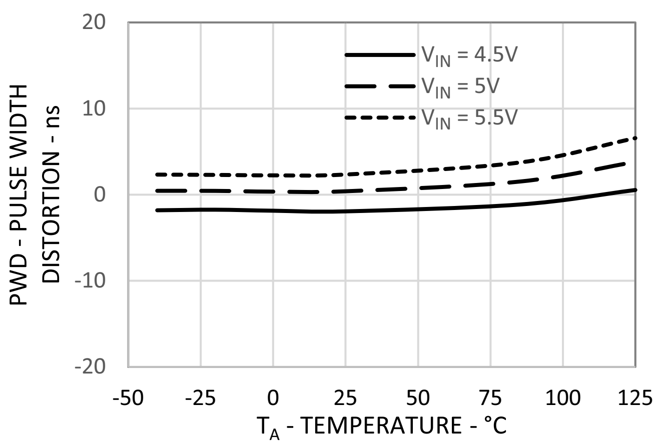


Figure 11: V_F vs Temperature

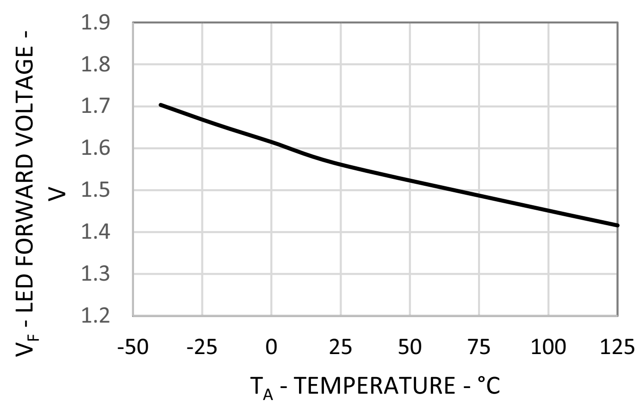


Figure 12: I_{DDL} vs Temperature

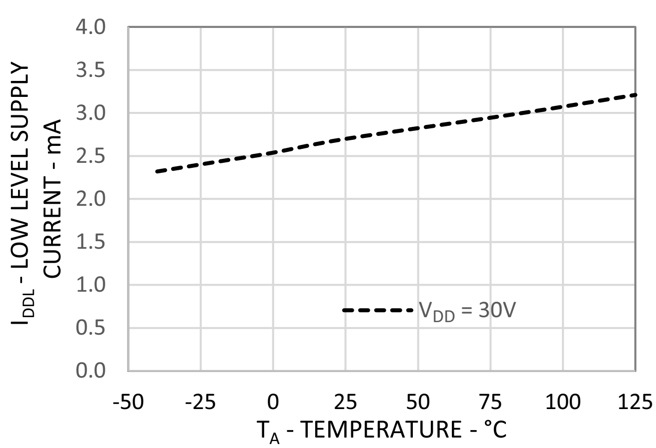


Figure 13: I_{DDH} vs Temperature

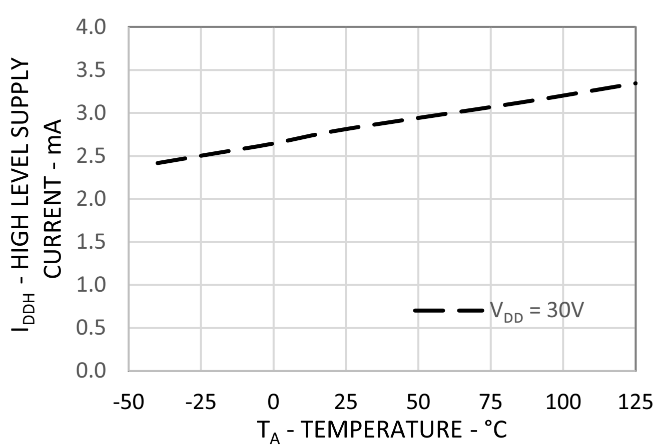


Figure 14: I_{OL} vs V_{OUTN}

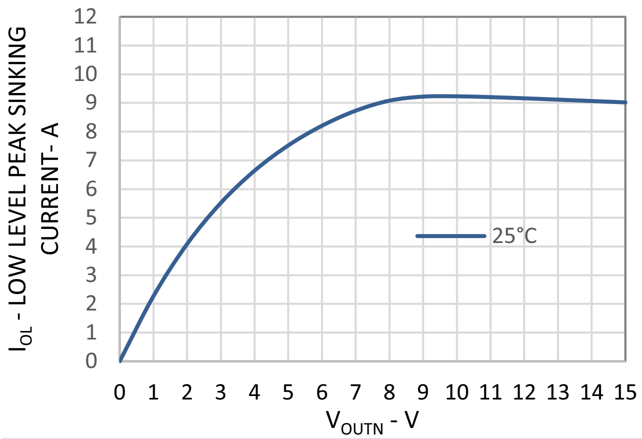


Figure 15: I_{OH} vs (V_{DD} – V_{OUTP})

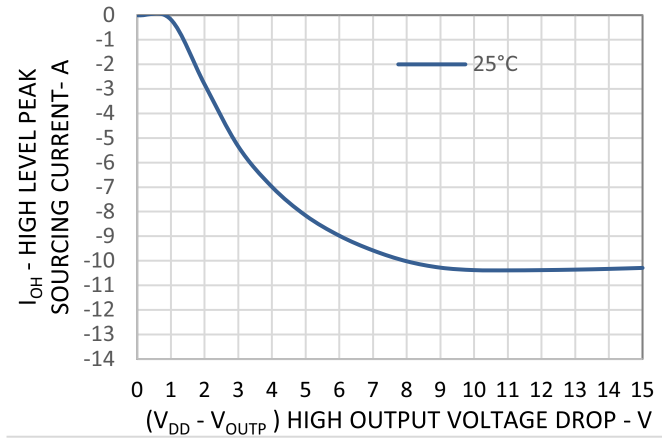
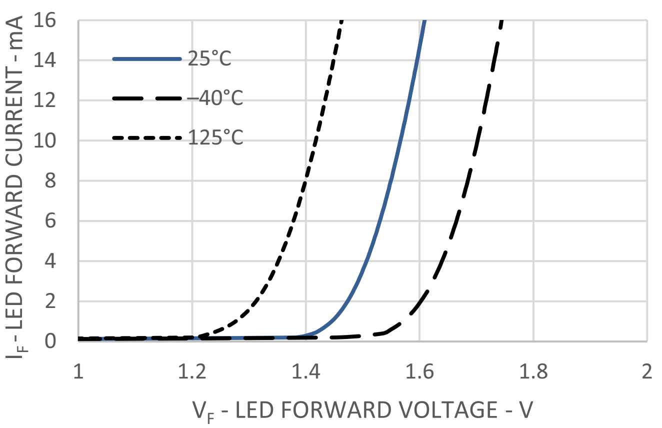


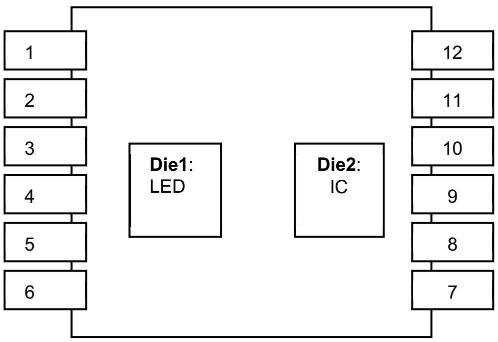
Figure 16: I_F vs V_F



Thermal Resistance Model for ACFL-3161

The diagram for Thermal Resistance measurement is shown in Figure 17. This is a multi-chip package with two heat sources. Effects for heating of one die due to the adjacent dice are considered by applying the theory of linear superposition. One die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in a matrix form. This yields a 2-by-2 matrix for our case of two heat sources.

Figure 17: Thermal Resistance Measurements



$$\begin{vmatrix} R11 & R12 \\ R21 & R22 \end{vmatrix} \cdot \begin{vmatrix} P1 \\ P2 \end{vmatrix} = \begin{vmatrix} \Delta T1 \\ \Delta T2 \end{vmatrix}$$

Definitions

R_{11}: Thermal Resistance of Die1 due to heating of Die1 (°C/W)

R_{12}: Thermal Resistance of Die1 due to heating of Die2 (°C/W)

R_{21}: Thermal Resistance of Die2 due to heating of Die1 (°C/W)

R_{22}: Thermal Resistance of Die2 due to heating of Die2 (°C/W)

P_1: Power dissipation of Die1 (W)

P_2: Power dissipation of Die2 (W)

T_1: Junction temperature of Die1 due to heat from all dice (°C)

T_2: Junction temperature of Die2 due to heat from all dice (°C)

T_A: Ambient temperature (°C)

ΔT_1: Temperature difference between Die1 junction and T_A

ΔT_2: Temperature deference between Die2 junction and T_A

Equation 1:

$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_A$

Equation 2:

$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_A)$

Measurements Data

Measurement is done on a high effective thermal conductivity board according to JEDEC Standard 51-7.

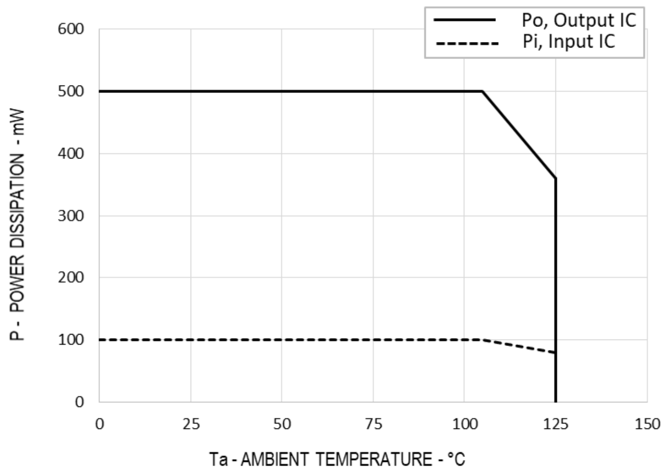
$$\begin{vmatrix} R11 & R12 \\ R21 & R22 \end{vmatrix} = \begin{vmatrix} 193.6 & 24.93 \\ 29.22 & 43.83 \end{vmatrix} °C/W$$

The junction temperature of LED and detector IC for any given power and ambient temperature can be calculated by using Equation 1 and Equation 2 with the measured thermal resistance values shown above. It is to be noted that the junction temperature increases proportionally with the increase in ambient temperature.

Power Dissipation Derating Chart

The power-derating chart Figure 18 shown the Die1 (LED) and Die2 (Output IC) power profile from 0°C to 125°C.

Figure 18: Power Derating Chart Based on High Effective Thermal Conductivity Board



The Die1 (LED) power dissipation is derated linearly 1 mW/°C above 105°C (100 mW) to 125°C (80 mW). While, Die2 (Output IC) is derated linearly 7 mW/°C above 105°C (500 mW) to 125°C (360 mW).

Notes on Thermal Calculation

Application and environmental design for ACFL-3161 needs to ensure that the junction temperature of the internal ICs and LED do not exceed 150°C. The following equations are for the purposes of calculating the maximum power dissipation and corresponding effects on junction temperatures. The thermal resistance model shown here is not meant to and will not predict the performance of a package in an application-specific environment; it can only be used as a reference for thermal performance comparison under specified PCB layout as shown in Figure 18.

Calculation of Input LED Power Dissipation - P_1

Input LED Power Dissipation (P_1) = $I_{F(LED)}$ (Recommended Max.) × $V_{F(LED)}$ (at 125°C) × Duty Cycle

Example:

P_1 = 16 mA × 1.85V × 50% duty cycle = 14.8 mW

Calculation of Output IC Power Dissipation- P_2

Output IC Power Dissipation (P_2) = $P_{O(Static)} + P_{HS} + P_{LS}$

Where:

- $P_{O(Static)}$: Static power dissipated by the output IC = $I_{DD} \times V_{DD}$
- P_{HS}: High side switching power dissipation at V_{OH} pin = $(V_{DD} \times Q_G \times f_{PWM}) \times R_{DS,OH(MAX)}/(R_{DS,OH(MAX)} + R_{GH}) / 2$
- P_{LS}: Low side switching power dissipation at V_{OL} pin = $(V_{DD} \times Q_G \times f_{PWM}) \times R_{DS,OL(MAX)}/(R_{DS,OL(MAX)} + R_{GL}) / 2$
- Q_G: IGBT gate charge at supply voltage
- f_{PWM}: Input LED switching frequency
- $R_{DS,OH(MAX)}$: Maximum high side output impedance
- R_{GH}: Gate charging resistance
- $R_{DS,OL(MAX)}$: Maximum low side output impedance
- R_{GL}: Gate discharging resistance

Example:

P_{HS} = (15V × 100 nC × 200 kHz) × 1.3Ω/ (1.3Ω + 2.2Ω) / 2 = 56 mW

P_{LS} = (15V × 100 nC × 200 kHz) × 1.2Ω/ (1.2Ω + 2.2Ω) / 2 = 53 mW

$P_{O(Static)}$ = 4 mA (Data Sheet Max.) × 15V = 60 mW

P_2 = 60 mW + 56 mW + 53 mW = 169 mW

Calculation of Junction Temperature for High Effective Thermal Conductivity Board

Example:

Input LED Junction Temperature, T_1

= $(R_{11} \times P_1 + R_{12} \times P_2) + T_A$

= (193.6°C/W × 14.8 mW + 24.93°C/W × 169 mW) + 125°C

= 132°C < T_J(absolute max) of 150°C

Output IC Junction Temperature, T_2

= $(R_{21} \times P_1 + R_{22} \times P_2) + T_A$

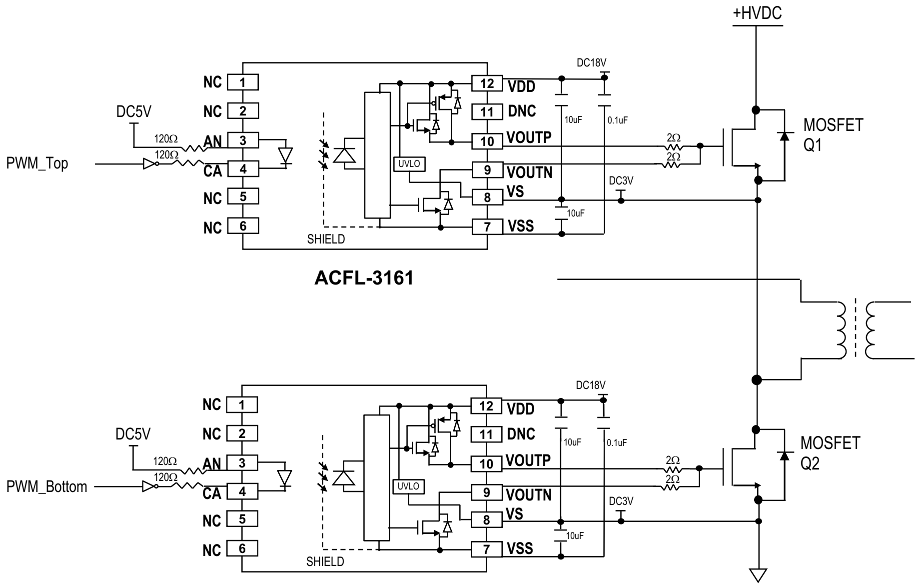
= (29.22°C/W × 14.8 mW + 43.83°C/W × 169 mW) + 125°C

= 133°C < T_J(absolute max) of 150°C

NOTE: Junction temperature of T_1 and T_2 must not exceed 150°C at given ambient temperature T_A.

Typical Application Circuit

Figure 19: ACFL-3161 Typical Application Circuit



NOTE: Component value is subjected to change based on application conditions.

Sizing the External Gate Resistor

The ACFL-3161 has a set of source and sink and outputs that offers flexibility in tuning the turn-on and turn-off gate resistors for optimum MOSFET/IGBT switching performance. Typically, when working on a new design, the gate resistor value can be selected based on the recommended values given in MOSFET/IGBT data sheet under certain test conditions. However, it is also important to consider the gate driver capability during the design so that peak gate current is within the recommended ratings of the driver. If the ACFL-3161 is used to drive MOSFET/IGBT directly, designer has to consider the power dissipation for both gate driver and external gate resistors.

Example:

Given V_{DD} = 18V, V_{SS} = –5V:

- Recommended $I_{OH(PEAK)}$ = Maximum V_{OUTP} peak output souring current = –6A
- Recommended $I_{OL(PEAK)}$ = Minimum V_{OUTN} peak output souring current = 6A
- Minimum gate turn-on resistor, Rgon(min) ≥ $(V_{DD} – V_{SS})/I_{OH(PEAK)} – R_{DS,OH(ON)}$ = 23V/6A – 0.4Ω = 3.43Ω
  – Select Rgon = 4Ω to start with.
- Minimum gate turn-off resistor, Rgon(min) ≥ $(V_{DD} – V_{SS})/I_{OL(PEAK)} – R_{DS,OL(ON)}$ = 23V/6A – 0.2Ω = 3.63Ω
  – Select Rgoff = 4Ω to start with.

Power dissipation of gate resistors can be calculated as follows:

Power dissipation in turn-on gate resistor, $P_{(Rgon)}$= Average $Igate(on)^2$ × Rgon

Power dissipation in turn-off gate resistor, $P_{(Rgoff)}$= Average $Igate(off)^2$ × Rgoff

Once initial Rgon and Rgoff values are selected, test the circuit with MOSFET/IGBT under actual application conditions to check for switching losses, MOSFET/IGBT voltage spike, and so on, to fine tune the gate resistor values.

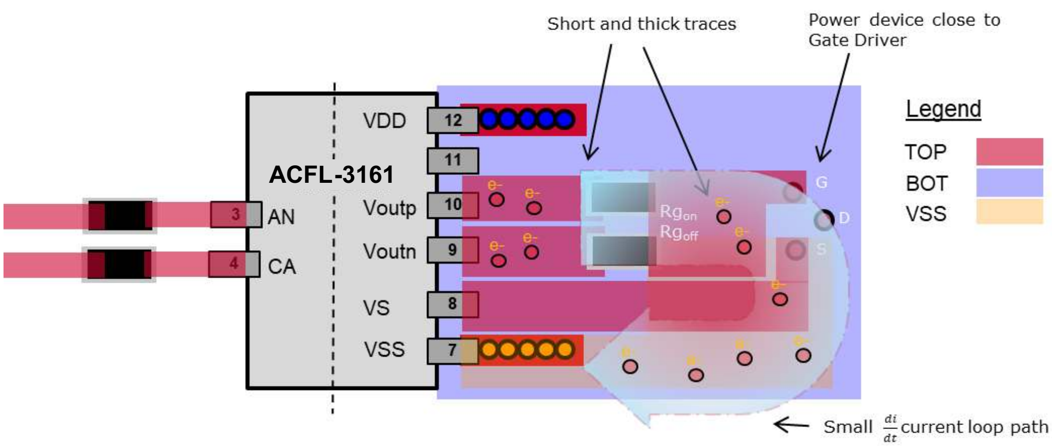
Layout Guidelines

The gate driver's output sinks about 10A, which the return current path of minimum inductance must be implemented during printed circuit board layout design to alleviate the effect of ground bounce; as the excitation of parasitic elements in the PCB/ gate driver become dominant.

The smallest loop between the outbound and return currents forms the least inductance. The gate driver should be placed close to the power devices (i.e., MOSFET/IGBT) with short and thick traces to minimize the parasitic inductance along the high current switching path.

Adequate spacing should always be maintained between the high voltages isolated circuitry and any input referenced circuitry. Minimum spacing between two adjacent high-side isolated channels (i.e. top and bottom channels) must be maintained as well. Insufficient spacing will reduce the effective isolation and may increase parasitic coupling that will degrade part performance. Figure 20 shows the recommended PCB layout guidelines.

Figure 20: PCB Layout Guidelines



The placement and routing of supply bypass capacitors requires special attention. During switching transients, the majority of gate charge is supplied by bypass capacitors. Maintaining short bypass capacitor trace lengths will ensure low supply ripple and clean switching waveforms. It is recommended to connect the bypass capacitors to power plane and ground plane with multiple via holes. The planes can provide better heat dissipation at the same time serve a natural decoupling capacitor to the IC.

Figure 21 shows the recommended bypass capacitors placement and PCB planes stack-up.

Figure 21: PCB Planes Stack-Up and Bypass Capacitors Placement